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ESE 2020 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 2

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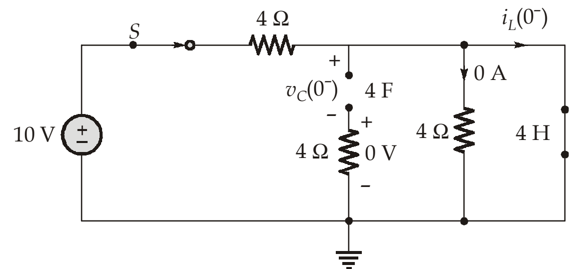
DETAILED EXPLANATIONS
Section A : Network Theory

1. (d)

Superposition theorem can't be used for the given circuit, because while acting one source alone, the circuit violates KVL.

2. (b)

At $t = 0^-$:



$$i_L(0^-) = \frac{10\text{ V}}{4\ \Omega} = 2.5\text{ A}$$

$$v_C(0^-) = 0\text{ V}$$

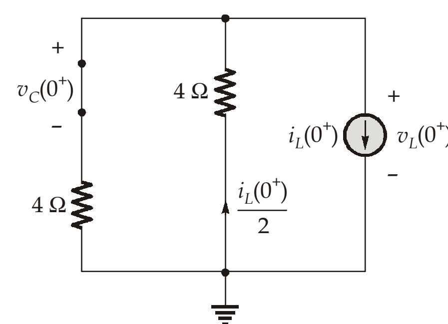
At $t = 0^+$:

$$v_C(0^+) = v_C(0^-) = 0\text{ V}$$

$$i_L(0^+) = i_L(0^-) = 2.5\text{ A}$$

$$v_L(0^+) = -(4\ \Omega)\frac{i_L(0^+)}{2}$$

$$= -4\times\frac{2.5}{2} = -5\text{ V}$$



3. (b)

Average power absorbed by a load depends only on fundamental components.

$$v(t) = 100\cos(\omega t) = 100\sin(\omega t + 90°)\text{ V}$$

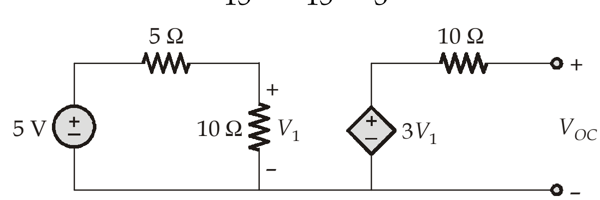
So,
$$P_{\text{avg(load)}} = \frac{V_1 I_1}{2}\cos\phi = \frac{100\times 5}{2}\cos(90° - 30°)\text{ mW}$$

$$= 250\cos(60°) = 125\text{ mW} = 0.125\text{ W}$$

4. (b)

From the given circuit, we have

$$V_1 = \frac{5\times 10}{15} = \frac{50}{15} = \frac{10}{3}\text{ V}$$



$$\therefore \quad V_{OC} = 3V_1 = 3\times\frac{10}{3} = 10\text{ V}$$

$$I_{SC} = \frac{10}{10} = 1\text{ A}$$

$$\therefore \quad R_{\text{Th}} = \frac{V_{OC}}{I_{SC}} = 10\ \Omega$$

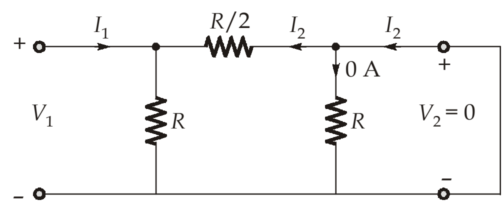
so,
$$P_{\max} = \frac{V_{Th}^2}{4R_{Th}} = \frac{V_{OC}^2}{4R_{Th}} = \frac{10\times 10}{4\times 10} = 2.5\text{ W}$$

5. (c)

Using transmission parameters,

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2$$

$$\therefore \quad \text{parameter } D = \left.\frac{-I_1}{I_2}\right|_{V_2=0}$$



$$I_2 = -I_1 \times \frac{R}{R+(R/2)} = -I_1 \times \frac{2}{3}$$

$$D = \left.\frac{-I_1}{I_2}\right|_{V_2=0} = \frac{3}{2}$$

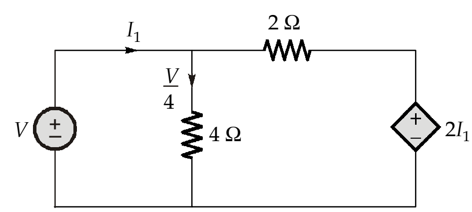
6. (b)

$$V = R_{eq}\, I_1$$

$$-I_1 + \frac{V}{4} + \frac{V-2I_1}{2} = 0$$

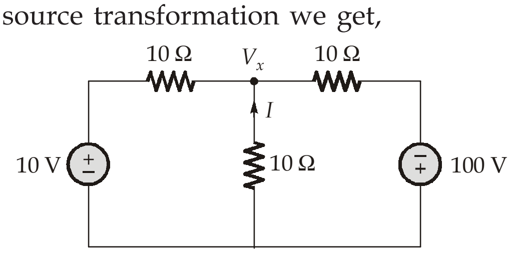
$$\frac{V}{4} + \frac{V}{2} = 2\, I_1$$

$$\frac{V}{I_1} = R_{eq} = (8\,||\,4) = \frac{8}{3} = 2.67\ \Omega$$



7. (c)

Redrawing the circuit after source transformation we get,



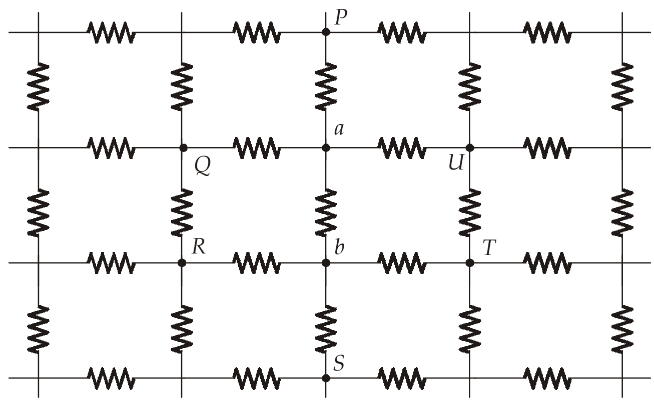
$$\frac{V_x - 10}{10} + \frac{V_x + 100}{10} + \frac{V_x}{10} = 0$$

$$3V_x + 90 = 0$$

$$V_x = -30 \text{ V}$$

$$\therefore \quad I = -\frac{V_x}{10} = \frac{30}{10} = 3 \text{ A}$$

8. (b)



Let the current flowing into the circuit at the node '*a*' will be *I*. Since the infinite network is symmetrical about '*a*', the current *I* in going from '*a*' to infinity, is divided equally along the branches *aQ*, *aU*, *aP* and *ab* as shown in the figure.

The current '*I*' then returns from infinity and is taken from the network at node '*b*'.

Again by symmetry, the current flowing along the branches *Rb*, *ab*, *Sb* and *Tb* are $I/4$.

∴ Total current flowing along *ab* is $I/4 + I/4 = I/2$

$$\therefore \quad V_{ab} = I/2 \times R$$

∴ Effective resistance $R_{ab} = R/2$.

9. (a)

Initially,
$$C_1 = 5 \text{ μF and } Q_1 = 17 \text{ μC}$$
$$C_2 = C \text{ μF and } Q_2 = 0$$
$$\therefore \quad Q_T = Q_1 + Q_2 = 17 \text{ μC} \quad \text{...(i)}$$

When C_1 is connected to C_2 parallely, the charge is transferred from C_1 to C_2. However the total charge remains equal to 17 μC. Due to the law of conservation of charge, for the capacitors connected in parallel.

$$\therefore \quad V_1 = V_2$$

$$\frac{Q_1}{C_1} = \frac{Q_2}{C_2}$$

$$\frac{10}{5} = \frac{7}{C}$$

$$C = \frac{7}{2} = 3.5 \text{ μF}$$

10. (c)

From z-parameter model,

$$V_1 = z_{11}I_1 + z_{12}I_2 \quad \text{...(i)}$$

$$V_2 = z_{21}I_1 + z_{22}I_2 \quad \text{...(ii)}$$

∵ Output port is short circuited

∴ $V_2 = 0$

∴ $$I_2 = \frac{-z_{21}}{z_{22}} I_1 \quad \text{...(iii)}$$

∴ From equation (i) and (iii),

$$V_1 = \left(z_{11} - \frac{z_{12} \times z_{21}}{z_{22}}\right) I_1$$

or $$I_1 = \frac{V_1}{\left(z_{11} - \frac{z_{12} \times z_{21}}{z_{22}}\right)} = \frac{3}{27 - \frac{9 \times 9}{27}}$$

$$I_1 = \frac{3}{24} = \frac{1}{8} = 0.125 \text{ A} = 125 \text{ mA}$$

11. (b)

The total number of possible links are

$$l = B - n + 1$$

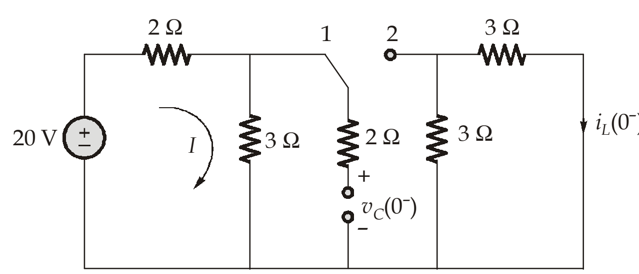
here, $B = 14$

$n = 8$

∴ $l = 14 - 8 + 1 = 7$

12. (c)

At $t = 0^-$ the circuit will be drawn as



By KVL in the first loop,

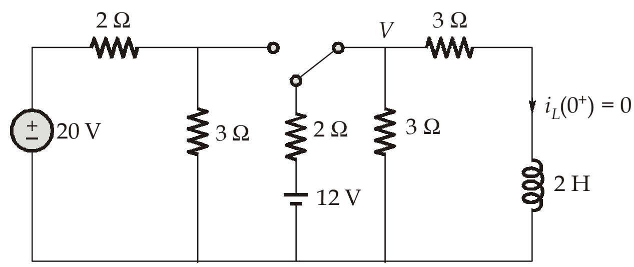
$$2I + 3I - 20 = 0$$

$$I = \frac{20}{5} = 4 \text{ A}$$

∴ $v_C(0^-) = v_C(0^+) = 3 \times 4 = 12 \text{ V}$

$i_L(0^-) = i_L(0^+) = 0$

Now, at $t = 0^+$ the circuit can be redrawn as



$$V = \frac{3 \times 12}{2+3} = 7.2 \text{ V}$$

Also; $$V = 3i(0^+) + \frac{2\,di(0^+)}{dt}$$

at $t = 0^+$, $$i = 0$$

$$V = \frac{2di(0^+)}{dt}$$

or $$\frac{di(0^+)}{dt} = \frac{V}{2} = \frac{7.2}{2} = 3.6 \text{ A/s}$$

13. (b)

The degree of each node in a fully connected graph is equal to $(n - 1)$

14. (a)

For the given circuit $$L_{eq} = L_1 + L_2 \pm 2\text{ M}$$

where $$M \propto \sqrt{L_1 L_2}$$

and $$L \propto N^2$$

when number of turns get halved,

$$L_1' = \frac{1}{4} L_1$$

and $$L_2' = \frac{1}{4} L_2$$

$$L_{eq}' = \frac{1}{4} L_1 + \frac{1}{4} L_2 \pm \frac{1}{4} \times 2\text{ M}$$

$$L_{eq}' = \frac{1}{4}(L_{eq})$$

$\therefore$ $$f_0' = \frac{1}{2\pi\sqrt{L_{eq}' C}} = \frac{1}{2\pi\sqrt{\frac{1}{4} L_{eq} C}}$$

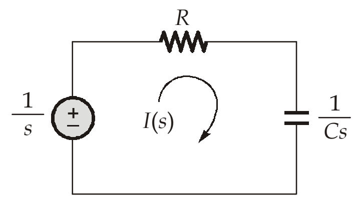
$$= \frac{2}{2\pi\sqrt{L_{eq} C}} = 2 f_0$$

15. (d)

$$i(t) = \frac{1}{8}e^{-t/2}\text{A} \qquad \text{(given)}$$

$$\therefore \quad I(s) = \frac{1}{8\left(s+\frac{1}{2}\right)} = \frac{2}{8(2s+1)} = \frac{1}{4(2s+1)} \qquad \text{...(i)}$$

as per the question,



The KVL equation in the loop

$$\frac{1}{s} = \left(R + \frac{1}{Cs}\right)I(s)$$

$$\frac{1}{s} = \left(\frac{1+RCs}{Cs}\right)I(s)$$

$$I(s) = \frac{C}{(1+RCs)} \qquad \text{...(ii)}$$

Comparing with equation (i), we get

$$C = \frac{1}{4} = 0.25\text{ F}$$

and

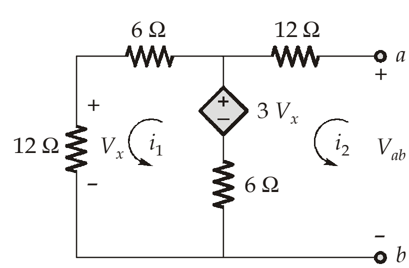
$$RC = 2$$

$$R \times \frac{1}{4} = 2$$

$$R = 8\ \Omega$$

16. (c)

The circuit can be redrawn as



By applying KVL in loop (i), we get,

$$3V_x = 6i_1 + 12i_1 + 6(i_1 - i_2)$$

$$3V_x = 24i_1 - 6i_2 \qquad \text{...(i)}$$

by applying KVL in loop (ii), we get

$$V_{ab} = 12i_2 + 3V_x + 6(i_2 - i_1)$$

$$V_{ab} = 18i_2 + 3[12 \times i_1] - 6i_1$$
$$= 18i_2 + 36i_1 - 6i_1$$
$$V_{ab} = 18i_2 + 30i_1 \quad \text{...(ii)}$$

∴ From equation (i)
$$3(12i_1) = 24i_1 - 6i_2$$
$$36i_1 - 24i_1 = -6i_2$$

or
$$i_1 = \frac{-6}{12}i_2 \quad \text{...(iii)}$$

∴ From equation (ii) and (iii)

$$V_{ab} = 18i_2 - 30\left(\frac{1}{2}\right)i_2 = (18 - 15)i_2$$
$$V_{ab} = 3i_2$$

or
$$\frac{V_{ab}}{i_2} = 3\ \Omega$$

17. (a)

From the given characteristics, it is clear that,

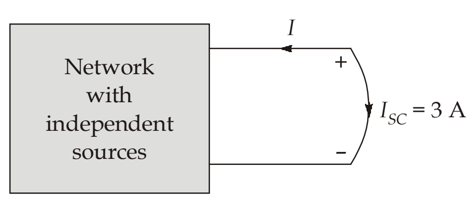
when $V = 0$ V (short circuit)

$I = -3$ A

and when $V = 15$ V

$I = 0$ A (open circuit)

∴ Network becomes,



$$V_{OC} = 15\text{ V}$$
$$I_{SC} = -I = 3\text{ A}$$

∴
$$R_{Th} = \frac{15}{3} = 5\ \Omega$$

and maximum power transferred is

$$P_{max} = \frac{V_{OC}^2}{4R_{Th}} = \frac{(15)^2}{4 \times 5} = \frac{15 \times 15}{20}$$
$$= \frac{45}{4} = 11.25\text{ W}$$

18. (a)

Here
$$Z_L = j\omega L = j \times 1000 \times 10^{-3} = j$$

and
$$Z_C = \frac{1}{j\omega C} = \frac{-j}{1000 \times 10^{-3}} = -j$$

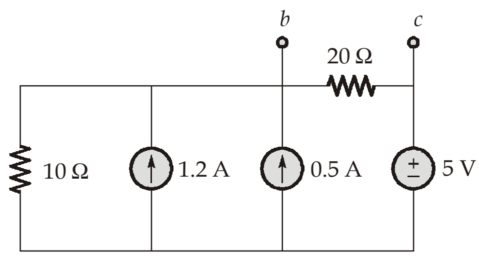
$$\therefore \quad Z_{eq} = 1 + (Z_L \,||\, Z_C)$$

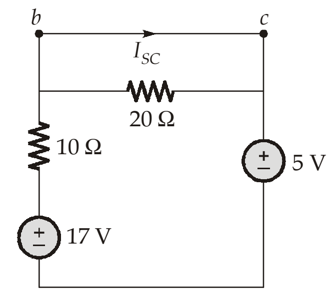
$$= 1 + \frac{(j)(-j)}{-j+j} = 1 + \frac{1}{0} = \infty$$

$$\therefore \quad I = 0$$

19. (d)

In order to obtain Norton's equivalent across the terminals 'b' and 'c' the circuit can be redrawn as

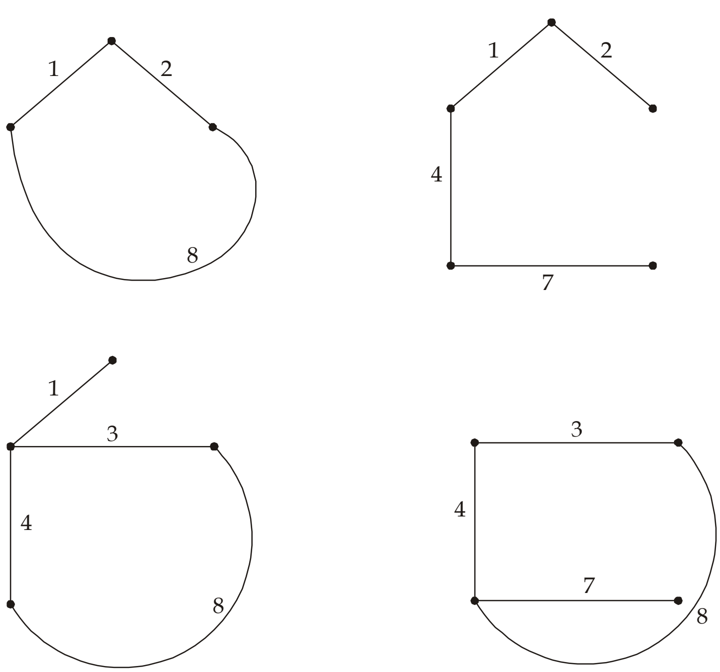




$$\therefore \quad I_{SC} = \frac{17-5}{10} = 1.2 \text{ A}$$

and $$R_{Th} = \frac{10 \times 20}{20+10} = 6.67\ \Omega$$

20. (b)

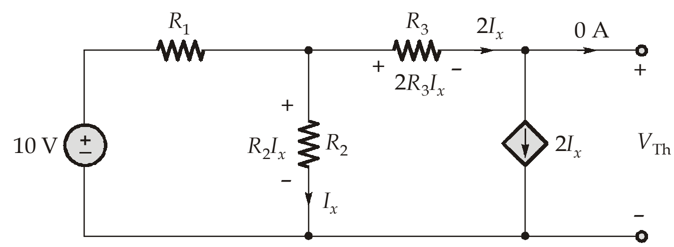


22. (b)

The reciprocity theorem is not applicable to the circuits with time varying elements.

23. (d)

Considering the given circuit,



$$V_{Th} = -2R_3I_x + R_2I_x = (R_2 - 2R_3)I_x$$

V_{Th} will be equal to zero, when $R_2 = 2R_3$.

In option (a) $\Rightarrow$ $R_2 = 15\ \Omega$ and $R_3 = 30\ \Omega$ $\Rightarrow$ $R_2 \neq 2R_3$

In option (b) $\Rightarrow$ $R_2 = 15\ \Omega$ and $R_3 = 10\ \Omega$ $\Rightarrow$ $R_2 \neq 2R_3$

In option (c) $\Rightarrow$ $R_2 = 20\ \Omega$ and $R_3 = 40\ \Omega$ $\Rightarrow$ $R_2 \neq 2R_3$

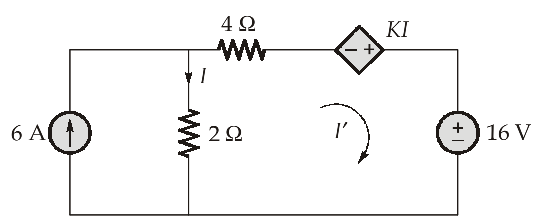
In option (d) $\Rightarrow$ $R_2 = 20\ \Omega$ and $R_3 = 10\ \Omega$ $\Rightarrow$ $R_2 = 2R_3$

So, option (d) is correct.

25. (b)

Here, the 8 Ω resistance in parallel with the 16 V source can be ignored.

$\therefore$ the circuit can be redrawn as



By KVL in the outer loop, we get,

$$4I' - KI + 16 + 2(I' - 6) = 0$$

or $$I' = \frac{KI - 4}{6} \quad \text{...(i)}$$

Also, $$I = 6 - I' = 6 - \left(\frac{KI - 4}{6}\right) = \frac{40 - KI}{6}$$

or $$I = \frac{40}{6 + K} \quad \text{...(ii)}$$

$\because$ The power dissipated in the 2 Ω resistor is 50 W.

$\therefore$ $$P_{2\Omega} = I^2 \times 2$$

$$50 = \left(\frac{40}{6 + K}\right)^2 \times 2$$

$$\frac{40}{6 + K} = \sqrt{25} = 5$$

or $$40 = 30 + 5\text{ K}$$

or $$K = 2$$

26. (d)

For maximum power transfer

$$Z_L = Z_s^* = (R_s + jX_s)^* = R_s - jX_s$$

$$I = \frac{V_m\angle 0°}{Z_s + Z_L} = \frac{V_m}{2R_s}$$

∴ Average power, $$P_{avg} = \frac{1}{2}I^2R = \frac{1}{2}\frac{V_m^2}{(2R_s)^2}\times R_s = \frac{V_m^2}{8R_s}$$

27. (a)

Here $v_0(t)$ is negative means current direction is opposite in the coils

∴ $$v_0(t) = \frac{M\,di_1(t)}{dt}$$

$$M = \frac{|v_0(t)|}{\left|\frac{di_1(t)}{dt}\right|} = \frac{40}{16} = 2.5\text{ H}$$

28. (b)

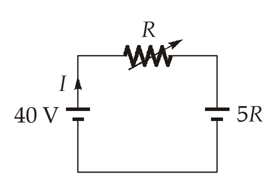
For a symmetrical two port network,

$$z_{11} = z_{22}$$
$$y_{11} = y_{22}$$
$$\Delta h = 1$$

and $$A = D$$

29. (b)

The circuit can be redrawn as,



When $I = 0$, $$40\text{ V} = 5R$$
$$R = 8\ \Omega$$

30. (b)

At $t = 0^-$ when switch was closed.

The voltage across the capacitor is

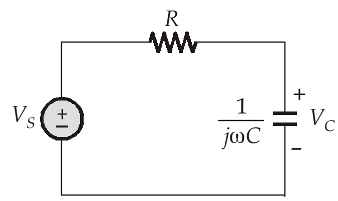
$$v(0^-) = \frac{10\times 2}{5} = 4\text{ V}$$

∵ Capacitor does not allow the sudden changes in the voltage across it.

∴ $$v(0^-) = v(0^+) = 4\text{ V}$$

31. **(b)**

For a series RC circuit,



Here, $$V_C = \frac{V_S}{R+\frac{1}{j\omega C}}\left(\frac{1}{j\omega C}\right) = \frac{V_S}{j\omega RC+1}$$

Phase difference between V_S and V_C,

$$\phi = \tan^{-1}\omega RC$$

As $\omega\uparrow \phi\uparrow$; $R\uparrow \phi\uparrow$; $C\uparrow \phi\uparrow$

As $\omega\downarrow \phi\downarrow$

32. **(b)**

The time constant for RC circuit is

$$\tau = R_{eq}\,C_{eq}$$

here, $$R_{eq} = 2\ \Omega$$

and $$C_{eq} = \frac{(4\text{ F}+4\text{ F})(8\text{ F})}{(4\text{ F}+4\text{ F})+8\text{F}} = \frac{8\text{ F}\times 8\text{ F}}{16\text{ F}} = 4\text{ F}$$

$\therefore$ $$\tau = 2\times 4 = 8\text{ sec}$$

33. **(c)**

$$H(s) = \frac{V_0(s)}{I(s)} = \frac{(s+1)}{(5s+8)(3s+2)}$$

$\because$ $$i(t) = 4u(t) \Rightarrow I(s) = 4/s$$

$\therefore$ $$V_0(s) = \frac{(s+1)}{(5s+8)(3s+2)}\times 4/s$$

$\therefore$ Final value, $$\lim_{s\to 0} sV_0(s) = \lim_{s\to 0}\frac{(s+1)}{(5s+8)(3s+2)}\times 4$$

$$= \frac{1}{8\times 2}\times 4 = \frac{4}{16} = \frac{1}{4} = 0.25$$

34. **(b)**

From h-parameter model,

$$V_1 = h_{11}I_1 + h_{12}V_2 \quad \text{...(i)}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \quad \text{...(ii)}$$

From transmission parameter model,

$$V_1 = AV_2 - BI_2 \quad \text{...(iii)}$$

$$I_1 = CV_2 - DI_2 \quad \text{...(iv)}$$

where, $$B = \left.\frac{-V_1}{I_2}\right|_{V_2 = 0}$$

$\therefore$ From equation (i) and (ii), keeping $V_2 = 0$, we get,

$$B = \frac{-h_{11}}{h_{21}}$$

35. (d)

Power efficiency of the source can be more than 50%. But power efficiency will be 50% when maximum power is being delivered to R_L.

36. (d)

Power factor in any circuit is given by cos ϕ where ϕ is the angle between voltage and current in the circuit.

$\because$ The voltage across and current through the capacitor are in phase quadrature.

$\therefore$ $$\phi = 90°$$

and $$\cos 90° = 0 \quad \text{(Power factor)}$$

38. (c)

Any combination and interconnection of network elements like resistor, capacitor, inductor or electrical energy sources are known as networks, however a closed energized network is known as a circuit. A network need not contain energy source but a circuit must contain energy source.

Section B : Digital Circuits

39. (c)

$$f(x_1\, x_2\, x_3) = \Pi M(0, 1, 5)$$

$x_1 \backslash x_2 x_3$	00	01	11	10
0	0	0	1	1
1	1	0	1	1

$$f(x_1\, x_2\, x_3) = x_2 + x_1\bar{x}_3$$

40. (d)

$$f = \bar{x}_1\bar{x}_2 I_0 + \bar{x}_1 x_2 I_1 + x_1\bar{x}_2 I_2 + x_1 x_2 I_3$$

$$= \bar{x}_1\bar{x}_2 x_3 + \bar{x}_1 x_2 \bar{x}_3 + x_1\bar{x}_2\bar{x}_3 + x_1 x_2 x_3$$

$$= (x_1 \odot x_2)x_3 + (x_1 \oplus x_2)\bar{x}_3$$

$$= x_1 \oplus x_2 \oplus x_3$$

41. (d)

For $S = 1$, $f = (A + B) \Rightarrow$ OR gate
for $S = 0$, $f = \bar{B}$ $\Rightarrow$ NOT gate

42. (b)

For minimum value of 'y' the value of 'x' should be minimum

$\therefore$ minimum value of x = 4

$\therefore$ $(23)_4 + (21)_4 = (110)_4 = (4^2 + 4 + 0)_{10} = (20)_{10}$

43. (b)

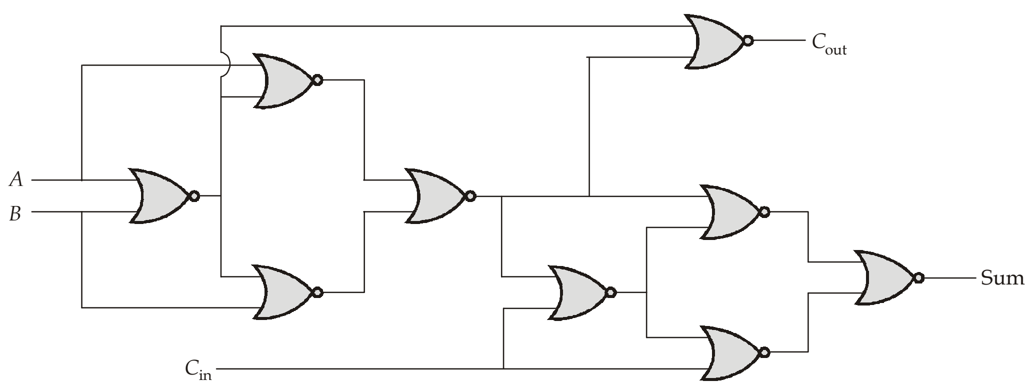
$$f = (x\bar{y} + \bar{x}\,\bar{y}) \oplus x = \bar{y} \oplus x$$
$$= \bar{x}\,\bar{y} + xy = x \odot y$$

44. (a)

$$Q^+ = Q \oplus X = Q\bar{X} + \bar{Q}X$$

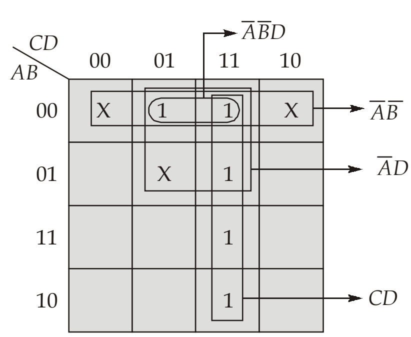
Hence, it represents a T-flip-flop.

45. (b)



So, minimum 9 two-input NOR gates are required to design a full-adder circuit.

46. (d)



Therefore, the simplified expressions can be given as:

$$f(A,B,C,D) = \bar{A}\bar{B} + CD$$
$$= \bar{A}D + CD = \bar{A}\bar{B}D + CD$$

47. (c)

$$F(ABCD) = \bar{A}+\bar{B}+\bar{A}\bar{C}\bar{D}+\bar{A}\bar{B}C+\bar{A}C\bar{D}+\bar{B}C\bar{D}$$
$$= \bar{A}(1+\bar{C}\bar{D}+\bar{B}C+C\bar{D})+\bar{B}(1+C\bar{D}) = \bar{A}+\bar{B} = \overline{AB}$$

thus, only one two-input NAND gate is required.

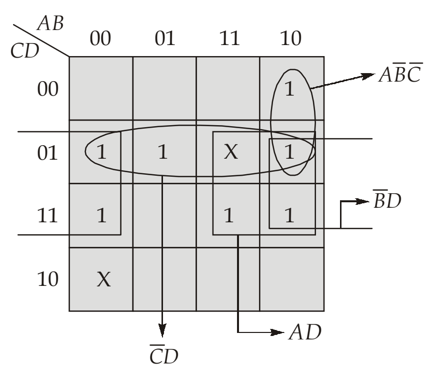
49. (b)

$$D = \bar{B}Q_n + A$$

which is equal to the excitation equation of a SR-flip flop

$$D = \bar{R}Q_n + S$$

50. (c)



$$f(A, B, C, D) = \bar{C}D + AD + \bar{B}D + A\bar{B}\bar{C}$$

51. (d)

$$f(w, x, y, z) = \Sigma m(4, 5, 7, 8, 10, 12, 15)$$

wx	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$	
00	0	0	0	0	$I_0 = 0$
01	1	1	1	0	$I_1 = \bar{y} + z$
11	1	0	1	0	$I_3 = y \odot z$
10	1	0	0	1	$I_2 = \bar{z}$

∴ $$I_1(B) = \bar{y} + z$$
$$I_3(A) = y \odot z$$

52. (b)

Q_A	Q_B	T_A $(Q_A + Q_B)$	T_B $(\bar{Q}_A + Q_B)$	Q_A^+	Q_B^+
0	0	0	1	0	1
0	1	1	1	1	0
1	0	1	0	0	0
0	0	0	1	0	1

Thus, MOD = 3

53. (c)

$$f_i = 2 \text{ kHz}$$
$$f_0 = 256 \text{ kHz}$$
$$\therefore \quad \text{MOD} = \frac{256}{2} = 128$$
$$\therefore \quad n = \lceil \log_2(\text{MOD}) \rceil = 7$$

54. (c)

$$f_{out} = I_0 + I_1 + I_3 + I_6 + I_7$$
$$f_{out} = \bar{C}\,\bar{B}\,\bar{A} + \bar{C}\,\bar{B}A + \bar{C}\,B\,A + CB\bar{A} + CBA$$
$$= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + \bar{A}BC + ABC$$
$$f_{out}(A, B, C) = \Sigma m(0, 4, 6, 3, 7) = \Sigma m(0, 3, 4, 6, 7)$$

55. (c)

$$Z = 1 \text{ thus } A > B$$
$$X = 1 \text{ thus } A = B$$

but if $X = 0$ and $Z = 0$, then $Y = 1$, and hence $A < B$.

56. (c)

$$\text{Total states} = 14$$
$$\therefore \quad f_{out} = \frac{50 \times 10^3}{14} = 3.57 \text{ kHz}$$

58. (d)

$$2r + 3 + 4r + 4 + r + 4 + 3r + 2 = 2r^2 + 2r + 3$$
$$10r + 13 = 2r^2 + 2r + 3$$
$$2r^2 - 8r - 10 = 0$$
$$r^2 - 4r - 5 = 0$$
$$r = 5, -1$$

$\because$ Radix cannot be negative

$$\therefore \quad r = 5$$

59. (b)

3-bit gray code is

000
001
011
010
110
111 ⇒ Two clock cycles are required (110 → 101)
101
100

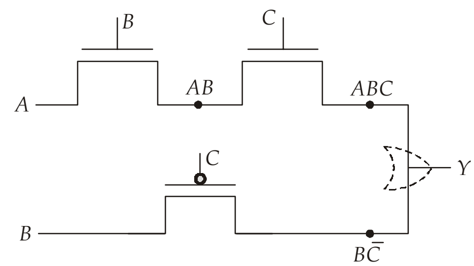
60. **(d)**

The circuit will combine two 4-bit *ADC* and will result in an 8-bit *ADC* circuit. It is used to reduced number of comparator in the circuit.

61. **(c)**

AB \ CD	00	01	11	10
00	1		1	
01		1		1
11	1		1	
10		1		1

62. **(b)**



$$Y = ABC + B\bar{C} \qquad [\because \text{ The nodes acts as wired OR logic}]$$
$$= B(AC + \bar{C}) = B(A + \bar{C})$$

63. **(a)**

$$F(A, B, C\ ...) = A + \bar{A}B(1 + C + \bar{C}D + \bar{C}\bar{D}E + ...)$$
$$= A + \bar{A}B$$
$$= A + B \quad \Rightarrow \quad \text{two NOR gates are required.}$$

65. **(b)**

Min decimal base $\Rightarrow$ $x = 7$

$\therefore$ $(216)_7 = 2 \times 7^2 + 7 + 6$

$= 2 \times 49 + 7 + 6 = 98 + 7 + 6 = (111)_{10}$

66. **(c)**

The decimal equivalent of number 44 can be represented as

$$(44)_{10} = (00101100)_2$$

Now, 2's complement representation of $(-44)_{10} = (11010100)_2$

67. **(a)**

A \ BC	00	01	11	10
0	0	0	1	1
1	0	0	1	1

F_1

A \ BC	00	01	11	10
0	0	1	0	1
1	0	1	0	1

F_2

∴ $F_1 \times F_2 =$

A \ BC	00	01	11	10
0	0	0	0	1
1	0	0	0	1

∴ $F_1 F_2 = B\bar{C}$

68. (c)

$$F(A, B, C) = \bar{A}C + \bar{B}$$

The following function can be represented on a K-map as

A \ BC	00	01	11	10
0	1	1	1	0
1	1	1	0	0

To calculate the maxterms we just have to see the position of zeros.

∴ $F(A, B, C) = \Pi M(2, 6, 7)$

70. (d)

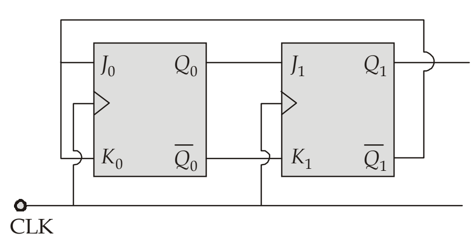
$$F = \left(\overline{A\bar{B} + \bar{A}B + C}\right)\left(\bar{C} + A\bar{B} + \bar{A}B\right)$$

$$= \overline{A\bar{B} + \bar{A}B} \cdot \bar{C} + (A\bar{B} + \bar{A}B) \cdot C$$

$$= (\bar{A}\bar{B} + AB)\bar{C} + A\bar{B}C + \bar{A}BC$$

$$= \bar{A}\bar{B}\bar{C} + AB\bar{C} + A\bar{B}C + \bar{A}BC$$

71. (b)



J_1	K_1	J_0	K_0	$Q_1(t+1)$	$Q_0(t+1)$	
Q_0	$\bar{Q}_0$	$\bar{Q}_1$	$\bar{Q}_1$	0	0	
0	1	1	1	0	1	3 stable state
1	0	1	1	1	0	
0	1	0	0	0	0	→ Repeat

Hence, the circuit is a mod-3 counter.

72. (d)

ROM is an example of a combinational circuit.

73. (d)

The time required for addition in a parallel adder does not depends upon the number of input bits.

74. (c)

In TDM, MUX can be used at transmitting end and DeMUX can be used at receiving end.

❍❍❍❍