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ESE 2027 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 2

Section A : Network Theory

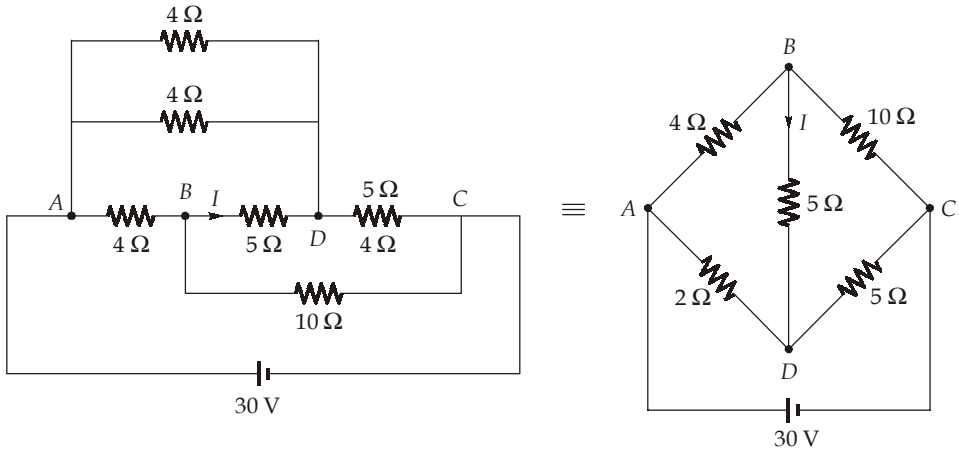
Section B : Digital Circuits

1.	(a)	**16.**	(c)	**31.**	(b)	**46.**	(c)	**61.**	(c)
2.	(b)	**17.**	(c)	**32.**	(a)	**47.**	(a)	**62.**	(b)
3.	(c)	**18.**	(a)	**33.**	(b)	**48.**	(b)	**63.**	(c)
4.	(b)	**19.**	(a)	**34.**	(a)	**49.**	(d)	**64.**	(b)
5.	(b)	**20.**	(a)	**35.**	(a)	**50.**	(c)	**65.**	(d)
6.	(a)	**21.**	(a)	**36.**	(c)	**51.**	(a)	**66.**	(b)
7.	(a)	**22.**	(d)	**37.**	(c)	**52.**	(a)	**67.**	(d)
8.	(d)	**23.**	(a)	**38.**	(c)	**53.**	(c)	**68.**	(d)
9.	(a)	**24.**	(a)	**39.**	(c)	**54.**	(a)	**69.**	(c)
10.	(d)	**25.**	(c)	**40.**	(b)	**55.**	(c)	**70.**	(b)
11.	(c)	**26.**	(a)	**41.**	(b)	**56.**	(d)	**71.**	(b)
12.	(c)	**27.**	(a)	**42.**	(b)	**57.**	(b)	**72.**	(c)
13.	(c)	**28.**	(a)	**43.**	(b)	**58.**	(c)	**73.**	(d)
14.	(a)	**29.**	(a)	**44.**	(b)	**59.**	(c)	**74.**	(b)
15.	(c)	**30.**	(a)	**45.**	(a)	**60.**	(d)	**75.**	(d)

Section A : Network Theory

1. (a)

Given circuit can be rearranged as,



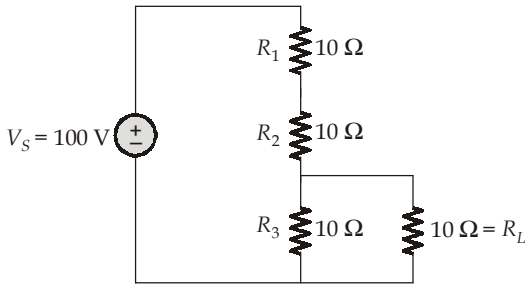
Since the above circuit is a balanced Wheatstone bridge as,

$$Z_{AD}\, Z_{BC} = Z_{AB}\, Z_{DC}$$

$\therefore$ $$I = 0 \text{ A}$$

2. (b)

Given circuit is,

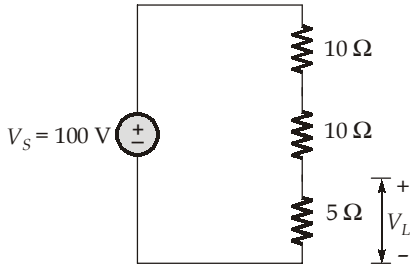


R_3 and R_L is in parallel.

Equivalent resistance of parallel combination,

$$10 \parallel 10 = 5\ \Omega$$

The simplified circuit can be drawn as below:

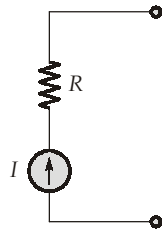


Using voltage division rule,

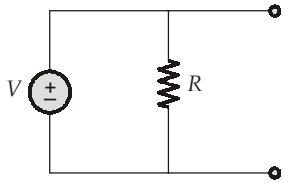
$$V_L = \frac{V_s \times 5}{10+10+5} = \left(\frac{5}{5+10+10}\right) \times 100 = \frac{5}{25} \times 100$$

$\therefore$ $V_L = 20$ V

3. (c)



Here, the current is fixed by the current source, irrespective of the series element. Thus, R is redundant if we find current through load.



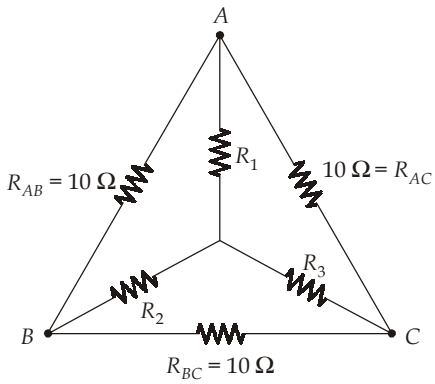
Here, the voltage across the parallel element is fixed by the ideal voltage source, so it does not affect the voltage of the rest of the circuit. Thus, R becomes redundant if we find voltage through load.

4. (b)

Electromotive force is the energy supplied by a source per unit charge that causes current to flow through a circuit. It can also be defined as the open-circuit potential difference between the terminals of a source and is measured in volts (V).

5. (b)

Converting the given Delta network into Star network,



$$R_1 = \frac{R_{AB} \cdot R_{AC}}{R_{AB} + R_{AC} + R_{BC}}$$

$$R_1 = \frac{10 \times 10}{10+10+10} = \frac{100}{30} = 3.33\ \Omega$$

$$R_2 = \frac{R_{AB}.R_{BC}}{R_{AB}+R_{AC}+R_{BC}} = \frac{10\times10}{30} = 3.33\Omega$$

$$R_3 = \frac{R_{AC}.R_{BC}}{R_{AB}+R_{AC}+R_{BC}} = \frac{10\times10}{10+10+10} = \frac{100}{30} = \frac{10}{3} = 3.33\ \Omega$$

6. (a)

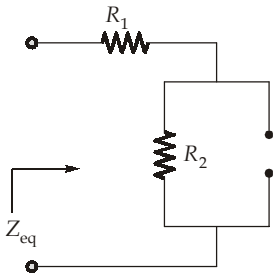
For two rated loads in series across a supply equal to their rated voltage:
We directly calculate the power consumption as,

$$P_T = \frac{P_{1\text{rated}} \cdot P_{2\text{rated}}}{P_{1\text{rated}} + P_{2\text{rated}}} = \frac{40\times60}{40+60} = \frac{2400}{100} = 24\ \text{W}$$

Alternatively, we can calculate the resistance of load using the given rated voltage and power; find the equivalent resistance of the series combination and calculate the total power consumed using $P = V^2/R_{eq}$.

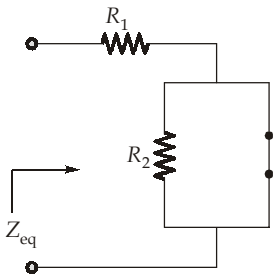
7. (a)

For $\omega = 0$, $X_C = \infty$ i.e. the capacitor acts as open circuit and $Z_{eq} = 10\ \Omega$ (from the plot)



$\therefore \quad Z_{eq} = R_1 + R_2 = 10\ \Omega$

Put $\omega = \infty$, $X_C = 0$ i.e. the capacitor acts as short circuit, and $Z_{eq} = 4\ \Omega$ (from the plot)



$\therefore \quad Z_{eq} = R_1$

$R_1 = 4\ \Omega$

We have, $R_1 + R_2 = 10\ \Omega$

$\therefore \quad R_2 = 6\ \Omega$

8. (d)

Given quality factor $Q = 1000$ and center frequency $\omega_0 = 10^6$ rad/sec.

For series RLC circuit, $Q = \frac{\omega_0 L}{R}$, $\omega_0 = \frac{1}{\sqrt{LC}}$

$\therefore$ $$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

$\Rightarrow$ For option (d): $$Q = \frac{1}{0.001}\sqrt{\frac{1\ \mu H}{1\ \mu F}} = 1000$$

So, $L = 1\ \mu H$, $C = 1\ \mu F$ and $R = 0.001\ \Omega$.

9. (a)

Given currents are,

$$i_1 = -4\sin(377t + 25°) = 4\cos(377t + 25° + 90°)$$
$$i_1 = 4\cos(377t + 115°) = 4 \angle 115°A$$
$$i_2 = 5\cos(377t - 40°) = 5 \angle -40°A$$

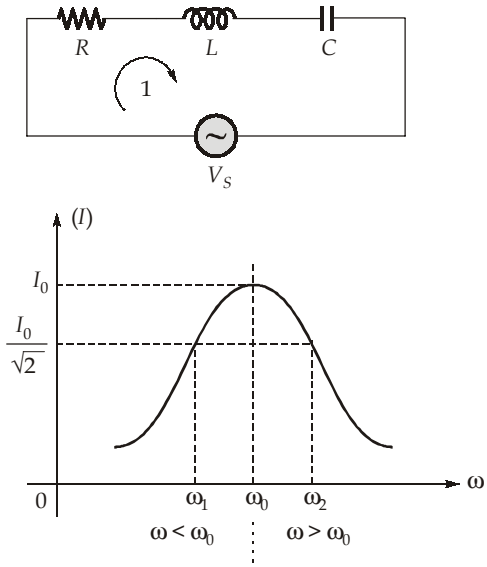
$\therefore$ Phase angle between i_1 and i_2 is,

$$\phi = 115° - (-40°) = 155°$$

Here, i_2 lags i_1 by 155°.

10. (d)

For series R-L-C circuit,



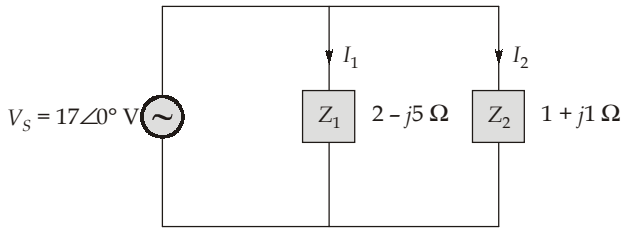
1. For $\omega < \omega_0$, $X_C > X_L$, thus series RLC circuit behave like an RC circuit
2. For $\omega > \omega_0$, $X_C < X_L$, thus series RLC circuit behave like an RL circuit
3. For $\omega = \omega_0$, $X_L = X_C$ and hence, $Z = R + j(X_L - X_C) = R$. Thus, series RLC circuit behave like resistive circuit.
4. At resonance $X_L = X_C$;

$$Z_{min} = R,$$
$$I_{max} = \frac{V}{Z_{min}}$$

Hence, current is maximum at $\omega = \omega_0$.

11. (c)

Given Z_1 and Z_2 are in parallel with voltage source, the circuit can be drawn as below:



$$Z_1 = \left(\sqrt{2^2+5^2}\right)\angle \tan^{-1}\left(\frac{-5}{2}\right) = 5.385\angle -68.20°\ \Omega$$

Thus, $$I_1 = \frac{V_s}{Z_1} = \frac{17\angle 0°}{5.385\angle -68.20°} = 3.16\angle 68.2°\text{A}$$

Similarly, $$Z_2 = 1 + j1 = \sqrt{2}\angle 45°\ \Omega$$

$$I_2 = \frac{V_s}{Z_2} = \frac{17\angle 0°}{\sqrt{2}\angle 45^\circ} = 12.02\angle -45°\text{A}$$

$$I_2 = 12.02\ \angle -45°\text{A}$$

12. (c)

$$\text{Power factor} = \cos\theta = \frac{R}{Z}$$

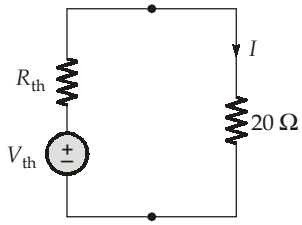
For RC circuit we have leading power factor.

13. (c)

1. The superposition theorem is not applicable to power since it is a non linear parameter
2. The superposition theorem is also applicable for the circuit having initial condition.
3. The superposition theorem is not applicable to the network containing.
   (a) Non linear elements.
   (b) Unilateral elements such as diode or BJT.

14. (a)

Using Millman's theorem, the equivalent circuit can be drawn as below:



$$R_{th} = \frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4}} = \frac{1}{G_1+G_2+G_3+G_4}$$

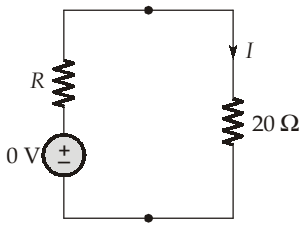
$$V_{th} = \frac{V_1G_1 + V_2G_2 + V_3G_3 + V_4G_4}{G_1+G_2+G_3+G_4}$$

$$V_{th} = \frac{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}+\frac{V_4}{R_4}}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4}}$$

$$= \frac{\frac{200}{50}+\frac{160}{40}-\frac{100}{25}-\frac{80}{20}}{\frac{1}{50}+\frac{1}{40}+\frac{1}{25}+\frac{1}{20}}$$

$$= \frac{4+4-4-4}{\frac{1}{50}+\frac{1}{40}+\frac{1}{25}+\frac{1}{20}} = 0$$

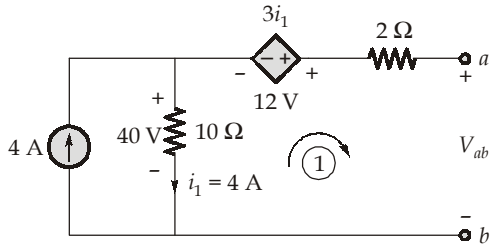
$\therefore$ $V_{th} = 0$



$\therefore$ $I = \frac{0}{R+20} = 0$ A

15. (c)

For Thevenin voltage,



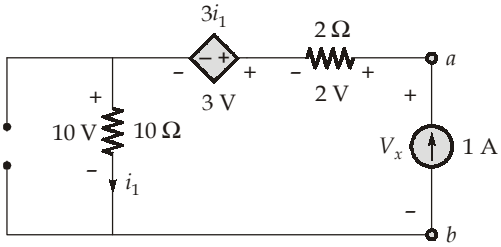
Applying KVL, we get

$$-40 - 12 + V_{ab} = 0$$

$$V_{ab} = 52 \text{ V}$$

For Thevenin Resistance,

Current source is considered as open circuit, and a 1 A current source is connected across the terminals *a*-*b*:



$$V_x = 2 + 3 + 10 = 15 \text{ V}$$

$$R_{th} = \frac{V_x}{1 \text{ A}} = \frac{15}{1}$$

$$R_{\text{th}} = 15 \ \Omega$$

16. (c)

For maximum power transfer, $Z_L = Z_S^*$

Given, $Z_L = 4 + 3j \ \Omega$

$\therefore$ The source impedance must be

$$Z_S = 4 - 3j \ \Omega$$

17. (c)

Reciprocity theorem is applicable to the networks comprising of linear, time-invariant, bilateral, passive elements, such as resistors, inductors and capacitors with one independent source. It states that the ratio of excitation (source) to response remains constant when the positions of the excitation and response are interchanged.

18. (a)

- Voltage sources dual is current sources.
- Resistance dual is conductance.
- Inductor dual is capacitor.
- Capacitor dual is inductor.
- Series connection dual is parallel connection and vice-versa.

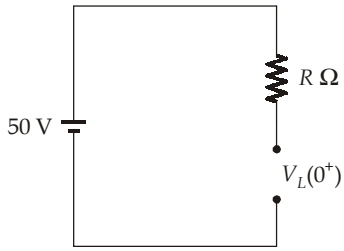
19. (a)

For a DC source, an uncharged inductor [$I(0^-) = 0$] will act as an open circuit at $t = 0$ as the inductor does not allow sudden change in current, whereas it will act as a short circuit at steady state.

20. (a)

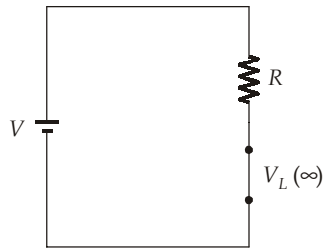
Given inductor is initially uncharged. Since the inductor does not allow sudden change in current,

at $(t = 0^-)$	$(t = 0^+)$
$i_L(0^-) = 0$	$i_L(0^+) = 0$ A



$$V_L(0^+) = 50 \text{ V}$$

At $t = \infty$, the inductor is replaced by a short circuit



$$V_L(\infty) = 0$$

$$\therefore \quad V(t) = [V_L(0^+) - V_L(\infty)]e^{-\frac{t}{\tau}} + V_L(\infty)$$

where $\tau = \dfrac{L}{R}$

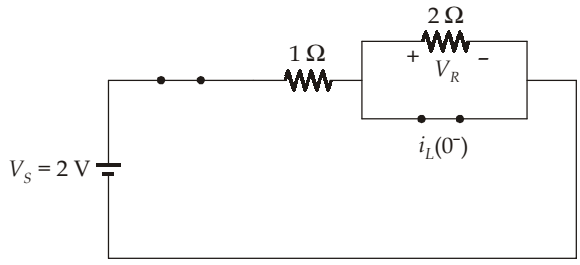
$$V(t) = [50]e^{-\frac{R}{L}t}$$

Given: $R = 10\ \Omega,\ L = 10\ \text{H}$

$$\therefore \quad V(t) = 50e^{-t}\ \text{V}$$

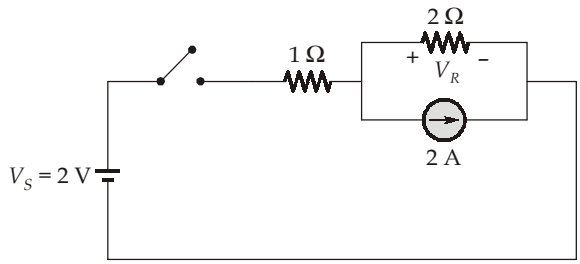
21. (a)

At $t = 0^-$, switch is closed for a long time, hence the circuit is in steady state and thus, the inductor acts as short circuit.



$$i_L(0^-) = \frac{2}{1} = 2\ \text{A}$$

At $t = 0^+$, the switch is open and since inductor does not allow sudden change in current $i_L(0^-) = i_L(0^+) = 2$ A, hence the circuit becomes:



$$\therefore \quad V_R = -2 \times 2 = -4\ \text{V}$$

Magnitude of the voltage,

$$|V_R| = 4\ \text{V}$$

22. (d)

At $t = 0^-$ switch is open,

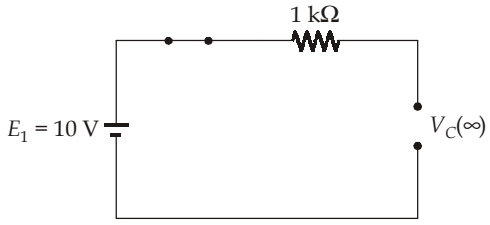
$$V_C(0^-) = 0$$

At $t = 0^+$ switch is closed,

$$V_C(0^-) = V_C(0^+) = 0 \text{ V}$$

For $0 < t < 5$ ms:

At steady state, the capacitor acts as open circuit, hence the circuit can be drawn as,



$$V_C(\infty) = 10 \text{ V}$$

For $0 < t < 5$ ms:
$$V_C(t) = [V_C(0^+) - V_C(\infty)]e^{-\frac{t}{RC}} + V_C(\infty)$$

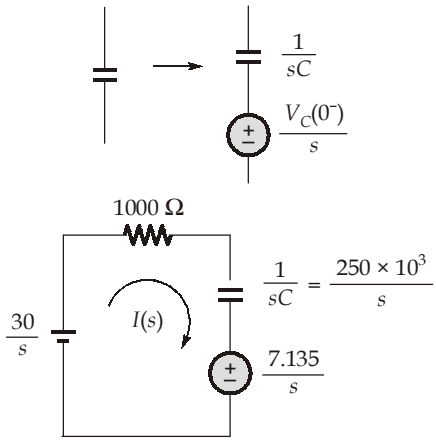
where,
$$\tau = RC = 10^3 \times 4 \times 10^{-6} = 0.004 \text{ sec}$$

$\therefore$
$$V_C(t) = 10 - 10e^{-\frac{t}{0.004}} \text{ V}$$

At $t = 5$ msec,

$$V_C(t) = 10(1 - e^{-250\times5\times10^{-3}}) = 7.135 \text{ V}$$

For $t > 5$ msec, switch is at position B: Replace the circuit in s-domain with initial capacitor voltage present.



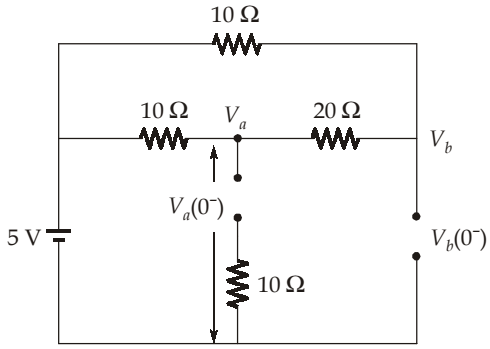
$$I(s) = \frac{\frac{30}{s} - \frac{7.135}{s}}{1000 + \frac{250\times10^3}{s}} = \frac{\frac{22.865}{s}}{\frac{1000(s+250)}{s}} = \frac{22.865\times10^{-3}}{s+250}$$

Taking the inverse Laplace transform:

$$i(t) = 22.865\ e^{-250t}\ u(t) \text{ mA}$$

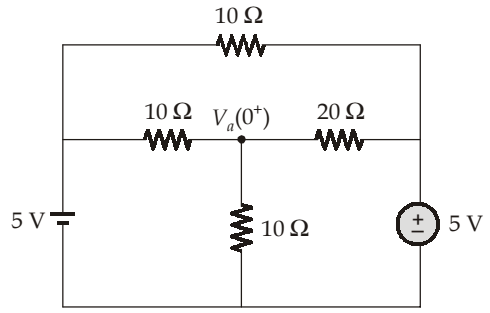
23. (a)

At $t = 0^-$, switch is open for long time. Thus, at steady state, capacitor is replaced by an open circuit.



$$V_b(0^-) = 5 \text{ V}$$
$$V_a(0^-) = 5 \text{ V}$$

The capacitor doesn't allow sudden change in voltage. Thus, when the switch is closed at $t = 0^+$, $V_b(0^-) = V_b(0^+) = 5$ V. At $t = 0^+$, the circuit can be drawn as below:



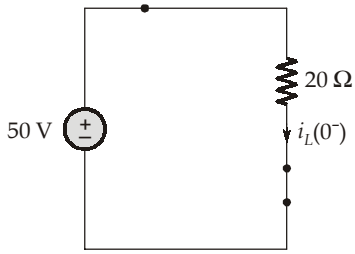
Applying KCL at node a,

$$\frac{V_a(0^+)-5}{10}+\frac{V_a(0^+)}{10}+\frac{V_a(0^+)-5}{20}=0$$

$$2V_a(0^+) - 10 + 2V_a(0^+) + V_a(0^+) - 5 = 0$$
$$5V_a(0^+) = 15$$
$$V_a(0^+) = 3 \text{ V}$$

24. (a)

At $t = 0^-$, the switch is at position 1, and the circuit is in the steady state condition. Thus, the inductor is replaced by a short circuit.

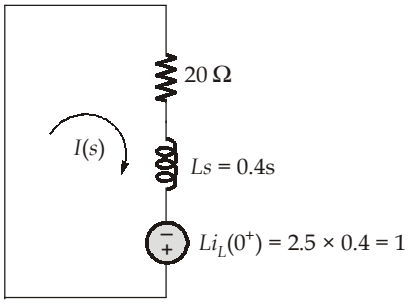


$$i_L(0^-) = \frac{50}{20} = 2.5 \text{ A}$$

Inductor doesn't allow a sudden change of current, thus

$$i_L(0^-) = i_L(0^+) = 2.5 \text{ A}$$

For $t > 0$, redrawing the circuit in s-domain,



$$\therefore \quad I(s) = \frac{1}{20 + 0.4s} = \frac{1}{0.4(s+50)} = \frac{2.5}{s+50}$$

Taking the inverse Laplace transform,

$$i(t) = 2.5\, e^{-50t}\, u(t) \text{ A}$$

25. (c)

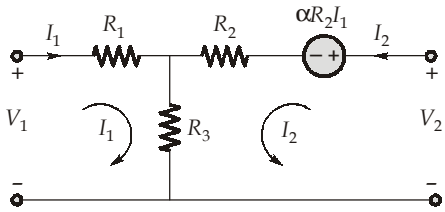
For $ABCD$ parameters, the condition of reciprocity is given by,

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = 1$$

$$\therefore \quad AD - BC = 1$$

26. (a)

Let the loop currents are I_1 and I_2,



Standard equations for z-parameters:

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

By using KVL in loop (1),

$$V_1 = (R_1 + R_3)\, I_1 + R_3 I_2 \qquad \ldots(1)$$

By using KVL in loop (2),

$$-V_2 + \alpha R_2 I_1 + (R_2 + R_3) I_2 + R_3 I_1 = 0$$

$$V_2 = (R_3 + \alpha R_2)\, I_1 + (R_2 + R_3)\, I_2 \qquad \ldots(2)$$

Comparing eq.(1) and eq.(2) with standard equations, we get,

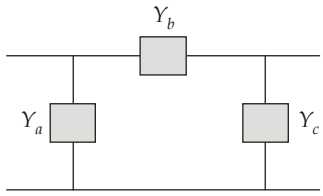
$$[Z] = \begin{bmatrix} R_1 + R_3 & R_3 \\ \alpha R_2 + R_3 & R_2 + R_3 \end{bmatrix}$$

27. (a)

Given, $Y_{11} = \frac{2}{100}\,\mho;\ Y_{12} = \frac{-1}{100}\,\mho;\ Y_{21} = \frac{-1}{100}\mho;\ Y_{22} = \frac{4}{300}\mho$

$$Y_{12} = Y_{21}$$

Reciprocity condition satisfy. Thus, the equivalent two-port network can be drawn as below:

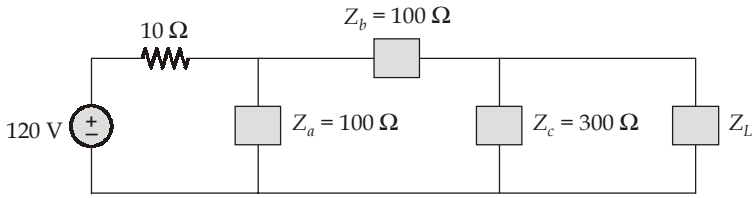


$$Y_a = Y_{11} + Y_{12} = \frac{1}{100}\,\mho$$

$$Y_b = -Y_{12} = \frac{1}{100}\,\mho$$

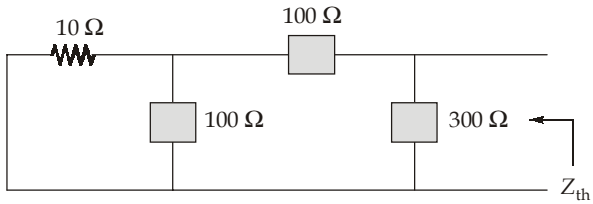
$$Y_c = Y_{22} + Y_{21} = \frac{1}{300}\,\mho$$

Thus, the overall circuit can be drawn as below:



For maximum power transfer, $Z_L = Z_{th}$.

To calculate Z_{th}, we short circuit the voltage source and disconnect the load Z_L as shown below:



$$Z_{th} = [(10\ \Omega \,||\, 100\ \Omega) + 100\ \Omega] \,||\, 300\ \Omega$$

$$Z_{th} = \left[\frac{100}{11} + 100\right] || \, 300$$

$$Z_{th} = \frac{\frac{1200}{11}\times 300}{\frac{1200}{11} + 300} = \frac{\frac{1200}{11}\times 300}{\frac{1200+3300}{11}} = \frac{1200\times 300}{4500}$$

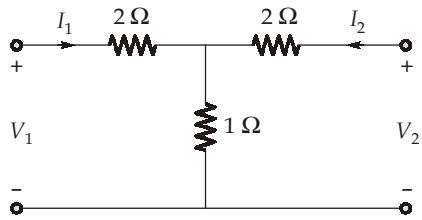
$$Z_L = Z_{th} = 80\ \Omega$$

28. (a)

Converting delta network to star network,

$$R_Y = \frac{R \times R}{R + R + R} = \frac{R}{3} = 1\,\Omega$$

Thus, the circuit can be drawn as below:



Standard $ABCD$ parameter equations:

$$V_1 = AV_2 - BI_2 \quad \text{...(1)}$$

$$I_1 = CV_2 - DI_2 \quad \text{...(2)}$$

Applying KVL in input loop, $V_1 = 3I_1 + I_2$ ...(i)

Applying KVL in output loop, $V_2 = I_1 + 3I_2$

$$I_1 = V_2 - 3I_2 \quad \text{...(a)}$$

Substituting equation (a) in equation (i),

We get,

$$V_1 = 3(V_2 - 3I_2) + I_2$$

$$V_1 = 3V_2 - 9I_2 + I_2$$

$$V_1 = 3V_2 - 8I_2 \quad \text{...(b)}$$

Comparing equation (a) by (2), we get

$$C = 1\,\mho,\ D = 3$$

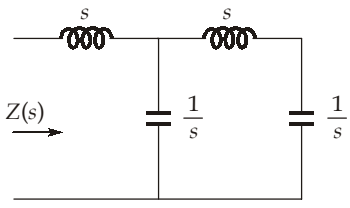
Comparing equation (b) by (1), we get

$$A = 3,\ B = 8\,\Omega$$

$$\therefore \quad \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 3 & 8\,\Omega \\ 1\,\mho & 3 \end{bmatrix}$$

29. (a)

Drawing the given circuit in s-domain,



$$Z(s) = s + \left[\frac{1}{s} \| \left(s + \frac{1}{s}\right)\right] = s + Z'(s)$$

where

$$Z'(s) = \frac{1}{s} \| \left(\frac{s^2+1}{s}\right) = \frac{\frac{1}{s} \times \frac{s^2+1}{s}}{\frac{1}{s} + \frac{s^2+1}{s}} = \frac{\frac{s^2+1}{s^2}}{\frac{s^2+2}{s}} = \frac{s^2+1}{s(s^2+2)}$$

Thus, $$Z(s) = s + \frac{s^2+1}{s^3+2s} = \frac{s^4+2s^2+s^2+1}{s^3+2s} = \frac{s^4+3s^2+1}{s^3+2s}$$

30. (a)

The transmission parameters are given by,

$$V_1 = AV_2 - BI_2; \quad I_1 = CV_2 - DI_2$$

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} = \text{open circuit reverse voltage gain}$$

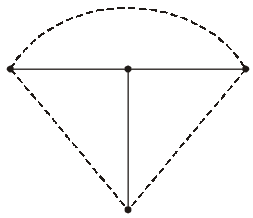
$$B = \left.-\frac{V_1}{I_2}\right|_{V_2=0} = \text{short circuit transfer impedance}$$

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = \text{open circuit transfer admittance}$$

$$D = \left.-\frac{I_1}{I_2}\right|_{V_2=0} = \text{short circuit reverse current gain}$$

ABCD parameters are most effectively used in transmission line.

31. (b)



- A tree contains all the nodes of the graph.
- A tree is connected graph and has no closed path.

Options (a) and (d) contain loops, whereas option (c) is not a connected graph. Hence, option (b) is a valid tree for the given network.

32. (a)

- The concept of duality strictly applies only to planar graphs, hence statement 1 is correct.
- In network duality, topological properties perfectly interchange. A closed loop or fundamental tie-set in the original planar network translates directly into a node, or fundamental cut-set in the dual network, hence statement 2 is correct.
- Every single branch in the original planar graph translates to exactly one respective branch in the dual graph. The total number of branches remains entirely identical across both graphs, hence statement 3 is incorrect.

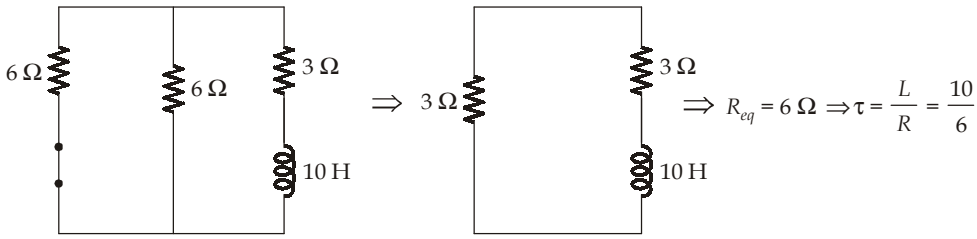
33. (b)

$$\text{Natural frequency} = \frac{1}{\text{Time constant}}$$

For R-L circuit, Time constant $\tau = \dfrac{L}{R_{eq}}$

$\therefore$ Natural frequency $= \dfrac{R_{eq}}{L}$, where R_{eq} is the equivalent resistance across inductance

To determine R_{eq}, we short circuit the ideal voltage source,



$\therefore$ Natural frequency 'f' $= \dfrac{6}{10} = 0.6$ Hz

34. (a)

If $[A]$ is the reduced incidence matrix and $[A^T]$ is the transposed matrix of $[A]$, then the number of possible trees of a graph is given by

$$N = \text{Determinant}[A A^T]$$

$$= \left| \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 1 & -1 & -1 \end{bmatrix}_{3\times 6} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 1 \\ 0 & 0 & -1 \\ 0 & -1 & -1 \end{bmatrix}_{6\times 3} \right|$$

$$= \begin{vmatrix} 2 & 0 & 1 \\ 0 & 2 & 1 \\ 1 & 1 & 4 \end{vmatrix}_{3\times 3}$$

$N = 2(8 - 1) - 0 + 1(0 - 2) = 14 - 2$

$N = 12$

35. (a)

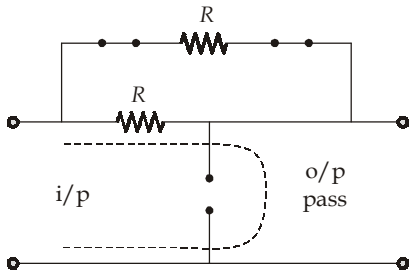
At $f = 0$,

- $X_L = 2\pi f L = 0$

  Inductor is replaced by a short circuit.

- $X_C = \dfrac{1}{2\pi f C} = \dfrac{1}{0} = \infty$

Capacitor is replaced by an open circuit.



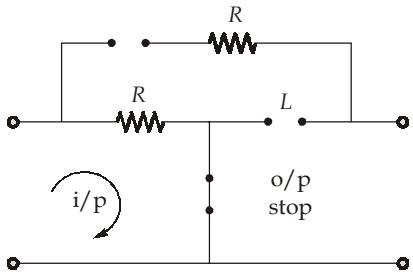
At $f = \infty$,

- $$X_L = 2\pi fL = \infty$$

Inductor is replaced by an open circuit.

- $$X_C = \frac{1}{2\pi fC} = 0$$

Capacitor is replaced by a short circuit.



Since low frequencies are passed by the circuit and high frequencies are attenuated/ blocked, the network acts as a Low pass filter.

36. (c)

- Below resonance, the inductive susceptance is greater than the capacitive susceptance i.e. $1/\omega L > \omega C$. As a result, the net susceptance is inductive, meaning the circuit behaves like a parallel RL circuit.
- At resonance, the inductor and capacitor currents are equal in magnitude and opposite in phase, not zero. They cancel each other at the supply terminals. This results in a minimum source current and a purely resistive (unity power factor) load for the source. Thus, statement (II) is false.

37. (c)

Elements should be also bilateral to satisfy the reciprocity. Thus, Statement (II) is false.

38. (c)

The voltage across the inductor is given by:

$$v = L\frac{di}{dt}$$

Thus, the potential drop across the inductor is proportional to the rate of change of the current. For direct current, $di/dt = 0$. Therefore, voltage across the inductor $v = 0$ i.e. the pure inductor behaves as a short circuit. Hence, Statement (I) is true but Statement (II) is false.

Section B : Digital Circuits

39. (c)

To ensure that the ripple voltage on the D.C. supply does not affect the accuracy of the A/D converter, the maximum allowed peak-to-peak ripple voltage must be less than or equal to one LSB i.e. the maximum ripple voltage is nearly equal to the ADC resolution given by,

$$\text{Maximum peak to peak ripple voltage} = \frac{5}{2^{10}-1} \approx 4.89\ \text{mV}$$

40. (b)

The maximum number that can be represented using a 2's complement form is $(2^{n-1} - 1)$ and the most negative number that can be represented using 2's complement form is -2^{n-1}.

41. (b)

(a) A MUX is a combinational circuit since it has no feedback element present.

(b) A MUX has only 1 output line, n select lines and 2^n input lines. It propagates one the 2^n input signals to the output based on the select-line inputs.

(c) Multiplexers can be constructed using basic logic gates, AND gates for enabling inputs, OR gates for combining them, and NOT gates for the select line complements.

(d) A MUX can be used to construct any logic gate by appropriately connecting its data inputs and select lines.

42. (b)

The resolution of the DAC is equal to the value of the output corresponding to the LSB input. Assuming the input $b_3b_2b_1b_0 = 0001$,

$$V_0 = -\frac{R_F}{R} \times b_0$$

$$-0.1 = -\frac{R_F}{8\times10^3} \times 5$$

$$R_F = \frac{0.1\times8\times10^3}{5}\ \Omega = 160\ \Omega$$

43. (b)

The given counter is a MOD-6 counter as it has six distinct states. Considering n flip-flops,

$$2^n \geq \text{MOD}$$

$$2^n \geq 6$$

$$\therefore \quad n_{\min} = 3$$

44. (b)

N-MOS can be fabricated with the required area less than that of P-MOS and RTL logic family. Thus, an N-MOS logic family has the highest packing density.

45. (a)

$$f(A, B, C, ...) = A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D + ...$$

$$= A + \bar{A}(B + \bar{B}C + \bar{B}\bar{C}D + ...)$$

$$= A + \bar{A}X \qquad (\text{where } X = B + \bar{B}C + \bar{B}\bar{C}D + ...)$$

$$= A + X \qquad (\because A + \bar{A}X = A + X)$$
$$= A + B + \bar{B}C + \bar{B}\bar{C}D + ...$$
$$= A + B + \bar{B}(C + \bar{C}D + ...)$$
$$= A + B + \bar{B}Y \qquad \text{where } Y = C + \bar{C}D + ...$$
$$= A + B + C + ...$$

Hence, option (a) is correct.

46. (c)

The K-map of the given function $f(A, B, C) = \Sigma m(1, 2, 5, 6)$ is as follows:

A \ BC	00	01	11	10
0	0	1	0	1
1	0	1	0	1

The K-map of the function $\overline{f(A, B, C)}$ is as follows:

A \ BC	00	01	11	10
0	1	0	1	0
1	1	0	1	0

$$\therefore \quad \overline{f(A, B, C)} = \bar{B}\bar{C} + BC = B \odot C$$

47. (a)

The output logic function of the given circuit can be expressed as,

$$f = \overline{\left(\overline{(\overline{AB})C}\right)\left(\overline{\bar{C}D}\right)} = (\overline{AB})C + \bar{C}D = (\bar{A} + \bar{B})C + \bar{C}D$$

48. (b)

The first MUX acts as a transparent latch when Clk = 1 and holds its data when Clk = 0. The second MUX acts as a transparent latch when Clk = 0 and holds its state when Clk = 1. Since the output Q updates to the value of D precisely on the falling edge (high-to-low transition) of the clock signal, this structure forms a Master-Slave Negative Edge-Triggered D Flip-Flop.

49. (d)

The resolution or the minimum value of current at the output for LSB is

$$\frac{I_{FS}}{2^n - 1} = \frac{2\text{ mA}}{63} = 31.746\ \mu\text{A}$$

Thus, for $(100000)_2 = (32)_{10}$ as an input, the output is, $I_{out} = 32 \times 31.746 \times 10^{-6} = 1016\ \mu\text{A}$

The error is 0.5% on full scale.

So, the absolute error, $$\delta = \frac{0.5 \times 2 \times 10^{-3}}{100} = \pm 10\ \mu\text{A}$$

Thus, the range of output current, I_{out} = 1006 μA to 1026 μA

50. (c)

From the given diagram,

$$J_1 = \bar{Q}_1 Q_2$$
$$K_1 = \bar{Q}_2$$
$$J_2 = K_2 = \bar{Q}_1$$

Also given, $Q_1 = 0$; $Q_2 = 0$ initially. The state table of the circuit can be drawn as below:

Clk	Q_1	Q_2	J_1	K_1	J_2	K_2
0	0	0	0	1	1	1
1	0	1	1	0	1	1
2	1	0	0	1	0	0
3	0	0	0	1	1	1

The counter goes through three distinct states in the sequence: 111 → 011 → 100. Thus, it is a MOD-3 counter.

51. (a)

The truth table of the circuit can be drawn as below:

V_1	V_2	Y	M_1	M_2	M_3	M_4
0	0	V_{DD}	OFF	OFF	ON	ON
0	V_{DD}	0	OFF	ON	OFF	ON
V_{DD}	0	0	ON	OFF	ON	OFF
V_{DD}	V_{DD}	0	ON	ON	OFF	OFF

Thus, the circuit works as a positive NOR gate.

52. (a)

From the figure, we can conclude that,

$$Y_0 = X_0 \odot X_0$$
$$Y_1 = X_1 \oplus X_0$$
$$Y_2 = X_2 \oplus X_0$$

Now, for given input, $X_2 = 1$, $X_1 = 0$, $X_0 = 1$,

$$Y_0 = 1$$
$$Y_1 = 1$$
$$Y_2 = 0$$

So, $(Y_2 Y_1 Y_0) = (011)_2 = (3)_{10}$

53. (c)

For a n-bit dual-slope ADC, the worst-case conversion time is

$$t_{max} = 2^{n+1} T_{clock} = 2^9 T_{clock}$$

Minimum conversion rate, $$R_{min} = \frac{1}{t_{max}} = \frac{1}{2^9 T_{clock}} = \frac{f_{clock}}{2^9} = \frac{50000}{512} = 97.65 \text{ Hz}$$

54. (a)

We can look at the options by adding $(2F)_{16}$ to the second operand and checking if it matches the first operand.

1. $(2F)_{16} + (2F)_{16} = (5E)_{16}$

   Thus, first option is correct

2. $(F1)_{16} + (2F)_{16} = (120)_{16}$

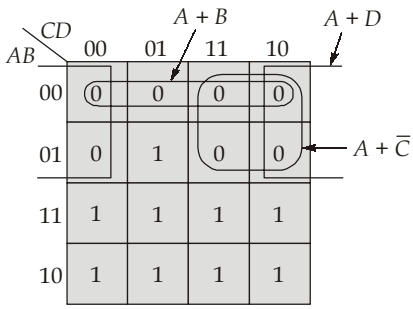
   Thus, second option is correct

3. $(22)_{16} + (2F)_{16} = (51)_{16}$

   Thus, third option is incorrect.

55. (c)

Drawing the K-map, we have,



For the maxterm expression, we group the 0 terms in K-Map and thus, we get,

$$f = \Pi M(0, 1, 2, 3, 4, 6, 7)$$

$$= (A+B)(A+\bar{C})(A+D)$$

56. (d)

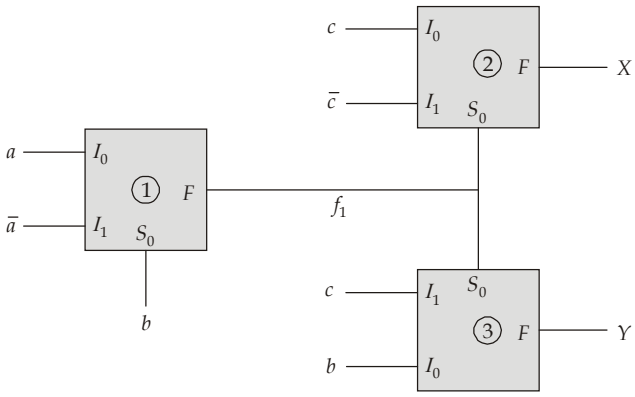
To create 5 bit parallel adder, we require 4-full adder plus 1 Half adder.

A 1-bit full adder requires 2 XOR gates, 2 AND gates, and 1 OR gate. For 4 full adders, we require 8 Ex-OR gates, 8 AND gates and 4-OR gates.

and for 1 Half adder, we require only 1 Ex-OR gate and one AND gate.

Thus, for 5-bit adder, we require 9 Ex-OR gates, 9 AND gates and 4 OR gates.

57. (b)



The output of 1st MUX, $f_1 = (a\bar{b} + \bar{a}b)$

Thus, Output $X = \overline{(a\bar{b} + \bar{a}b)}c + (a\bar{b} + \bar{a}b)\bar{c} = \overline{(a \oplus b)} \cdot c + (a \oplus b) \cdot \bar{c}$

$= a \oplus b \oplus c$

and Output $Y = \overline{(a\bar{b} + \bar{a}b)}b + (a\bar{b} + \bar{a}b)c = (ab + \bar{a}\bar{b}) \cdot b + (a\bar{b} + ab) \cdot c$

$= ab + a\bar{b}c + \bar{a}bc = (ab + a\bar{b}c) + (ab + \bar{a}bc)$

$= a(b + \bar{b}c) + b(a + \bar{a}c) = a(b + c) + b(a + c) = ab + bc + ca$

Here, X represents the expression of Sum and Y represents the expression of Carry for a Full-adder. So, the given circuit can act as a full-adder.

58. (c)

A combinational circuit does not have any feedback paths or storage elements. The output depends only on the present input values, and not on the past inputs.

59. (c)

$(64)_8 = 6 \times 8 + 4 = (52)_{10}$

$(-64)_{10} + (52)_{10} = (-12)_{10}$

thus, $X = -12$

60. (d)

An n-bit ring counter can count only n-pulses whereas an n-bit ripple counter can count 2^n pulses. In a ring counter, we do not require a decoder circuit because we can read the count by simply noting which flip-flop is set.

An n-bit Johnson counter has 2^n distinct states, thus statement 3 is not correct.

61. (c)

The output 'F' can be represented in the K-Map as below:

AB \ CD	00	01	11	10
00	1	0	1	0
01	1	0	1	1
11	1	0	0	0
10	1	0	0	0

thus, $F = \bar{A}BC + \bar{A}CD + \bar{C}\bar{D}$

F can also be expressed as

$F = \bar{A}BC + \bar{A}CD + \bar{C}\bar{D}(A + \bar{A})$

$= \bar{A}BC + \bar{A}CD + \bar{A}\bar{C}\bar{D} + A\bar{C}\bar{D}$

62. (b)

Converting the octal numbers to binary,

$$(26)_8 = (00010110)_2$$

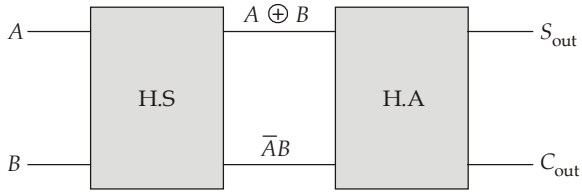
and $$(75)_8 = (00111101)_2$$

In 2's complement form, $$-(75)_8 = (11000010)_2 + 1 = (11000011)_2$$

$$\begin{array}{r} 0\,0\,0\,1\,0\,1\,1\,0 \\ 1\,1\,0\,0\,0\,0\,1\,1 \\ \hline (1\,1\,0\,1\,1\,0\,0\,1)_2 \end{array}$$

Result in 2's complement form $\Rightarrow$

63. (c)



$$\therefore \quad S_{out} = (A \oplus B) \oplus \overline{A}B$$

$$C_{out} = (A \oplus B) \cdot \overline{A}B$$

$$\therefore \quad S_{out} = (A\overline{B} + \overline{A}B)(\overline{\overline{A}B}) + (\overline{A}\overline{B} + AB)(\overline{A}B)$$

$$= (A\overline{B} + \overline{A}B)(A + \overline{B})$$

$$= A\overline{B}$$

and $$C_{out} = (A\overline{B} + \overline{A}B)(\overline{A}B)$$

$$= \overline{A}B$$

64. (b)

$$(09)_{10} \xrightarrow{\text{Excess-3}} (12)_{10} = 1100$$

$$(09)_{10} \xrightarrow{\text{BCD}} 1001$$

$$(10)_{10} = 1010 \xrightarrow{\text{Gray Code}} 1111$$

$$(10)_{10} \xrightarrow{\text{Binary Code}} 1010$$

Note: To convert a binary number to its corresponding Gray code,keep the most significant bit (MSB) the same. For each subsequent bit, perform an XOR operation between the current binary bit and the previous binary bit.

65. (d)

For PMOS

$$Y = \overline{(A \cdot B)(C + D)}$$

$$Y = (\overline{AB}) + (\overline{C} \cdot \overline{D})$$

$$Y = (\overline{A} + \overline{B}) + (\overline{C} \cdot \overline{D})$$

66. (b)

The Master-Slave configuration is used to eliminate Race-around condition ensuring that the output changes only once per clock cycle.

67. (d)

- A multiplexer selects one of several input signals and forwards it to a single output. Thus, it can be used as a data selector.
- Multiplexer circuit can also be used in data acquisition devices where the input data is to be received from many sources.
- By feeding sequential select signals (such as from a counter), multiple parallel data bits can be read out one by one, effectively converting parallel data into a serial data stream.

Thus, all the given statements are correct.

68. (d)

- CMOS circuits draw negligible static power because one of the complementary transistors (N-channel or P-channel) is always turned off in steady states.
- The noise margin of a CMOS gate is proportional to the supply voltage V_{DD}. So, increasing VDD results in higher noise margin.
- CMOS devices are sensitive to electrostatic discharge (ESD), which can damage their thin gate-oxide layer.

Thus, all the given statements are correct.

69. (c)

$$x \oplus y \oplus xy = x \oplus (y \oplus xy) = x \oplus \left(y(\overline{xy}) + \overline{y}(xy)\right)$$
$$= x \oplus \left(y(\overline{x} + \overline{y}) + \overline{y}(xy)\right) = x \oplus \overline{x}y$$
$$= \overline{x}(\overline{x}y) + x(x + \overline{y}) = x + x\overline{y} + \overline{x}y$$
$$= x + \overline{x}y = x + y$$

70. (b)

A standard n-bit shift register cannot directly function as a Modulo-2^n binary counter, as it requires binary counting logic. A Linear Feedback Shift Register (LFSR) can only generate up to $2^n - 1$ states using feedback logic.

71. (b)

Representing the given Boolean expression in K-Map,

AB \ CD	00	01	11	10
00	×	1	1	×
01		×	1	
11			1	
10			1	

$\therefore$ $Y = \overline{A}\overline{B} + CD$

72. (c)

AND + NOT Gate and OR + NOT Gate make the universal gates NAND and NOR respectively, which are sufficient to realize any logic function. However, they are not necessary to realize a logic function, they are only sufficient. Hence, only statement 3 is correct.

73. (d)

At each active clock edge, the output Q takes the value of the D-input sampled at that instant. The output does not continuously follow the input between clock edges. Thus, all the given statements are correct.

74. (b)

The output of a NAND gate is given by

$$Y = \overline{A \cdot B \cdot C.....}$$

If all the inputs are shorted to get one input, we get $Y = \overline{A}$, i.e. an inverter.

The reason does not mention the condition of all inputs being '1' and output to be '0'. Thus, Both Statement (I) and Statement (II) are true but Statement (II) is not a correct explanation of Statement (I).

75. (d)

A demultiplexer routes one data input to a selected output based on the select lines, whereas a decoder activates the output corresponding to the given input lines. Thus, a demux can be used as decoder if the input lines are treated as enable input and the select line as the input. Hence, Statement (I) is false.

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