DETAILED SOLUTIONS

MADE EASY

Leading Institute for ESE, GATE & PSUs

Test Centres: Delhi, Hyderabad, Bhopal, Jaipur, Pune

ESE 2027 : Prelims Exam
CLASSROOM TEST SERIES

ELECTRICAL ENGINEERING

Test 2

Section A : Electrical Circuits [All Topics]

Section B : Digital Electronics + Microprocessors [All Topics]

ANSWER KEY

1. (d)	**16.** (a)	**31.** (b)	**46.** (d)	**61.** (d)
2. (c)	**17.** (d)	**32.** (c)	**47.** (b)	**62.** (c)
3. (c)	**18.** (a)	**33.** (c)	**48.** (a)	**63.** (c)
4. (b)	**19.** (c)	**34.** (d)	**49.** (b)	**64.** (d)
5. (c)	**20.** (c)	**35.** (b)	**50.** (c)	**65.** (b)
6. (d)	**21.** (a)	**36.** (d)	**51.** (d)	**66.** (b)
7. (d)	**22.** (d)	**37.** (c)	**52.** (b)	**67.** (b)
8. (c)	**23.** (d)	**38.** (d)	**53.** (d)	**68.** (b)
9. (c)	**24.** (c)	**39.** (c)	**54.** (b)	**69.** (b)
10. (c)	**25.** (d)	**40.** (c)	**55.** (b)	**70.** (c)
11. (b)	**26.** (b)	**41.** (b)	**56.** (b)	**71.** (c)
12. (c)	**27.** (a)	**42.** (b)	**57.** (d)	**72.** (c)
13. (b)	**28.** (b)	**43.** (b)	**58.** (d)	**73.** (a)
14. (c)	**29.** (c)	**44.** (a)	**59.** (d)	**74.** (b)
15. (a)	**30.** (c)	**45.** (a)	**60.** (c)	**75.** (b)

DETAILED EXPLANATIONS
Section A : Electrical Circuits

1. (d)

Limitations of superposition theorem:

- This theorem is applicable only to linear circuits..
- This theorem cannot be used to measure power.
- This theorem is applicable only for the circuits having more than one source.

2. (c)

If the voltage or current associated with a particular resistor is used as a controlling variable for a dependent source, it must not be included in the source transformation and should be left untouched.

3. (c)

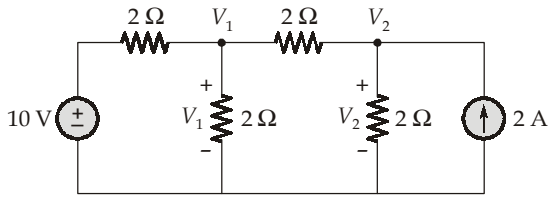
Both Statements 1 and 2 are correct.

- Interchange of an ideal voltage source and an ideal ammeter in any passive linear bilateral circuit will not change the ammeter reading.
- The interchange of an ideal current source and an ideal voltmeter in any passive linear bilateral circuit will not change the voltmeter reading.

4. (b)

"In a two-terminal electrical network containing at least one inductor and one capacitor, we define resonance as the condition which exists when the input impedance of the network is purely resistive."

5. (c)



KCL at node V_1 :

$$\frac{V_1 - 10}{2} + \frac{V_1}{2} + \frac{V_1 - V_2}{2} = 0$$

$$3V_1 - V_2 = 10 \quad \ldots(i)$$

KCL at node V_2 :

$$\frac{V_2}{2} + \frac{V_2 - V_1}{2} = 2$$

$$2V_2 - V_1 = 4 \quad \ldots(ii)$$

By solving (i) and (ii), we get

$$V_2 = \frac{22}{5} \ ;$$

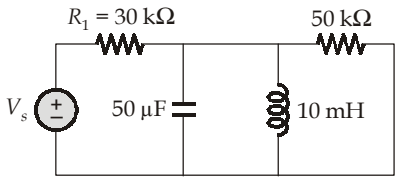
$$V_1 = \frac{24}{5}$$

$$|V_1 - V_2| = \frac{2}{5}$$

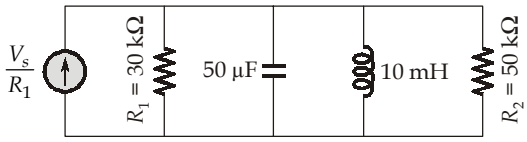
Multiply by 9 in numerator and denominator, we get

$$|V_1 - V_2| = \frac{18}{45}$$

6. (d)

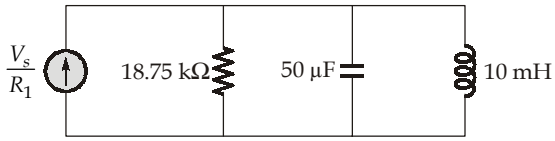


Apply source transformation,



$$R_1 \parallel R_2 = (30 \parallel 50)$$

$$\Rightarrow \quad \frac{30 \times 50}{30 + 50} = 18.75 \text{ k}\Omega$$



Above circuit is parallel RLC circuit.

Resonant frequency, $\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{10 \times 10^{-3} \times 50 \times 10^{-6}}}$

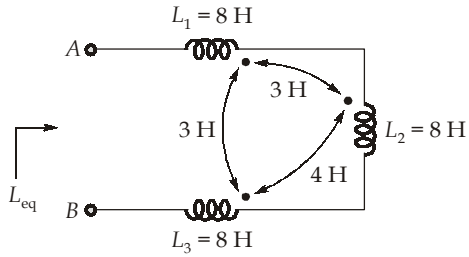
$= 1.414\text{K rad/sec}$

Quality factor, $Q = \frac{R}{\omega_0 L} = \frac{18.75 \times 10^3}{1.414 \times 10^3 \times 10 \times 10^{-3}}$

$= 1326.02546 \approx 1326$

Bandwidth, $\text{B.W.} = \frac{\omega_0}{2\pi Q} = \left(\frac{1.414 \times 10^3}{1326}\right)\frac{1}{2\pi} = 0.1697 \text{ Hz}$

7. (d)



$M_{12} = 3$ H

$M_{13} = 3$ H

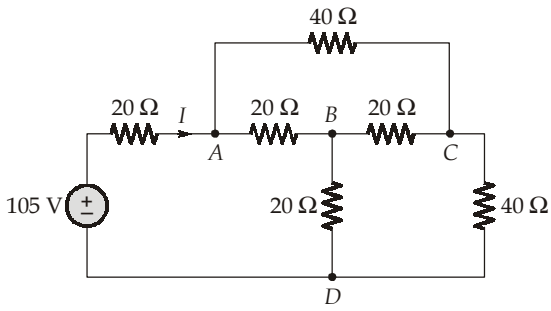
$M_{23} = 4$ H

current is leaving L_1

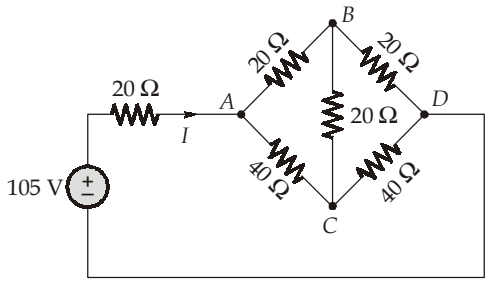
current is entering in L_2 and L_3

$$L_{eq} = L_1 + L_2 + L_3 - 2M_{12} - 2M_{13} + 2M_{23}$$
$$= 8 + 8 + 8 - 2 \times 3 - 2 \times 3 + 2 \times 4$$
$$= 20 \text{ H}$$

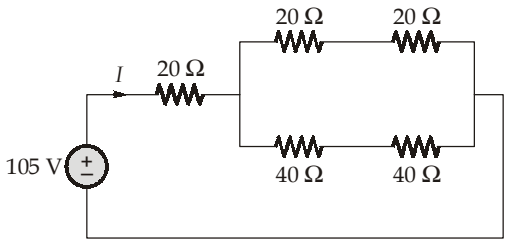
8. (c)

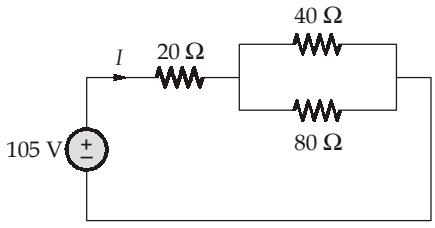


Rearranging the circuit,



Above circuit is balanced Wheatstone bridge rearranging the circuit

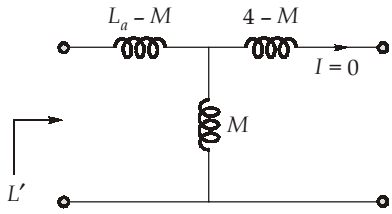




$$I = \frac{105}{20 + (40 \parallel 80)} = \frac{105}{20 + \frac{80}{3}} = 2.25\,\text{A}$$

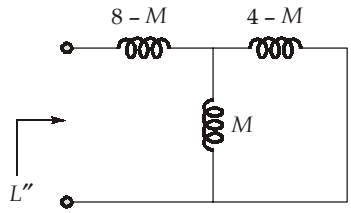
9. (c)

Case-1: Terminal 3 and 4 open circuited,



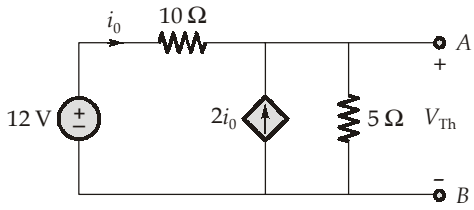
$$L' = L_a - M + M$$
$$8 = L_a$$
$$L_a = 8\ \text{H}$$

Case-2: Terminal 3 and 4 short circuited,



$$L'' = 6\ \text{H (given)}$$
$$L'' = (8 - M) + [(4 - M) \parallel M]$$
$$= (8 - M) + \frac{M \times (4 - M)}{M + (4 - M)} = (8 - M) + \frac{M \times (4 - M)}{4}$$
$$6 = \frac{32 - 4M + 4M - M^2}{4}$$
$$32 - M^2 = 24$$
$$M^2 = 8$$
$$\Rightarrow \quad M = 2\sqrt{2}$$
$$M = K\sqrt{L_a L_b}$$
$$2\sqrt{2} = K\sqrt{8 \times 4} = K \times 4\sqrt{2}$$
$$K = \frac{2}{4} = 0.5$$

10. (c)



KCL node A: $$i_0 + 2i_0 = \frac{V_{Th}}{5}$$

$$3i_0 = \frac{V_{Th}}{5} \quad \text{...(i)}$$

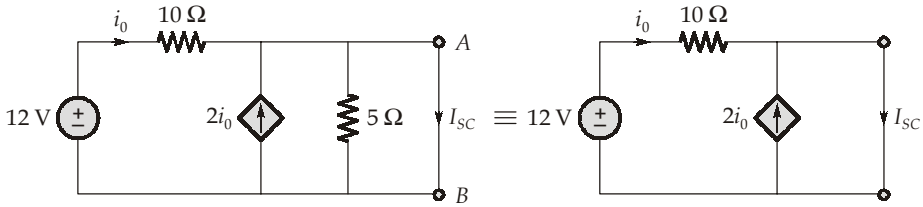
$$i_0 = \frac{12 - V_{Th}}{10}$$

Put value of i_0 in equation (i),

$$3\left(\frac{12 - V_{Th}}{10}\right) = \frac{V_{Th}}{5}$$

$$V_{th} = 7.2 \text{ V}$$

- Calculation of norton current



$$i_0 = \frac{12}{10} = 1.2\text{A}$$

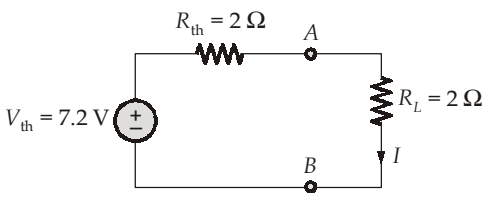
$$I_{SC} = i_0 + 2i_0$$

$$\Rightarrow \quad I_{SC} = 3i_0 = 3(1.2) = 3.6 \text{ A}$$

- Thevenin resistance across AB is:

$$R_{Th} = \frac{V_{Th}}{I_{SC}} = \frac{7.2}{3.6} = 2\Omega$$

- A load connected across AB,



Current through load,

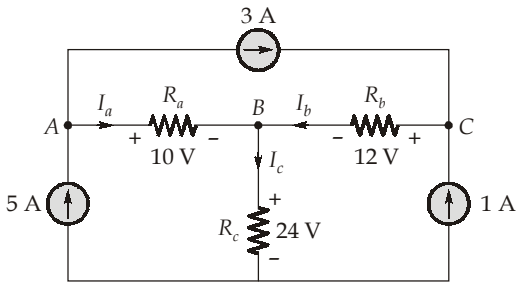
$$R_L = 2\ \Omega$$

$$I = \frac{7.2}{2+2} = 1.8 \text{ A}$$

11. (b)

KCL at node A:

$$3 + I_a = 5$$
$$I_a = 2 \text{ A}$$
$$R_a = \frac{10}{2} = 5\ \Omega$$



KCL at node C:

$$3 + 1 = I_b$$
$$\Rightarrow \quad I_b = 4$$
$$R_b = \frac{12}{4} = 3\Omega$$

KCL at node B:

$$I_a + I_b = I_c$$
$$2 + 4 = I_c$$
$$I_c = 6 \text{ A}$$
$$R_c = \frac{24}{6} = 4\Omega$$

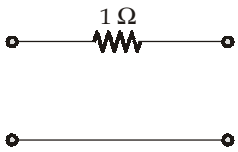
$R_a = 5\ \Omega$, $R_b = 3\ \Omega$, $R_c = 4\ \Omega$

$$R_a + R_b + R_c = 12\ \Omega$$

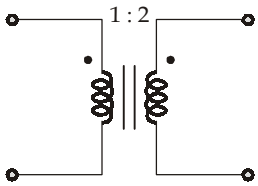
12. (c)

Overall T-parameter

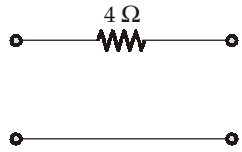
$$[T] = [T_1]\,[T_2]\,[T_3]$$



$$\Rightarrow \quad [T_1] = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$$



$$\Rightarrow \quad [T_2] = \begin{bmatrix} a & 0 \\ 0 & \frac{1}{a} \end{bmatrix} = \begin{bmatrix} 0.5 & 0 \\ 0 & 2 \end{bmatrix}$$



$$\Rightarrow \quad [T_3] = \begin{bmatrix} 1 & 4 \\ 0 & 1 \end{bmatrix}$$

$$[T] = [T_1]\,[T_2]\,[T_3]$$

Multiply $[T_1]\,[T_2]$

$$[T_1]\,[T_2] = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0.5 & 0 \\ 0 & 2 \end{bmatrix} = \begin{bmatrix} 0.5 & 2 \\ 0 & 2 \end{bmatrix}$$

$$[T] = \begin{bmatrix} 0.5 & 2 \\ 0 & 2 \end{bmatrix}\begin{bmatrix} 1 & 4 \\ 0 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 0.5 & 4 \\ 0 & 2 \end{bmatrix}$$

13. (b)

Time constant, $\tau = \dfrac{L}{R_{eq}}$

$$R_{eq} = 1 + (5 \,||\, 20) = 5\ \Omega$$

$$\tau = \frac{2}{5} = 0.4\,\text{sec}$$

Given, $i(0) = 20$ A

For $t > 0$

$$i(t) = 20e^{-t/0.4}\text{A}$$
$$= 20e^{-2.5t}$$

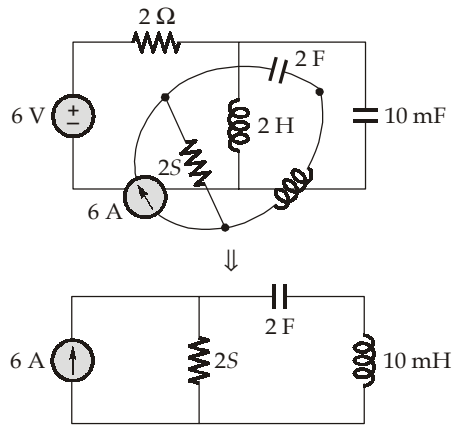
Apply KCL

$$i(t) + \frac{V(t)}{20} + \frac{V(t)}{5} = 0$$

$$5\ V(t) = -20\ i(t)$$
$$V(t) = -4\ i(t)$$

$$\Rightarrow \quad V(t) = -80e^{-2.5t}\ \text{V}\ ;\ t > 0$$

14. (c)



15. (a)

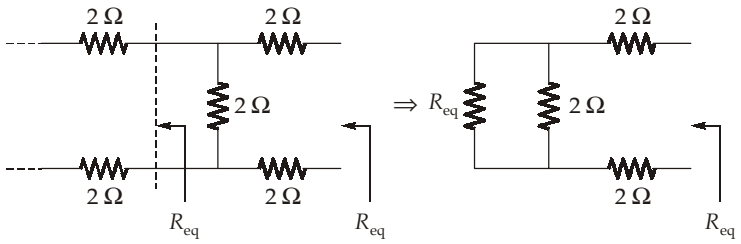
$$\text{Total charge} = \Delta q = 2 \times 10 = 20 \text{ C}$$

The voltage drop is

$$V = \frac{\Delta w}{\Delta q} = \frac{2.3 \times 10^3}{20} = 115 \text{ V}$$

16. (a)

Considering only left half of network



$$R_{eq} = 4 + (2 \parallel R_{eq}) = 4 + \frac{2R_{eq}}{2 + R_{eq}}$$

$$= \frac{8 + 6R_{eq}}{2 + R_{eq}}$$

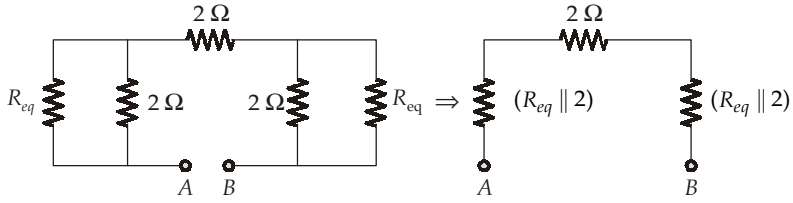
$$2R_{eq} + R_{eq}^2 = 8 + 6R_{eq}$$

$$R_{eq}^2 - 4R_{eq} - 8 = 0$$

$$R_{eq} = \frac{4 \pm \sqrt{16 + 32}}{2} = \frac{4 \pm \sqrt{48}}{2}$$

$$= 2 + 2\sqrt{3} \quad \text{(Consider only +ve value)}$$

The network can be redrawn as



$$(R_{eq} \| 2) = \frac{2 \times R_{eq}}{2 + R_{eq}} = \frac{4 + 4\sqrt{3}}{4 + 2\sqrt{3}}$$

$$R_{ab} = (R_{eq} \| 2) + 2\Omega + (R_{eq} \| 2)$$

$$= 2\left(\frac{4 + 4\sqrt{3}}{4 + 2\sqrt{3}}\right) + 2$$

$$R_{ab} = \frac{16 + 12\sqrt{3}}{4 + 2\sqrt{3}} = \frac{8 + 6\sqrt{3}}{2 + \sqrt{3}}$$

$$R_{ab} = 4.93\ \Omega$$

17. (d)

Expression of $V(t)$,
$$V(t) = \begin{cases} 30 & ; \quad 0 < t < 10 \\ -4t + 70 & ; \quad 10 \le t \le 15 \\ 10 & ; \quad t > 15 \end{cases}$$

Expression of $i(t)$,
$$i(t) = \begin{cases} 2t & ; 0 \le t \le 15 \\ -3t + 75 & ; 15 \le t \le 25 \end{cases}$$

Power,
$$P(t) = \begin{cases} 60t & ; \quad 0 < t < 10 \\ -8t^2 + 140t & ; \quad 10 < t < 15 \\ -30t + 750 & ; \quad 15 \le t \le 25 \end{cases}$$

18. (a)

Quantity	Dual
Mesh	Node
Link	Twig
Tieset	Cutset
Loop current	Node voltage

19. (c)

For parallel circuit, $Y = G + j(B_C - B_L)$

where, $G = \frac{1}{R}, B_L = \frac{1}{X_L}, B_C = \frac{1}{X_C}$

$$\Rightarrow \quad Y = \frac{1}{2} + j\left(\frac{1}{10}\right) - j\left(\frac{1}{5}\right)$$
$$= 0.5 + j(0.1 - 0.2)$$
$$= (0.5 - j0.1)\mho$$

20. (c)

Given, $\overline{V} = 150 \angle 30°$ V

$\overline{I} = 2 \angle -15°$ A

$f = 50$ Hz

$$\overline{Z} = \frac{\overline{V}}{\overline{I}} = \frac{150\angle 30°}{2\angle -15°} = 75\angle 45° \ \Omega$$

$\Rightarrow$ Power factor angle, $\phi = 45°$

Power loss, $P = VI \cos \phi$

$= 150 \times 2 \times \cos 45°$

$$= 150 \times 2 \times \frac{1}{\sqrt{2}} = 150 \times \sqrt{2} = 212.1 \text{ W}$$

21. (a)

Power, $P = I^2R$

$$\Rightarrow \quad R = \frac{P}{I^2} = \frac{250}{(1)^2} = 250 \ \Omega$$

For a series RLC circuit, Q-factor,

$$Q = \frac{\omega_0 L}{R} = \frac{2\pi f_0 L}{R}$$

$$\Rightarrow \quad L = \frac{QR}{2\pi f_0} = \frac{5 \times 250}{2\pi \times 1000} = 0.2 \text{ H}$$

22. (d)

In AC circuits, for maximum power transfer,

- $Z_L = Z_{th}^*$; if the impedance has variable reactive component. Thus, for circuit A, $Z_l = Z_s^*$ and for circuit D, $X_l = -X_s$.
- $Z_L = |Z_{th}|$; if the impedance has only variable resistive component.

Thus, for circuit C, $R_l = \sqrt{R_s^2 + (X_s + X_l)^2}$

and for circuit B, $R_l = |Z_s| = \sqrt{R_s^2 + X_s^2}$

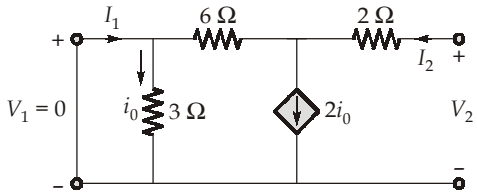
23. (d)

Time domain analysis becomes complex when the system has special input functions and more inductors and capacitors.

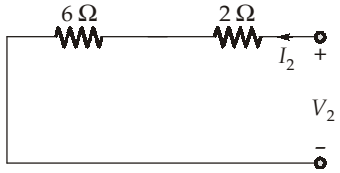
24. (c)

"y_{22}" is called short-circuit output admittance given as,

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0}$$



Due to short-circuit, "i_0" becomes zero, thus the dependent source can be open circuited.
The simplified circuit is,



$$\therefore \quad y_{22} = \frac{I_2}{V_2} = \frac{1}{6+2} = \frac{1}{8} = 0.125\text{S}$$

25. (d)

A. Series-Parallel Connection: The resultant *h*-parameter matrix is the sum of *h*-parameter matrices of each individual two-port networks.

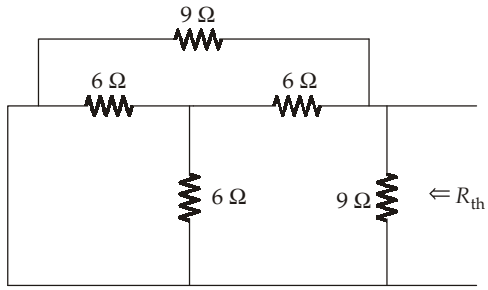
B. Parallel-Series Connection: The resultant *g*-parameter matrix is the sum of *g*-parameter matrices of each individual two-port networks.

C. Parallel Connection: The resultant *y*-parameter matrix for parallel connected networks is the sum of *y* matrices of each individual two-port networks.

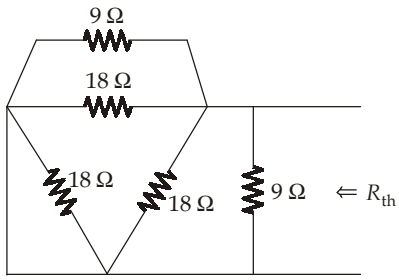
D. Series Connection: The resultant *z*-parameter matrix for the series-connected networks is the sum of *z* matrices of each individual two-port networks.

26. (b)

To calculate R_{th}, deactivate all independent sources.



Using star to delta transformation,



$$R_{th} = 9 \parallel [(9 \parallel 18) \parallel 18] = 9 \parallel \frac{9}{2} = \frac{9 \times \frac{9}{2}}{9 + \frac{9}{2}} = \frac{9 \times 9}{27} = 3\ \Omega$$

For maximum power transfer,

$$R_L = R_{th} = 3\ \Omega$$

27. (a)

at $t = 0^-$

$$V_c(0^-) = V_c(0^+) = 0\ \text{V}$$

at $t > 0$

$$V_c(\infty) = 1\ \text{V}$$

$$V_c(t) = 1\left(1 - e^{-\frac{t}{RC}}\right)$$

$$\frac{dV(t)}{dt} = \frac{1}{RC} e^{-\frac{t}{RC}}$$

$$\frac{dV(0^+)}{dt} = \frac{1}{RC}$$

28. (b)

$$i(t) = \frac{-4 \times 10^{-3}}{8}\left[V(t) - 8\right]$$

$$i(t) = -\frac{1}{2} \times 10^{-3}\left[V(t) - 8\right] = -\frac{1}{2} \times 10^{-3} V(t) + 4 \times 10^{-3}$$

$$V(t) = \frac{2i(t) - 8 \times 10^{-3}}{-10^{-3}} = -2 \times 10^3 i(t) + 8$$

Hence, $R_{th} = 2 \times 10^3\ \Omega$

$$\text{Time constant} = \tau = \frac{L}{R_{th}} = \frac{8 \times 10^{-3}}{2 \times 10^3} = 4\ \mu\text{s}$$

29. (c)

$A \rightarrow$ Mutually adding – coils in parallel.

$B \rightarrow$ Mutually opposing – coils in parallel.

$C \rightarrow$ Mutually opposing – coils in series.

$D \rightarrow$ Mutually adding – coils in series.

For coils in series, $L_{eq} = L_1 + L_2 \pm 2M$

(+ for series aiding connection and – for series opposing connection)

For coils in parallel,

$$L_{eq} = \frac{L_1 L_2 - M^2}{L_1 + L_2 \pm 2M}$$

(– for parallel aiding connection and + for parallel opposing connection)

30. (c)

Whenever an ideal voltage source and ideal current source are connected in series, the current through the combination would be same as the current source. Hence, it will behave like an ideal current source alone and if they are connected in parallel, it will behave like an ideal voltage source alone.

31. (b)

- Forced current is the current due to the external voltage source while the initial condition is zero, which gives zero state response.
- Natural current is the current because of initial conditions with all external voltage sources set to zero, which gives zero input response.

32. (c)

For a series RLC circuit,

$$X_{eq} = |X_L - X_C| = \omega L - \frac{1}{\omega C}$$

At low frequency, $\omega L << 1/\omega C$, hence the circuit impedance is capacitive with

$$X_{eq} = -\frac{1}{\omega C}$$

At high frequency, $\omega L >> 1/\omega C$, hence the circuit impedance is inductive with

$$X_{eq} = \omega L$$

33. (c)

When, load $Z_L = 500 \angle -90° = -j500\ \Omega$

$$Z_{eq} = [Z_L \parallel 500\ \Omega]$$

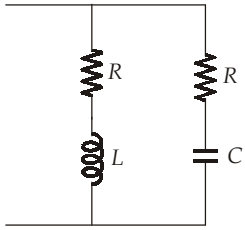
$$Z_{eq} = \frac{-500j \times 500}{500 - 500j} = \frac{-500j}{1 - j} = 250\sqrt{2} \angle -45°$$

$\Rightarrow$ $\cos \phi = \cos 45°$

Power factor = 0.707 lead

34. (d)

For unity power factor, imaginary term of impedance should be zero.



$$Z(j\omega) = \frac{(R + j\omega L)\left(R - \frac{j}{\omega C}\right)}{R + j\omega L + R - \frac{j}{\omega C}}$$

$$Z(j\omega) = \frac{(R + j\omega L)\left(R - \frac{j}{\omega C}\right)\left(2R - j\omega L + \frac{j}{\omega C}\right)}{\left(2R + j\omega L - \frac{j}{\omega C}\right)\left(2R - j\omega L + \frac{j}{\omega C}\right)}$$

$$\text{Imaginary term} = \left(\omega L R^2 - \frac{R^2}{\omega C}\right) - \left(\frac{\omega L^2}{C} - \frac{L}{\omega C^2}\right)$$

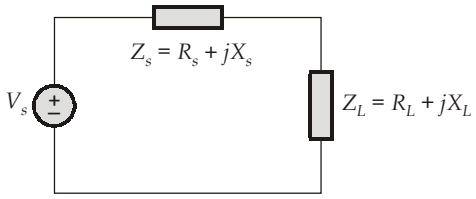
$$= R^2\left(\omega L - \frac{1}{\omega C}\right) - \frac{L}{C}\left(\omega L - \frac{1}{\omega C}\right)$$

For unity power factor, Imaginary term = 0

$$\left(R^2 - \frac{L}{C}\right)\left(\omega L - \frac{1}{\omega C}\right) = 0$$

$$R = \sqrt{\frac{L}{C}}$$

35. (b)



For maximum power transfer

$$Z_L = Z_s^*$$

i.e., $R_L = R_S$ and $X_L = -X_S$

36. (d)

Loop analysis is based on analyzing the network with the help of KVL equations. The loop matrix so obtained from the simultaneous equations cannot be zero and negative and is independent of voltage and current sources and depends on the value of resistances.

37. (c)

$$V_1 = 40I_1 + j20I_2$$
$$V_2 = j30I_1 + 50I_2$$
$$V_1 = 100\angle 0°$$

and $V_2 = -10I_2$

Thus, $-10I_2 = j30I_1 + 50I_2$

$$\therefore \quad \frac{I_2}{I_1} = -j0.5$$

38. (d)

- Superposition theorem can't be used for the given circuit, because while acting one source alone, the circuit violates KVL.
- Superposition theorem is applicable when there are different source.

39. (c)

Series and parallel RLC circuits fall into one of three categories, depending on the relative values of R, L and C :

Overdamped $\alpha > \omega_0$

Critically damped $\alpha = \omega_0$

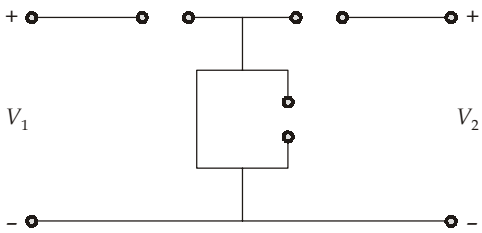
Underdamped $\alpha < \omega_0$

40. (c)

At $\omega = 0$,

i.e., $f = 0$

$$X_L = 0$$
$$X_C = \infty$$



There is no connection between input and output,

So, $V_2 = 0$

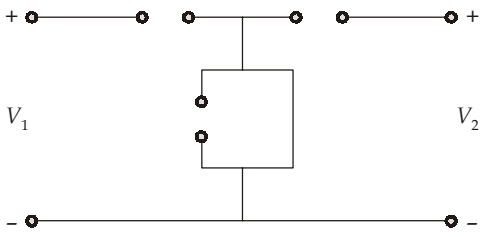
At $\omega = \infty$,

i.e. $f = \infty$,

$$X_L = \infty$$
$$X_C = 0$$

Then also, there is no connection between input and output,

So, $V_2 = 0$



Band pass filter.

41. (b)

Applying KVL in loop-1,

$$v_1 = L_1\frac{di_1}{dt} + M\frac{di_2}{dt}$$

and, $i_2 = 0$

$\therefore$ $$v_1 = L_1\frac{di_1}{dt}$$

$\therefore$ $$\frac{di_1}{dt} = \frac{v_1}{L_1} \quad \text{...(i)}$$

Again, in the output loop,

$$v_2 = M\frac{di_1}{dt} + L_2\frac{di_2}{dt}$$

and, $i_2 = 0$,

$$v_2 = M\frac{di_1}{dt} \quad \text{...(ii)}$$

From equation (i) and (ii), we get

$$v_2 = \frac{Mv_1}{L_1}$$

$$v_{x-y} = \frac{Mv_1}{L_1}$$

42. (b)

y-parameters of 1 Ω resistor network are $\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$

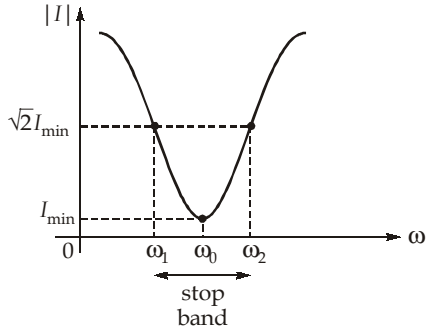
New y-parameter,

$$= \begin{bmatrix} 5 & 3 \\ 1 & 2 \end{bmatrix} + \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 6 & 2 \\ 0 & 3 \end{bmatrix} S$$

43. (b)

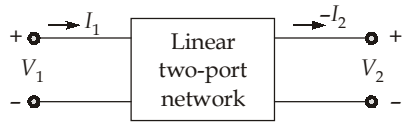
Under parallel resonance condition, the net admittance is minimum so current is also minimum, hence it acts as "rejector circuit". Thus, this phenomenon can be used in the design of band stop or band rejection filter.



At parallel resonant frequency, the currents through '*L*' and '*C*' components are Q-times the supply current. Hence, this circuit is considered as "current amplification circuit".

45. (a)

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2$$

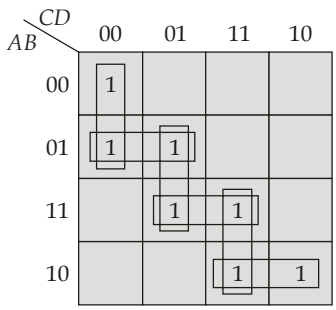


The above two-port parameters provide a measure of how a circuit transmits voltage and current from a source to a load. These parameters are useful in the analysis of transmission lines (such as cable and fiber) because they express sending-end variables (V_1 and I_1) in terms of the receiving-end variables (V_2 and $-I_2$). For this reason, these parameters are called transmission parameters, and are also known as *ABCD* parameters. These parameters are used in the design of telephone systems, microwave networks, and radars.

Section B : Digital Electronics + Microprocessors

46. (d)

Essential prime implicants which is having atleast one minterm which is not the part of any other prime implicants. Now using *K*-map for the given function,



Here total no. of prime implicants = 6 and the no. of essential prime implicants = 2.

Minimize expression = $\bar{A}\bar{C}\bar{D} + B\bar{C}D + ACD + A\bar{B}C$

Total no. of literals in minimized expression = 12.

47. (b)

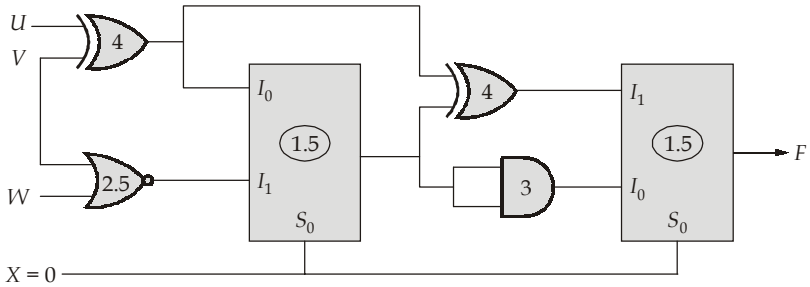
For a function F to be self dual, it should satisfy two conditions:

1. No. of min terms = No. of max. terms.
2. There should not be any mutually exclusive term; option (d), $F(A, B, C) = \Sigma m(0, 2, 3, 6)$.

Condition-1 is satisfied and condition-2 is also satisfied as it does not have any mutually exclusive term.

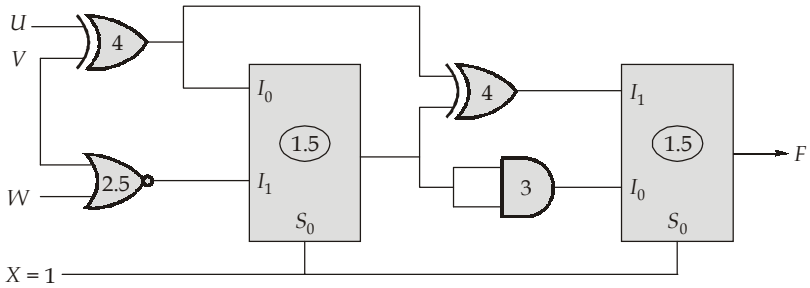
48. (a)

For $X = 0$



Propagation delay = 4 + 1.5 + 3 + 1.5 = 10 nsec

For $X = 1$



Propagation delay = 2.5 + 1.5 + 4 + 1.5

= 9.5 nsec

Maximum propagation delay = 10 nsec

49. (b)

$$Y = \bar{C}(A\bar{C} + BC) + C(B\bar{C} + AC)$$

$$= A\bar{C} + AC = A$$

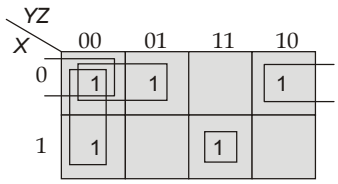
50. (c)

- TRAP is edge as well as level triggered vectored interrupt and it has highest priority.
- RST 7.5 is edge triggered, vectored interrupt.
- RST 6.5 is a level triggered, vectored interrupt.
- TRAP and INTR is unaffected by SIM instructions.

51. (d)

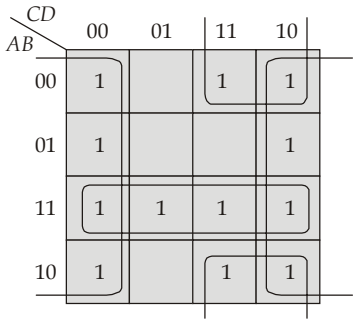
$$F = \overline{(\overline{XYZ}) \oplus (XY) \oplus (\overline{YZ}) \oplus (XZ)}$$

X	Y	Z	XY	$\overline{YZ}$	XZ	$\overline{XYZ}$	F
0	0	0	0	1	0	1	1
0	0	1	0	1	0	1	1
0	1	0	0	1	0	1	1
0	1	1	0	0	0	1	0
1	0	0	0	1	0	1	1
1	0	1	0	1	1	1	0
1	1	0	1	1	0	1	0
1	1	1	1	0	1	0	1

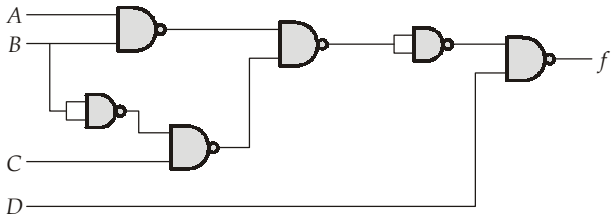


$$F = \bar{X}\bar{Y} + \bar{Y}\bar{Z} + \bar{X}\bar{Z} + XYZ$$

52. (b)



From the K-map, we have, $f = \bar{D} + AB + \bar{B}C$



53. (d)

Type of the clock is positive edge triggered and it is ripple counter,

Let the present state at (Q_1Q_0) = 10 then next four states are

$10 \rightarrow 01 \rightarrow 00 \rightarrow 11 \rightarrow 10$

Hence answer is 01, 00, 11, 10

54. (b)

$$f = \overline{AC} + \bar{A}C$$
$$= \overline{A(\overline{AB} + \bar{A}B)} + \bar{A}(\overline{AB} + A\bar{B})$$
$$f = \overline{A\bar{B}} + \bar{A}(\bar{A} + \bar{B} + \bar{A}B)$$
$$f = \bar{A} + B + \bar{A} + \bar{A}\bar{B} + \bar{A}B$$
$$= \bar{A} + B$$

55. (b)

$$f = 1 \cdot \bar{S}_2\bar{S}_1 + \overline{A \cdot B} \cdot \bar{S}_2 S_1 + 0 \cdot S_2 \cdot \bar{S}_1 + 0 \cdot S_2 S_1$$
$$f = \bar{S}_2\left[\bar{S}_1 + \overline{AB}S_1\right]$$

56. (b)

Q_2^{+1}	Q_1^{+1}	Q_0^{+1}
0	0	0
0	0	1
0	1	1
1	1	0
1	0	1
0	1	0
⋮	⋮	⋮

Here, $Q_2^{+1} = Q_1$

$Q_1^{+1} = Q_0$

$Q_0^{+1} = Q_2 \odot Q_1$

So, the sequence of Q_0 is 011010 ....

57. (d)

Option (a) and (b) are properties of Von-neumann architecture. Speed of harvard architecture is more than Von-Neumann. This type of architecture can result in space wastage because instruction memory cannot utilize the left over space in the data memory.

58. (d)

A	B	Q_{n+1}	J	K
0	0	Q_n	0	0
0	1	1	1	0
1	0	$\bar{Q}_n$	1	1
1	1	0	0	1

$$J = A \oplus B$$

59. (d)

LXI H, XX 65H

Flag resister value unknown

MVI M, FFH

INR M

Value of M is 00H

$\Rightarrow \quad Z = 1$

INR does not affect the carry flag.

60. (c)

Only statement-3 is incorrect because encoder is a combinational circuit that performs the reverse operation of decoder. It has maximum of 2^n input lines and 'n' output lines, hence it encodes the information from 2^n input an n-bit code.

61. (d)

$J = \bar{Q} \qquad K = 1$

	Clock	J	K	Q^+
Initially				0
	1	1	1	1
	2	0	1	0
	3	1	1	1
	4	0	1	0
	5	1	1	1

62. (c)

$Q_{n+1} = D_n = X \oplus Q_n$

X	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$X = 0 \quad \Rightarrow \quad Q_{n+1} = Q_n$

$X = 1 \quad \Rightarrow \quad Q_{n+1} = \bar{Q}_n$

$\therefore$ It is a T flip-flop.

63. (c)

Given, $\left(\frac{403}{30}\right)_b = (12.1)_b$

$$\frac{4b^2 + 0b + 3}{3b + 0} = b + 2 + \frac{1}{b}$$

$$4b^2 + 3 = 3b^2 + 6b + 3$$
$$b^2 - 6b = 0$$
$$b = 6$$

So, base of number system is 6.

64. (d)

CLK				
Initially	0	1	1	0
1	1	0	1	1
2	0	1	0	1
3	1	0	1	0

MSB by XORing of last two bits

65. (b)

Given, $F(A, B, C) = \Sigma m(1, 3, 5, 6)$

From the given options, B, C was selected as inputs and A as select line to MUX

	I_0	I_1
$\bar{B}\bar{C}$	0	4
$\bar{B}C$	(1)	(5)
$B\bar{C}$	2	(6)
BC	(3)	7

Therefore,
$$I_0 = \bar{B}C + BC = (\bar{B} + B)C$$
$$I_0 = C$$
$$I_1 = \bar{B}C + B\bar{C} = B \oplus C$$

66. (b)

There are four 8-bit program invisible registers available in 8085 namely instruction register. Temporary register, W register, Z register.

67. (b)

- A master-slave flip-flop stores only 1-bit of information.
- Gray code is generally used with position disk as a position indicator.
- A demultiplexer can be used as a decoder by interchanging select lines with input.

68. (b)

ANI 00H clears accumulator contents and in term sets zero flag. LXI and DCX instructions don't affect the flags. Therefore, JNZ instructions don't affect the flags. Therefore, JNZ instructions fails for the first time itself (Since $Z = 1$).

8085 microprocessor don't jump back to loop again.

$\therefore$ NOP executed only for 1 time.

69. (b)

- Serial data : bits arrive one by one on the same line. Hence it takes more time and less hardware.
- Parallel data : bits arrive simultaneously. Hence it takes less time but more hardware.

70. (c)

$$Y = B\bar{C} + \bar{B}C \Rightarrow B \oplus C$$

$$F = \bar{S}_1 A + S_1 \cdot 1 = \bar{S}_1 A + S_1$$

$$S_1 = Y$$

$$F = \bar{Y}A + Y \Rightarrow A + Y$$

$$Y = B \oplus C$$

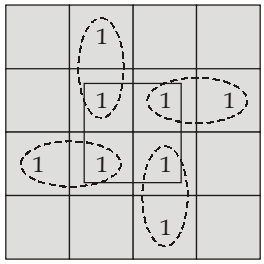
$$F = A + B \oplus C = \overline{\overline{A + (B \oplus C)}} = \overline{\bar{A} \cdot [\bar{B} \odot \bar{C}]}$$

71. (c)

- Dynamic RAM can be implemented by MOS only.
- Static RAM dissipates more power due to BJT and static RAM can be implemented by both BJT and MOS.
- Flash type ADC is fastest.

Flash > SAR > Counter type > Dual-slope

72. (c)



Number of PI = 5

EPI = 4

RPI = 1

73. (a)

- Unconditional CALL instruction requires 18 T-states of execution.
  But conditional CALL takes 18 T-states if the condition is true. otherwise it takes 9-T states.
  Note: Unconditional CALL is always executed.
- 8086 uses 20 lines for address BUS.
- All conditional JUMP are short JUMPs.

75. (b)

Both the statements are correct but there is no relation between them.