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# ESE 2026: Prelims Exam CLASSROOM TEST SERIES

# E&T ENGINEERING

Test 6

Section A: Electronic Devices & Circuits + Analog Circuits

Section B: Control Systems-1 + Microprocessors and Microcontroller-1

Section C: Network Theory-2 + Digital Circuits-2

1.	(d)	16.	(d)	31.	(c)	46.	(a)	61.	(b)
2.	(b)	17.	(c)	32.	(a)	47.	(b)	62.	(d)
3.	(b)	18.	(c)	33.	(b)	48.	(c)	63.	(a)
4.	(*)	19.	(d)	34.	(c)	49.	(a)	64.	(b)
5.	(a)	20.	(c)	35.	(b)	50.	(c)	65.	(c)
6.	(d)	21.	(d)	36.	(b)	51.	(d)	66.	(d)
7.	(b)	22.	(d)	37.	(c)	<b>52.</b>	(c)	67.	(b)
8.	(b)	23.	(d)	38.	(a)	53.	(c)	68.	(c)
9.	(a)	24.	(c)	39.	(c)	54.	(d)	69.	(b)
10.	(b)	25.	(a)	40.	(d)	55.	(b)	70.	(c)
11.	(d)	26.	(d)	41.	(a)	56.	(c)	71.	(b)
12.	(d)	27.	(c)	42.	(d)	57.	(d)	72.	(d)
13.	(b)	28.	(c)	43.	(d)	58.	(a)	73.	(a)
14.	(a)	29.	(c)	44.	(d)	59.	(a)	74.	(c)
15.	(b)	30.	(a)	45.	(a)	60.	(b)	75.	(c)



# **DETAILED EXPLANATIONS**

# Section A: Electronic Devices & Circuits + Analog Circuits

# 1. (d)

- For avalanhe breakdown (dominant at higher breakdown voltages, typically > 5.5 V), the voltage increases with temperature due to increased scattering reducing charge carrier mean free path. Since the statement 1 uses the general term "Zener breakdown voltage" and this characteristics is true for the common avalanche-dominant zener diode. Hence statement-1 is correct.
- Zener diodes can be used as voltage clamps in transient voltage suppression (TVs) circuits. The clamping action limits high-frequency noise or sharp voltage spikes (transients) that contain high-frequency components, thereby reducing the noise level seen by rest of the circuit. Hence statement 2 is correct.
- The statement-3 is a primary application of the zener diode, where it is used in its reverse breakdown region. When the voltage across the device exceeds the zener voltage  $(V_z)$ , the diode clamps the voltage at  $V_{z'}$  shunting the excess current away from the sensitive components. Hence statement-3 is correct.

# 2. (b)

Given for silicon  $P^+N$  junction diode,

Carrier life time,

$$\tau_p = 10 \, \mu \text{sec}$$

Mobility,

$$\mu_P = 3500 \text{ cm}^2/\text{V-sec}$$

Required ratio:

$$\frac{D_P}{L_P} = \frac{D_P}{\sqrt{D_P \tau_P}} = \sqrt{\frac{D_P}{\tau_P}} = \sqrt{\frac{\mu_P \cdot V_T}{\tau_P}}$$

*:*.

$$\frac{D_P}{L_P} = \sqrt{\frac{3500 \times 0.026}{10 \times 10^{-6}}} = \sqrt{9100000} \simeq 3016 \text{ cm/s}$$

# 3. (b)

LEDs start emitting light in nanoseconds, not microseconds.

# 4. (\*)

The photocurrent increases with an increase in light intensity.

Schottky photodiodes are used in optical communication where the bandwidth is high, not low. Hence, statement (1) and statement (3) are incorrect. So, no option is matching.

# 5. (a)

Given, wavelength of silicon photodetector,

$$\lambda = 4.23 \, \mu \text{m}$$

But,

$$\lambda = \frac{1.24}{E_{\sigma} \text{ (eV)}} \mu \text{m}$$

∴ Energy gap,

$$E_g = \frac{1.24}{\lambda} \text{ eV} = \frac{1.24}{4.23} \text{ eV} = 0.293 \text{ eV}$$

# 6. (d)

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7. (b)

In an n-type MOS capacitor, inversion forms a minority carrier (p-type) channel, not majority.

8. (b)

For a photodiode, the steady-state photo current density is,

$$\begin{split} J &= q [W + L_n + L_p] G \\ J &= 1.6 \times 10^{-19} [0.1 + 2 + 1] \times 10^{-3} \times 10^{20} \\ J &= 4.96 \times 10^{-2} \text{ A/cm}^2 = 49.6 \text{ mA/cm}^2 \end{split}$$

9. (a)

In planar BJTs, both junctions are formed by diffusion into the same side of the wafer, not drift.

10. (b)

Given, Length of semiconductor, L = 4 cm

Applied DC voltage,  $V_{\rm dc}$  = 8 V

Electron mobility,  $\mu_n = 1200 \text{ cm}^2/\text{V-s}$ 

We know that, Drift velocity,  $v_d = \mu_n E$  (Consider magnitude)

$$v_d = \mu_n \times \frac{V_{dc}}{L} = 1200 \times \frac{8}{4} = 2400 \text{ cm/s}$$

Average Collision time of electrons is,

$$\tau = \frac{L}{v_d} = \frac{4}{2400} = 1.66 \text{ ms}$$

- 11. (d)
  - The depletion region acts as an insulator at equilibrium.
  - The metallurgical junction is only a geometrical boundary, while the depletion region extends on both sides.
  - The built-in potential depends on internal charge separation, not external bias.
- 12. (d)
- 13. (b)

Given,

Drain current,

$$I_D = 3 \text{ mA}$$

Drain to source voltage,

$$V_{DS} = 2 \text{ V}$$

Since the MOSFET is operating in saturation region,

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 [1 + \lambda V_{DS}] \qquad ...(i)$$

where,  $\lambda$  is channel length modulation parameter. The drain to source conductance,

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}}$$

$$g_{ds} = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 (\lambda) \qquad ...(ii)$$

From equation (i), we can write

$$\frac{I_D}{1+\lambda V_{DS}} \,=\, \mu_n C_{ox} \frac{W}{2L} \big(V_{GS} - V_T\big)^2$$

We can rewrite equation (ii) as,

$$g_{ds} = \frac{I_D}{1 + \lambda V_{DS}} \cdot \lambda = \frac{I_D}{\frac{1}{\lambda} + V_{DS}} = \frac{3 \times 10^{-3}}{\frac{1}{0.05} + 2}$$

*:*.

$$g_{ds} = 0.136 \text{ mS}$$

14. (a)

By applying an electric field, tilting of energy band causes electrons move toward decreasing potential energy (opposite to the field).

15. (b)

Diffusion profiles depend on forward bias (higher bias  $\rightarrow$  higher injection). In p-n junction, applying a higher forward bias voltage increases the injection of minority carriers into the p and n regions, thereby affecting their diffusion profiles.

16. (d)

The Early effect, or base-width modulation, in a BJT is the variation in the effective base width due to changes in the collector-base voltage. Due to early effect, common-base current gain ( $\alpha$ ) increases, current through emitter junction increases and also punch-through can occur.

17. (c)

Given, optical power incident on photodiode is,

Photo current,

$$P_0 = 2 \mu W$$
$$I_P = 5 \mu A$$

Responsivity,

$$R = \frac{I_p}{P_0} = \frac{5}{2} \text{ A/W} = 2.5 \text{ A/W}$$

18. (c)

In a MOS capacitor, the capacitance is the series combination of the oxide capacitance ( $C_{ox}$ ) and the semiconductor capacitance ( $C_s$ ), so the reciprocal of the total capacitance is the sum of the reciprocals of the individual capacitances:

$$\frac{1}{C_{\text{total}}} = \left[ \frac{1}{C_{ox}} + \frac{1}{C_s} \right]$$

19. (d)

For an NMOS device operating in the linear region,

Transconductance,

$$g_m = \frac{\mu_n C_{ox} W}{L} \cdot V_{DS} = 0.045 \times 10^{-4} \times 2.5$$
  

$$g_m = 0.1125 \times 10^{-4} \text{ T}$$

20. (c)

Given, 
$$C_1 = 40 \text{ nF}$$
,  $C_2 = 60 \text{ nF}$ ,  $L = 24 \text{ mH}$ 

For a Colpitts oscillator,

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$



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where 
$$C_{eq} = \frac{C_1 \times C_2}{C_1 + C_2} = \frac{40 \times 60}{100} = 24 \text{ nF}$$
 
$$\therefore \qquad f_0 = \frac{1}{2\pi\sqrt{24 \times 10^{-3} \times 24 \times 10^{-9}}}$$
 
$$f_0 = \frac{10^6}{48\pi} = 6.63 \text{ kHz}$$
 Feedback fraction,  $F_f = \frac{C_1}{C_2} = \frac{40}{60} = 66.67\%$ 

#### 21. (d)

For an n-channel MOSFET,

but 
$$g_{m} = \frac{g_{m}}{2\pi(C_{gs} + C_{gd})}$$

$$\vdots \qquad \qquad f_{T} = \frac{\frac{W}{L} \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{T})}{2\pi(C_{gs} + C_{gd})} \qquad ...(i)$$

$$\vdots \qquad \qquad I_{D} = \frac{1}{2} \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{T})^{2}$$

$$\vdots \qquad \qquad V_{GS} - V_{T} = \sqrt{\frac{2I_{D}}{\mu_{n} C_{ox} \frac{W}{L}}}$$

Substituting this into equation (i),

$$f_T = \frac{\sqrt{2 \times \frac{W}{L} \times \mu_n C_{ox} \times I_D}}{2\pi (C_{gs} + C_{gd})}$$

$$f_T \propto \sqrt{I_D}$$

Thus, option (d) satisfies the above non-linear relation.

#### 22. (d)

Given, Mid-band gain (A) = 500Feedback factor  $\left| \frac{1}{\beta} \right| = 20$ 

Upper cutoff frequency with feedback,

$$f'_{H} = f_{H} \times (1 + A\beta)$$
  
 $A\beta = 500 \times \frac{1}{20} = 25$   
 $f'_{H} = 60 \text{ kHz } (1 + 25)$   
 $f'_{H} = 156 \text{ kHz}$ 

 $\Rightarrow$ 

23. (d)

Given,

$$V_{rms} = 240 \text{ V}$$

Turns ratio,

$$N_1: N_2 = 4:1$$

Output voltage at secondary side of transformer,

$$V'_{rms} = \frac{240}{4} = 60 \text{ V}$$

Average value of full-wave rectified output,

$$V_{avg} = \frac{2V_m}{\pi}$$

But;

$$60 = \frac{V_m}{\sqrt{2}} \implies V_m = 60\sqrt{2}$$

*:*.

$$V_{avg} = \frac{2 \times 60 \times \sqrt{2}}{\pi} = 54.04 \text{ V}$$

24. (c)

Given,  $R_L = 5~\mathrm{k}\Omega; \, h_{fe} = -51; \, h_{ie} = 1.1~\mathrm{k}\Omega; \, h_{oe} = 25~\mu\mathrm{A/V}$ 

The current amplification of an emitter follower amplifier is,

$$A_{I} = \frac{-h_{fe}}{1 + h_{oe} \times R_{L}}$$

$$= \frac{-(-51)}{1 + 25 \times 10^{-6} \times 5 \times 10^{3}}$$

$$= \frac{51}{1.125} = 45.33$$

25. (a)

Statements 1 and 2 are correct.

Statement 3 is incorrect-clampers can be used in analog processing; they do not inherently prevent usage.

26. (d)

The given circuit is an astable multivibrator

$$\therefore \qquad \text{Time period, } T = (R_1C + R_2C)\ln\left(\frac{1+\beta}{1-\beta}\right)$$

where,  $R_1$  = 10 k $\Omega$ ,  $R_2$  = 20 k $\Omega$ , C = 10  $\mu F$ 

$$T = (10 \times 10^{3} \times 10 \times 10^{-6} + 20 \times 10^{3} \times 10 \times 10^{-6}) \ln\left(\frac{1 + 0.6}{1 - 0.6}\right)$$
$$T = 300 \times 10^{-3} \ln\left[\frac{1.6}{0.4}\right]$$

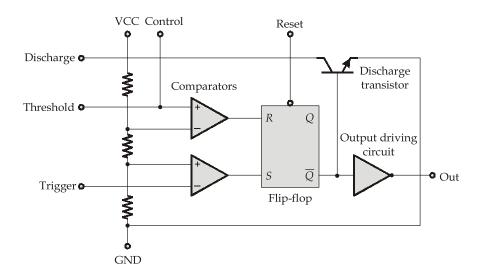
$$\begin{bmatrix} 0.4 \end{bmatrix}$$
  
= 0.3ln[4] = 0.3 × 1.38

$$= 0.3\ln[4] = 0.3 \times 1.38$$

$$T = 0.414 \text{ and}$$

$$T = 0.414 \text{ sec}$$

# 27. (c)



# 28. (c)

A monostable multivibrator returns to the stable state automatically after a single pulse. Thereore, statement-1 is false.

# 29. (c)

For an op-amp, 
$$CMMR = 20 \log \left( \frac{A_{DM}}{A_{CM}} \right)$$

where,  $A_{\it DM}$  : Differential-mode gain

 $A_{CM}$  : Common-mode gain

Given CMRR = 100 dB and  $A_{DM}$  = 4000

$$100 = 20 \log \left( \frac{4000}{\left( \frac{V_0}{15} \right)} \right)$$
$$5 = \log \left( \frac{4000 \times 15}{V_0} \right)$$
$$10^5 = \frac{4000 \times 15}{V_0}$$

:. Output common-mode voltage:

$$V_0 = \frac{4000 \times 15}{10^5} = 0.6 \text{ V}$$

# 30. (a)

In an RC phase shift oscillator, the frequency depends on R and C, not directly on the number of sections (though the number of sections affects phase and gain).

# 31. (c)

The beta cutoff frequency ( $f_B$ ) is the frequency at which the common-emitter current gain ( $\beta$ ) of a transistor amplifier drops to 0.707 (or –3 dB) of its mid-band value.  $\beta$ -cut off frequency for an amplifier is,

$$f_{\beta} = \frac{1}{2\pi r_e (C_T + C_D)}$$

$$\omega_{\beta} = \frac{1}{r_e (C_T + C_D)}$$

$$= \frac{1}{1500 \times (85 \times 10^{-12})}$$

$$= 0.0007874 \times 10^{10}$$

$$\omega_{\beta} = 7.8 \times 10^6 \text{ rad/s}$$

# 32. (a)

- Current-shunt feedback produces low input and low output impedance, not high.
- Current-series feedback is typically used for transconductance amplifiers, not transresistance.

# 33. (b)

- RC coupling is mainly for voltage amplification, not power amplification → Statement 2 is false.
- Direct-coupled amplifiers indeed suffer from thermal drift  $\rightarrow$  Statement 3 is true.

### 34. (c)

For a practical op-amp:

New bandwidth, 
$$BW_2 = BW_1(1 + A\beta)$$
  
Given:  $A = 10^6$ ;  $BW_1 = 10$  Hz;  $BW_2 = 100$  kHz  
 $\therefore 100 \times 10^3 = 10[1 + 10^6 \times \beta]$   
 $1 + 10^6\beta = 10^4$   
 $10^6\beta = 9999$   
 $\Rightarrow \beta = 9.999 \times 10^{-3}$ 

 $\therefore$  The percentage feedback,  $\beta = 0.99\%$  of negative feedback.

# 35. (b)

Adding a capacitor filter in a full-wave rectifier decreases the ripple factor.

## 36. (b)

In enhancement MOSFETs, the channel forms only after inversion caused by a sufficient positive or negative gate voltage (depending on MOSFET type).

# 37. (c)

A large time constant ensures the capacitor voltage does not discharge significantly during one cycle.

# 38. (a)

# Section B: Control Systems-1 + Microprocessors and Microcontroller-1

39. (c)

Given:

$$\frac{\omega(s)}{V_a(s)} = \frac{10}{1+10s} = \frac{10}{1+\tau s}$$

Thus, the open-loop time constant:

$$\tau = 10$$

For the closed-loop system:

$$\frac{\omega(s)}{R(s)} = \frac{\frac{10k_a}{1+10s}}{1+\frac{10k_a}{1+10s}} = \frac{10k_a}{1+10k_a+10s} = \frac{\frac{10k_a}{1+10k_a}}{1+\frac{10s}{1+10k_a}}$$

Thus, the new time constant is,

$$\tau_{\text{new}} = \frac{10}{1 + 10k_a}$$

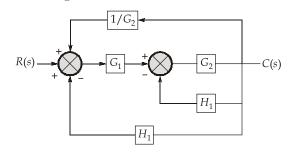
According to question,

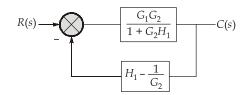
$$\frac{10}{1+10k_a} = \frac{1}{100} \times 10$$
$$1+10k_a = 100$$
$$k_a = 9.9$$

 $\Rightarrow$ 

40. (d)

Shifting takeoff point after Block  $G_2$ ,

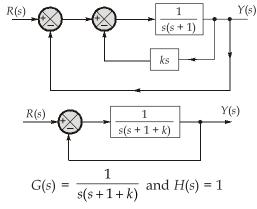




$$\frac{C(s)}{R(s)} = \frac{\frac{G_1 G_2}{1 + G_2 H_1}}{1 + \left(\frac{G_1 G_2}{1 + G_2 H_1}\right) \left(\frac{H_1 G_2 - 1}{G_2}\right)}$$

$$= \frac{G_1G_2}{1 + G_2H_1 + H_1G_1G_2 - G_1}$$
 
$$\frac{C(s)}{R(s)} = \frac{G_1G_2}{1 + G_1G_2H_1 + G_2H_1 - G_1}$$

#### 41. (a)



The characteristics equation,

$$1 + G(s)H(s) = 0$$

$$1 + \frac{1}{s(s+1+k)} = 0$$

$$\Rightarrow \qquad s(s+1+k) + 1 = 0$$

$$\Rightarrow \qquad s^2 + (k+1)s + 1 = 0$$

Comparing with the standard second-order form:

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0$$

We get, Natural frequency,  $\omega_n = 1$ 

It remains constant and does not depend of *k*.

$$2\xi\omega_n = k+1$$
$$\xi = \frac{k+1}{2}$$

Thus, the damping ratio depends on *k*:

Peak overshoot = 
$$M_p = e^{\frac{-2\pi}{\sqrt{1-\xi^2}}}$$
 and s on  $\xi$  which depends on  $k$ .

Since  $M_n$  depends on  $\xi$  which depends on k.

Hence the peak overshoot is influenced by the gain (k) of the tacho-generator.

#### 42. (d)

Closed-loop transfer function,

$$\frac{C(s)}{R(s)} = \frac{\frac{k}{(s+1)^2(s+2)}}{1 + \frac{k}{(s+1)^2(s+2)}}$$

$$\frac{C(s)}{R(s)} = \frac{k}{(s+1)^2(s+2)+k}$$

$$R(s) = \frac{1}{s}$$

Given,

Thus,

$$C(s) = \frac{k}{s[(s+1)^2(s+2)+k]}$$

From the final value theorem:

$$\lim_{s \to 0} sC(s) = 0.8 \text{ (given)}$$

$$\frac{k}{2+k} = 0.8$$

$$k = 8$$

 $\Rightarrow$  On solving,

# 43. (d)

Given the first two rows of Routh's table of a third order characteristics equation:

This is a special case of Routh's array because the first two rows having same elements so it will produce a row of zeros prematurely.

Since a row of zeros appears prematurely, form the auxiliary equation using the coefficients of  $s^2$  row:

 $\Rightarrow$ 

The coefficients 8 and 0 replace the zeros in the  $s^1$  row of the original table.

Since there are no sign changes in the first column of the entire Routh's tabulation, the equation (i) does not have any root in the right-half of the s-plane.

Solving the auxiliary equation, we get the two roots at s = j and s = -j which are also the roots of original characteristics equation. Thus, the equation has two roots on the  $j\omega$ -axis, and the system is marginally stable.

# 44. (d)

The characteristics equation is: 1 + G(s)H(s) = 0

$$1 + \left(\frac{k_p s + k_i}{s}\right) \left(\frac{1}{(s+2)(s+10)}\right) = 0$$
$$1 + \frac{k_p s + k_i}{s(s+2)(s+10)} = 0$$
$$s(s+2)(s+10) + k_p s + k_i = 0$$
$$s^3 + 12s^2 + (20 + k_p)s + k_i = 0$$

According to R-H array:

$$\begin{vmatrix} s^{3} & 1 & k_{p} + 20 \\ s^{2} & 12 & k_{i} \\ s^{1} & \frac{12k_{p} + 240 - k_{i}}{12} & 0 \\ s^{0} & k_{i} & 0 \end{vmatrix}$$

To ensure stability, all coefficients of the Routh array must be positive, which gives the conditions:

$$\frac{12k_p + 240 - k_i}{12} > 0 \text{ and } k_i > 0$$

$$k_p > \frac{k_i}{12} - 20 \text{ and } k_i > 0$$

or

# 45. (a)

Open-loop transfer function:

OLTF 
$$\Rightarrow$$
  $G(s) = \frac{ks}{(s-1)(s-4)}$ 

The characteristics equation is,

$$1 + G(s)H(s) = 0$$

$$\frac{ks}{(s-1)(s-4)} + 1 = 0$$

 $\Rightarrow$ 

$$ks + (s^2 - 5s + 4) = 0$$

$$k = \frac{-(s^2 - 5s + 4)}{s} = -\left[s - 5 + \frac{4}{s}\right]$$

For breakaway point:

$$\frac{dk}{ds} = 0$$

$$\frac{dk}{ds} = -\left[1 - 0 - \frac{4}{s^2}\right] = 0$$

We get,

$$s = \pm 2$$

Therefore valid breakaway point is s = 2

Now gain at s = 2 is

 $\Rightarrow k = \frac{\text{Product of distances from all the poles to breakaway point}}{\text{Product of distance from all the zeros to breakaway point}}$ 

Poles at : s = 1, 4Zero at : s = 0

Distances to s = 2:

- Pole at  $1 \rightarrow$  distance = 1
- Pole at  $4 \rightarrow$  distance = 2
- Zero at  $0 \rightarrow$  distance = 2

Gain, 
$$k = \frac{1 \times 2}{2} = 1$$

# 46. (a)

Given

$$G(s) = \frac{s^2 + 6s + 10}{s^2 + 2s + 2} = \frac{(s+3+i)(s+3-i)}{(s+1+i)(s+1-i)}$$

Since angle of arrival is calculated at zeros.

Here, zeros are

$$s = -3 - i$$

$$s = -3 + i$$

For calculation of angle of arrival at s = -3 + i, angle condition should be satisfied

i.e.,

$$\angle G(-3+i) = -180^{\circ}$$

$$\begin{split} -180^\circ &= \frac{\left[-3+i+3+i\right]\left[\theta_a\right]}{\left[-3+i+1+i\right]\left[-3+i+1-i\right]} \\ &= \frac{\left[2i\right]\left[\theta_a\right]}{\left[-2+2i\right]\left[-2\right]} \\ -180^\circ &= 90^\circ - \left[180^\circ - \tan^{-1}\frac{2}{2}\right] + 180^\circ + \theta_a \\ -180^\circ &= 135^\circ + \theta_a \\ \theta_a &= -225^\circ = \frac{-\pi}{4} \end{split}$$

 $\therefore \qquad \text{Thus, the other angle, } \theta_a = \frac{\pi}{4}$ 

 $\therefore$  Hence, Angle of arrival at its root loci =  $\pm \frac{\pi}{4}$ 

# 47. (b)

- Delay time  $(t_d)$  is the time required to reach at 50% of its final value by a time-response signal during its first cycle of oscillation.
- Settling time is the time required for the response to reach and stay within the specified range i.e either 3% or 5% of the final value.

Therefore, statements 1 and 3 are not correct.

# 48. (c)

CMP, CPI, and ORA instructions do not affect the accumulator.

ANI 5C instructions will change the contents of the accumulator.

(ANI is an AND operation with an 8-bit immediate data).

Accumulator AND 5C → Accumulator

# 49. (a)

The given program can be executed as

$$\begin{array}{c|c}
A & B \\
\hline
05 & 05 \\
+ 05 \\
+ 0A & 04 \\
\hline
0 & EH & 03 \\
\hline
11H & 02 \\
+ 02H & 01 \\
\hline
13H & 01
\end{array}$$

$$Z = 0; So JNZ PTR is true, and the loop repeats
$$\begin{array}{c}
1 & 1 & 1 \\
1 & 1 & 1 \\
1 & 1 & 1 \\
1 & 1 & 1 \\
1 & 1 & 1 \\
1 & 1 & 1 \\
1 & 1 & 1 \\
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# 50. (c)

• The DAD instruction performs double addition, in which contents of a register pair are added to the contents of the HL register pair, and again the result is stored in HL.

DAD 
$$R_P$$
  
HL  $\leftarrow$  (HL +  $R_P$ )

- The program counter is a 16-bit register and works as an instruction pointer since it holds the address of the next instruction to be fetched.
- In Indirect addressing, the address of the data is stored in the HL register pair, and the pair is mentioned in the instruction, as in MOV C, M.

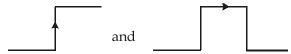
Thus, the HL register pair also acts as a data pointer.

# 51. (d)

- (i) IN and OUT instructions are used in I/O-mapped I/O schemes.
- (ii) In memory-mapped I/O schemes, I/O devices limit can exceed 256.

# 52. (c)

TRAP is a vectored interrupt with the highest priority, and it is both positive edge-triggered and level-triggered.



However, edge triggered is generally used for fast propagation of signals. So, the best option is (c).

## 53. (c)

1000 LXI SP, 27FF; SP = 27FF  
1003 CALL 1006; Decrements the top of stack by 2 
$$\rightarrow$$
 SP = 27FD

1006 POP H; Stores 06 in L and 10 in H

 $\rightarrow$  HL = 1006 and SP is incremented by 2 and SP = 27FF

Hence, both the given statements are correct.

$$\therefore$$
 SP = 27FF and HL = 1006

- 54. (d)
  - Memory-mapped I/O is a scheme in which an I/O device is mapped into the address space of the system, as if it were memory.

Hence, memory-related instructions are used for data transfer, thereby eliminating the need for dedicated I/O instructions.

- Since the total memory space is shared between memory and I/O devices, the actual memory space available for instructions and data is reduced.
- 55. (b)

A microprocessor does not have an on-chip main memory, and it does not need on-chip memory to run a program. However statement 2 is not correct explanation of statement 1. Statement 1 correctly states the difference between a microprocessor and a microcontroller.

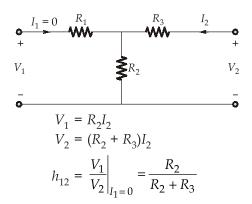
56. Root loci are symmetrical about the real axis ( $\sigma$ -axis).

# Section C : Network Theory-2 + Digital Circuits-2

57. (d)

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1 = 0}$$

when  $I_1 = 0$ :



Hence, option (d) is correct.

58.

The easiest way is to check the options.

$$Z_{11} = \frac{A}{C}$$
 and  $Z_{22} = \frac{D}{C}$ 

For the T-network:

$$Z_{11} = Z_A + Z_C$$

$$Z_{22} = Z_C + Z_B$$

Substituting the values:

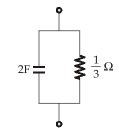
$$Z_{11} = \frac{A-1}{C} + \frac{1}{C} = \frac{A}{C}$$

$$Z_{22} = \frac{D-1}{C} + \frac{1}{C} = \frac{D}{C}$$

:. Option (a) is the correct option.

# 59. (a)

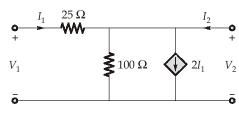
Input admittance



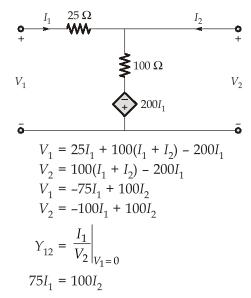
$$Y(s) = \frac{1}{R} + sC$$

$$Y(s) = 3 + 2s$$

# 60. (b)



By applying source transformation



so,

By equation (i)

٠.

$$V_2 = -100I_1 + 75I_1$$

$$V_2 = -25I_1$$

$$Y_{12} = \frac{I_1}{V_2} = -0.04 \text{ } \text{°S}$$

Alternate solution:

$$I_1 = \frac{V_1 - V_2}{25}$$

$$I_2 = 2I_1 + \frac{V_2}{10} + \frac{V_2 - V_1}{100}$$

Solving the above two equations, we get:

$$[Y] = \begin{bmatrix} 0.04 & -0.04 \\ 0.04 & -0.03 \end{bmatrix}$$

61. (b)

For a lattice circuit, the Z-parameters are:

$$[Z] = \begin{bmatrix} \frac{Z_A + Z_B}{2} & \frac{Z_B - Z_A}{2} \\ \frac{Z_B - Z_A}{2} & \frac{Z_A + Z_B}{2} \end{bmatrix}$$

Substituting the values:

$$Z_A = 3 + j4, Z = 3 - j4$$

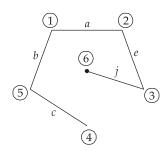
$$[Z] = \begin{bmatrix} \frac{(3+j4)+(3-j4)}{2} & \frac{(3-j4)-(3+j4)}{2} \\ \frac{(3-j4)-(3+j4)}{2} & \frac{(3+j4)+(3-j4)}{2} \end{bmatrix}$$

 $\Rightarrow$ 

$$[Z] = \begin{bmatrix} 3 & -j4 \\ -j4 & 3 \end{bmatrix}$$

62. (d)

Tree does not contain any loop,



63. (a)

$$H(s) = \frac{As + B}{s^2 + Cs + D}$$

At low frequency i.e. (s = 0)

$$H(0) = \frac{B}{D}$$

At high frequency i.e.  $(s \to \infty)$ 

$$H(\infty) = 0$$

The given transfer function represents a Low pass filter.

64. (b)

From the given graph,

The number of possible trees =  $N^{(N-2)}$ 

Where, N =Number of nodes in the graph.

Number of possible trees =  $4^{(4-2)} = 4^2 = 16$ 

65. (c)

From the figure, we get

$$J_A = K_A = 1;$$
  $J_B = K_B = \overline{Q_A}$ 

Clock	$J_A K_A$	$J_BK_B$	$Q_AQ_B$
0	11	11	00
1			11

So, the next state will be 11.

66. (d)

- When A = 1, then Q will be selected by the MUX and fed back to the D flip-flop, which gives the output Q again. So, at A = 1, it holds its state. When A = 0, then  $\overline{Q}$  will be selected by the MUX and fed back to the D flip-flop, and the output will be inverted.
- So, for A = 1 it holds the state and for A = 0 it interchanges the state i.e. for Q = 0 then it will go to Q = 1 and if Q = 1 then it will go to Q = 0.

Thus, option (d) is the correct option.

67. (b)

In standard TTL gates, the totem pole output stage is primarily used to decrease the output switching delay by actively sourcing and sinking current.

68. (c)

A 4-bit ripple counter will have a propagation delay of  $4t_{pd}$ , where  $t_{pd}$  is the propagation delay of one flip-flop. So, the counter will take a total time:

$$T = 4 t_{pd}$$
$$= 4 \times 12 \text{ nsec}$$
$$= 48 \text{ nsec}$$

69. (b)

MADE EASY

After 7-clock pulses, the content of the shift register will again become 1010.

70. (c)

HTL → High Noise Immunity

CMOS → High fan-out

 $I^2L \rightarrow$  Lowest product of power and delay

 $ECL \rightarrow Highest speed of operation.$ 

71. (b)

> Statements 1, 3 and 4 are correct. Statement 2 is incorrect, because the PLA, with both arrays programmable, is generally considered more flexible than the PAL. Hence, the correct option is (b).

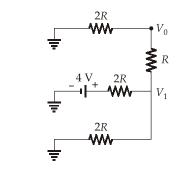
72. (d)

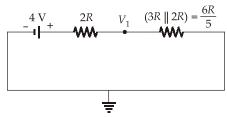
Maximum peak-to-peak ripple voltage

$$=\frac{FSV}{2^n-1}=\frac{5}{2^{10}-1}=\frac{5}{1023}=5.0 \text{ mV}$$

73. (a)

The circuit can be reduced as shown:





$$V_1 = \frac{\frac{6R}{5}}{\frac{6R}{5} + 2R} \times 4 = \frac{3}{2}V$$

$$V_0 = \frac{2R}{2R + R} \times \frac{3}{2} = 1 \text{ V}$$

74. (c)

Statements 1, 2 and 4 are correct. Statement 3 incorrectly describes the output dependency of the Mealy model, as the output is based on both the present state and the present input (which is the actual definition of the Mealy model).

75. (c)

Given, n = 4;  $t_{pd} = 30$  ns;  $t_s = 30$  ns

$$\begin{split} f_{\rm clk} &= ? \\ f_{\rm clk} &= \frac{1}{nt_{pd} + t_s} = \frac{1}{4 \times 30ns + 30ns} \\ &= 0.0066 \times 10^9 \ {\rm Hz} \\ &= 6.7 \ {\rm MHz} \end{split}$$

\_\_\_\_