DETAILED SOLUTIONS

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ESE 2026 : Prelims Exam
CLASSROOM TEST SERIES

ELECTRICAL ENGINEERING

Test 2

Section A : Electrical Circuits [All Topics]

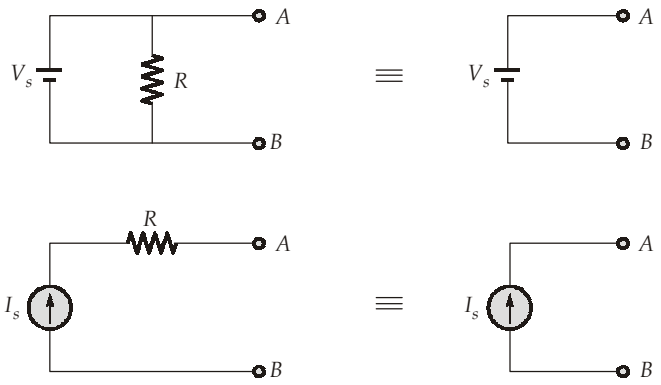
Section B : Digital Electronics + Microprocessors [All Topics]

ANSWER KEY

1. (c)	**16.** (d)	**31.** (c)	**46.** (c)	**61.** (d)
2. (d)	**17.** (a)	**32.** (b)	**47.** (d)	**62.** (d)
3. (d)	**18.** (c)	**33.** (c)	**48.** (c)	**63.** (c)
4. (c)	**19.** (b)	**34.** (d)	**49.** (c)	**64.** (a)
5. (a)	**20.** (a)	**35.** (b)	**50.** (b)	**65.** (d)
6. (c)	**21.** (c)	**36.** (c)	**51.** (c)	**66.** (b)
7. (c)	**22.** (a)	**37.** (b)	**52.** (b)	**67.** (b)
8. (a)	**23.** (d)	**38.** (d)	**53.** (a)	**68.** (d)
9. (c)	**24.** (c)	**39.** (a)	**54.** (a)	**69.** (d)
10. (b)	**25.** (a)	**40.** (c)	**55.** (a)	**70.** (b)
11. (d)	**26.** (c)	**41.** (b)	**56.** (d)	**71.** (b)
12. (c)	**27.** (c)	**42.** (a)	**57.** (c)	**72.** (a)
13. (a)	**28.** (c)	**43.** (c)	**58.** (c)	**73.** (d)
14. (c)	**29.** (b)	**44.** (c)	**59.** (a)	**74.** (b)
15. (b)	**30.** (c)	**45.** (d)	**60.** (c)	**75.** (c)

DETAILED EXPLANATIONS
Section A : Electrical Circuits

1. (c)



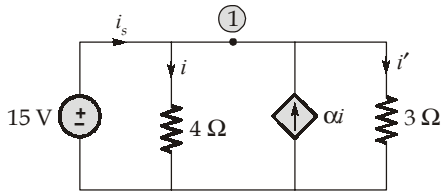
2. (d)

By inspection,

$$i = \frac{15}{4} = 3.75\ \text{A}$$

and the current through 3 Ω resistor is,

$$i' = \frac{15}{3} = 5\ \text{A}$$



Applying KCL at node (1), we get,

$$i_s + \alpha i = i + i'$$

$$\alpha = 1 + \frac{i'}{i} - \frac{i_s}{i}$$

As i_s can't be determined with the given data, α also can't be determined.

3. (d)

Let ϕ_1 = primary coil flux

ϕ_{12} = mutual flux

where $\phi_{12} = K\phi_1 = 0.5 \times \phi_1 = 0.7$

$\therefore$ $\phi_1 = \frac{0.7}{0.5} = \frac{7}{5} = 1.4\ \text{Wb}$

$\therefore$ The primary coil inductance,

$$L_1 = \frac{N\phi_1}{I_1} = \frac{250 \times \frac{7}{5}}{70}$$

$$= \frac{25}{5} = 5\ \text{H}$$

4. (c)

The impedance matrix is given by,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & -j\omega M \\ -j\omega M & j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Here $L_1 = 3$ H, $L_2 = 8$ H, and $M = 2$ H

From figure (B),

$$L_{eq} = L_1 + L_2 + 2M$$
$$= 3 + 8 + 4 = 15 \text{ H}$$

5. (a)

Let, v be the reference vector, it is clearly observed from the question that, i lags v by 30°.

Also, $$\frac{V_m}{I_m} = \frac{18}{2} = 9\ \Omega$$

$\therefore$ $$Z = \sqrt{R^2 + (\omega L)^2}$$

$$9^2 = R^2 + (\omega L)^2 \quad \text{...(i)}$$

$\because$ $$\frac{\omega L}{R} = \tan 30° = \frac{1}{\sqrt{3}}$$

$\therefore$ $$R = \sqrt{3}\,(\omega L) \quad \text{...(ii)}$$

From equation (i) and (ii),

$$9^2 = \left(\sqrt{3}\,\omega L\right)^2 + (\omega L)^2$$
$$2(\omega L) = 9$$
$$L = \frac{9}{2\times\omega} = \frac{9}{2\times 9} = 0.5 \text{ H} \qquad \because \omega = 9 \text{ rad/sec}$$

6. (c)

$$R = \frac{V^2}{P} = \frac{100\times 100}{10} = 1\ \text{k}\Omega$$

$\therefore$ $$I_R = \frac{V}{R} = \frac{100}{1000} = 0.1 \text{ A}$$

$\because$ $$I = \sqrt{I_R^2 + I_C^2}$$

$$0.3 = \sqrt{(0.1)^2 + (I_C)^2}$$

or, $$I_C = \sqrt{(0.3)^2 - (0.1)^2} = \frac{1}{10}\sqrt{3^2 - 1^2} = \frac{1}{10}\times 2\sqrt{2}$$

$$I_C = 0.2828$$

$\therefore$ $$C = \frac{I_C}{2\pi f \times V} = \frac{0.2828}{2\times 50\times\pi\times 100} = \frac{0.2828}{314\times 100} \approx 9\ \mu\text{F}$$

7. (c)

The internal impedance of the circuit is

$$Z_{in} = 3 + j4 - 8j = (3 - 4j)\ \Omega$$

The open circuit voltage across R_L

$$V_{oc} = 50\angle 0°\ \text{Volts}$$

As per the maximum power transfer theorem, for maximum power transfer,

or, $$R_L = |(3 - 4j)| = \sqrt{9+16} = 5\ \Omega$$

$$\therefore \quad |I| = \frac{50\angle 0°}{(3 - j4 + 5)} = \left|\frac{50\angle 0°}{8 - j4}\right|$$

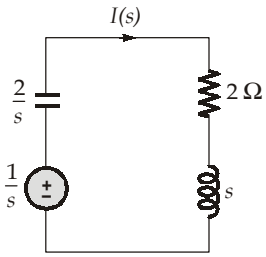
$$|I| = \frac{50\angle 0°}{\sqrt{64+16}} = \frac{50\angle 0°}{4\sqrt{5}}\ \text{A}$$

$$P_{max} = |I|^2 \cdot R_L = \left(\frac{50\angle 0°}{4\sqrt{5}}\right)^2 \times 5$$

$$= \frac{50\times 50}{16\times 5}\times 5 = \frac{2500}{16} = 156.25\ \text{W}$$

8. (a)

Taking the circuit in Laplace domain, we get,

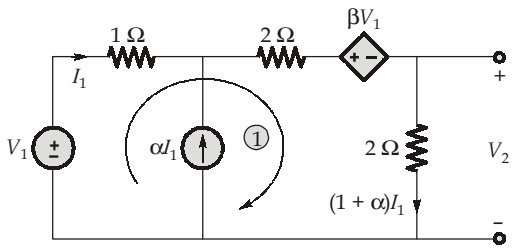


$$\therefore \quad I(s) = \frac{\frac{1}{s}}{2 + \frac{2}{s} + s} = \frac{1}{s^2 + 2s + 2} = \frac{1}{(s+1)^2 + 1}$$

By taking inverse Laplace transform,

$$i(t) = e^{-t}\sin t\, u(t)\ \text{A}$$

9. (c)



In loop (1), by applying KVL, we get,

$$V_1 = I_1 + 2(1+\alpha)I_1 + \beta V_1 + 2(1+\alpha)I_1$$

or $$(1-\beta)V_1 = (5+4\alpha)I_1$$

or $$V_1 = \frac{(5+4\alpha)}{(1-\beta)} I_1$$

Also, $$V_2 = (1+\alpha)I_1 \times 2 = 2(1+\alpha)I_1$$

$\because$ $$\frac{V_2}{V_1} = \frac{2(1+\alpha)(1-\beta)}{(5+4\alpha)}$$

$$\alpha = -\frac{3}{2} \Rightarrow 4\alpha = -6$$

So, $$\frac{V_2}{V_1} = \frac{2\left(1-\frac{3}{2}\right)}{(5-6)}(1-\beta) = (1-\beta)$$

$\therefore$ $$(1-\beta) = -\frac{1}{2}$$

or $$\beta = \frac{1}{2} + 1 = \frac{3}{2}$$

10. (b)

Total charge passed through the point is

$$q = \int_0^t i\,dt = \int_0^1 10t\,dt + \int_1^2 10\,dt$$

$$= 10\left[\frac{t^2}{2}\right]_0^1 + 10[t]_1^2 = 10\left[\frac{1}{2}\right] + 10[2-1] = 15\ \mu C$$

11. (d)

For maximum power transfer from the circuit of N to N_L , R_{Th} across the terminals should be 100 Ω.

Hence the voltage v should be

$$v = \frac{1}{2} \times 20 = 10\ V$$

Now, $$i = \frac{v}{R_{th}} = \frac{10}{100} = 0.1\ A$$

Applying KCL at top terminal of N_L we get,

$$0.1 = \frac{10}{200} + \frac{10 - v_a}{50}$$

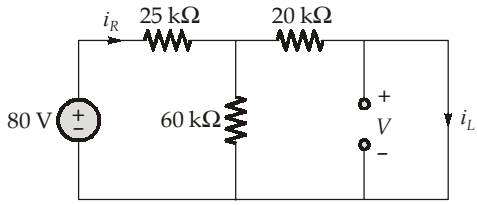
or $$0.1 = 0.05 + \frac{10 - v_a}{50}$$

$$10 - v_a = 0.05 \times 50$$

$$v_a = 10 - 2.5 = 7.5 \text{ V}$$

12. (c)

At $t = 0^-$, the equivalent circuit is shown below,



Here $$i_R(0^-) = \frac{80}{[25 + 20 \parallel 60]}\text{mA} = \frac{80}{40} = 2 \text{ mA}$$

Now, $$i_L(0^-) = \frac{60 \times 2}{(60 + 20)}\text{ mA} = 1.5 \text{ mA}$$

$\because$ $$i_L(0^+) = i_L(0^-) = 1.5 \text{ mA}$$

13. (a)

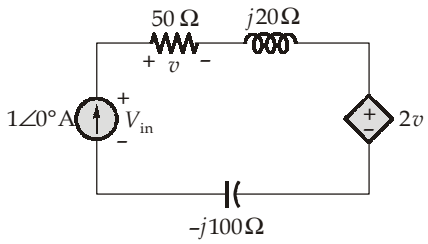
Inductive reactance,

$$X_L = j\omega L = j\,(10 \times 10^3)\,(2 \times 10^{-3}) = j\,20\ \Omega$$

Capacitive reactance, $$X_C = \frac{1}{j\omega C} = \frac{1}{j(10 \times 10^3)(1 \times 10^{-6})}$$

$$X_C = -j\,100\ \Omega$$

We can represent the circuit as shown below,



Here, $$V = 1\angle 0° \times 50 = 50 \text{ V}$$

Now, $$V_{in} = 1\angle 0° \times (50 + j20 - j100) + 2 \times 50$$

or, $$V_{in} = 50 - j80 + 100 = (150 - j\,80) \text{ V}$$

Therefore, $$Z_{in} = \frac{V_{in}}{1\angle 0°} = (150 - j80)\,\Omega$$

14. (c)

Using the dot polarities given in figure,

For coil 1 : $L_1 - M_{12} - M_{13} = 4 - 1 - 3 = 0 = L_{eq1}$

For coil 2 : $L_2 - M_{12} + M_{23} = 5 - 1 + 2 = 6 = L_{eq2}$

For coil 3 : $L_3 - M_{13} + M_{23} = 6 - 3 + 2 = 5 = L_{eq3}$

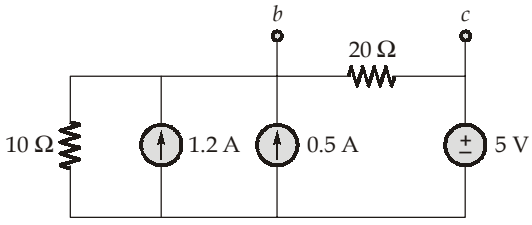
Effective inductance = $L_{eq1} + L_{eq2} + L_{eq3} = 0 + 6 + 5 = 11$ H

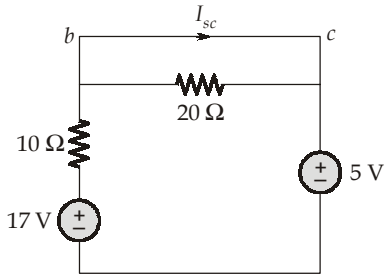
15. (b)

Reciprocity theorem is not applicable to the circuit with time varying elements and also not applicable to the circuit with dependent sources.

16. (d)

In order to obtain Norton's equivalent across the terminals '*b*' and '*c*' the circuit can be redrawn as





$$I_{SC} = \frac{17-5}{10} = 1.2 \text{ A}$$

$$R_{Th} = 10 \,||\, 20 = 6.67\ \Omega$$

17. (a)

Initially, $C_1 = 5\ \mu F, \quad Q_1 = 17\ \mu C$

$C_2 = C\ \mu F, \quad Q_2 = 0$

$Q_T = Q_1 + Q_2 = 17\ \mu C$

When C_1 is connected to C_2 parallel, charge transferred from C_1 to C_2. However the total charge remain equal to 17 μC.

$$V_1 = V_2$$

$$\frac{Q_1}{C_1} = \frac{Q_2}{C_2}$$

$$\frac{10}{5} = \frac{7}{C}$$

$$C = \frac{7}{2} = 3.5\ \mu F$$

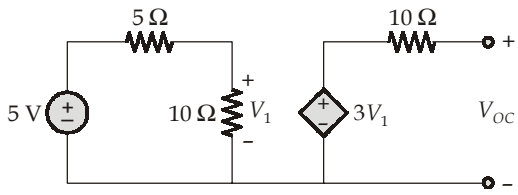
18. (c)

The degree of each node in a fully connected graph is equal to $(n - 1)$.

19. (b)

From the given circuit,

$$V_1 = 5\times\frac{10}{15} = \frac{10}{3}\text{V}$$



$$V_{OC} = 3V_1 = 10\text{ V}$$

$$I_{SC} = \frac{10}{10} = 1\text{A}$$

$$R_{\text{Th}} = \frac{V_{OC}}{I_{SC}} = 10\ \Omega$$

$$P_{\max} = \frac{V_{\text{Th}}^2}{4R_{\text{Th}}} = \frac{V_{\text{OC}}^2}{4R_{\text{Th}}} = \frac{10^2}{4\times10} = 2.5\text{ W}$$

20. (a)

Here $v_0(t)$ is negative means current direction is opposite in the coils,

$$v_0(t) = \frac{Mdi_1(t)}{dt}$$

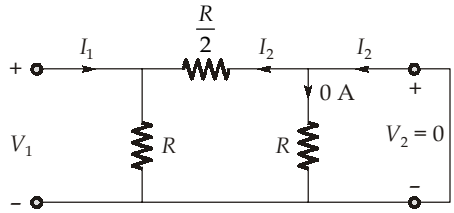
$$M = \frac{|v_0(t)|}{\left|\frac{di_1(t)}{dt}\right|} = \frac{40}{16} = 2.5\text{ H}$$

21. (c)

Using transmission parameters,

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2$$

$$\therefore \quad D = \left.\frac{-I_1}{I_2}\right|_{V_2=0}$$



$$I_2 = -I_1 \times \frac{R}{R+\frac{R}{2}} = -I_1 \times \frac{2}{3}$$

$$D = \left.\frac{-I_1}{I_2}\right|_{V_2=0} = \frac{3}{2}$$

22. (a)

For parallel RLC circuit,

$$Q = R\sqrt{\frac{C}{L}}$$

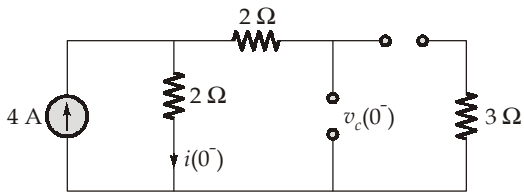
$$\xi = \frac{1}{2Q} = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

$\because \xi = 1$ for critically damped response

$$R = \frac{1}{2}\sqrt{\frac{L}{C}} = \frac{1}{2}\sqrt{\frac{8}{2}} = 1\ \Omega$$

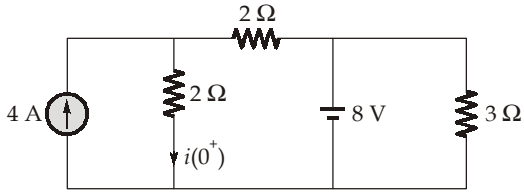
23. (d)

At $t = 0^-$



$$v_c(0^-) = v_c(0^+) = 8\ \text{V}$$

At $t = 0^+$



Using superpostion theorem,

$$i(0^+) = \frac{4\times 2}{2+2} + \frac{8}{2+2} = 4\ \text{A}$$

24. (c)

Using superposition theorem,

$$P = \left[\pm\sqrt{P_1} \pm \sqrt{P_2} + \pm\sqrt{P_3}\right]^2$$

$$= \left[\pm\sqrt{30} \pm \sqrt{120} \pm \sqrt{270}\right]^2$$

$$P_{max} = \left[\sqrt{30}+\sqrt{120}+\sqrt{270}\right]^2$$

$$= \left(\sqrt{30}\right)^2\left[1+\sqrt{4}+\sqrt{9}\right]^2$$

$$= 30[1+2+3]^2 = 1080 \text{ W}$$

25. (a)

$$I_1 = \frac{V}{Z_1} = \frac{V}{10+j5} = |I_1|\angle\phi_1$$

$$I_2 = \frac{V}{Z_2} = \frac{V}{8+j6} = |I_2|\angle\phi_2$$

$$I = I_1 + I_2 = |I|\angle\phi$$

$$\phi_1 = \phi_v - \tan^{-1}\left(\frac{5}{10}\right) = \phi_v - \tan^{-1}(0.5)$$

$$\phi_2 = \phi_v - \tan^{-1}\left(\frac{6}{8}\right) = \phi_v - \tan^{-1}(0.75)$$

$\therefore \quad \phi_1 > \phi_2$

$\Rightarrow I_1$ leads I_2

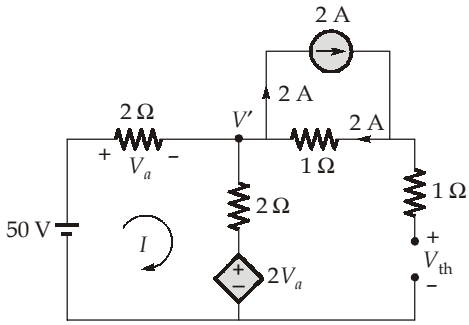
Resultant phase ϕ lies between ϕ_1 and ϕ_2

$$\phi_2 < \phi < \phi_1$$

Hence, I leads I_2 and lag behind I_1.

26. (c)

Disconnecting the load resistance, we calculate the Thevenin voltage across the open circuit terminals.



$$2I = V_a$$

by using KVL, $\quad 50 - 2V_a = 4I$

$$50 = 4I + 4I$$

$$8I = 50$$

$$I = \frac{50}{8} = \frac{25}{4}\text{A}$$

$$V' = 2I + 2V_a = 2I + 4I = 6I$$

$$V' = \frac{25}{4} \times 6 = 37.5 \text{ volt}$$

$$V_{th} = 2 + V' = 2 + 37.5$$

$$V_{th} = 39.5 \text{ V}$$

27. (c)

Given, $V_1 = 5V_2 - 3I_2$

$I_1 = 6V_2 - 2I_2$

From the given two-port network,

We can write, $V_2 = -5I_2$

Substituting the value of V_2 in the given equations,

$$V_1 = 5(-5I_2) - 3I_2 = -28I_2$$

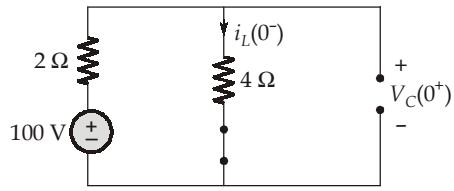
$$I_1 = 6(-5I_2) - 2I_2 = -32I_2$$

$\therefore$ Input impedance, $Z_{in} = \frac{V_1}{I_1} = \frac{-28I_2}{-32I_2} = \frac{7}{8}\Omega$

28. (c)

The circuit is in steady state at $t \to 0^-$

At $t = 0^-$, the capacitor is open-circuit and inductor is short-circuit. Hence,



$$i_L(0^-) = \frac{100}{6} = \frac{50}{3} \text{A}$$

Using voltage division, $V_C(0^-) = \frac{4}{6} \times 100 = \frac{200}{3} \text{V}$

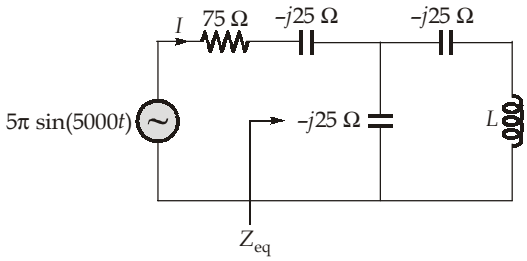
Capacitor can charge upto $\frac{200}{3}$ volts.

Charge stored by capacitor, $Q = CV$

$$Q = 3 \times 10^{-6} \times \frac{200}{3}$$

$$Q = 200 \ \mu\text{C}$$

29. (b)



According to the question, I should be zero, then Z_{eq} should be infinite

$$Z_{eq} = \frac{(j\omega L - j25)(-j25)}{(j\omega L - j25 - j25)} = \frac{1}{0} = \infty$$

$\therefore \quad j\omega L - j25 - j25 = 0$

$$j\omega L = j50$$

$$\omega L = 50$$

$$\omega = 5000 \text{ rad/sec (given)}$$

$$L = \frac{50}{5000} = 10 \text{ mH}$$

30. (c)

We have, $V = -2\sin(314t + 10°) = 2\cos(314t + 10° + 90°)$

$$V = 2\cos(314t + 100°) \text{ Volt}$$

$$V = 2\angle 100° \text{ Volt}$$

Now, $I = 5\cos(314t + 160°) = 5\angle 160° \text{ Amp}$

Here ; $\theta = \theta_V - \theta_I = 100 - 160° = -60°$

Power factor $\Rightarrow \quad \cos\theta = \cos(-60°) = 0.5\text{(leading)}$

Note: Leading because current is leading with voltage.

31. (c)

Symmetric conditions for 2-port parameters:

- $Z_{11} = Z_{22}$
- $Y_{11} = Y_{22}$
- $h_{11}\, h_{22} - h_{12}\, h_{21} = 1$
- $g_{11}\, g_{22} - g_{12}\, g_{21} = 1$
- $A = D$

Reciprocal conditions for 2-port parameters:

- $Z_{12} = Z_{21}$
- $Y_{12} = Y_{21}$
- $h_{12} = -h_{21}$
- $g_{12} = -g_{21}$
- $AD - BC = 1$

32. (b)

In a complete graph, each pair of graph vertices is connected by an edge. Hence, the number of edges in complete graph is ${}^{n}C_{2}$.

33. (c)

Tellegen's theorem:

- It is applicable to any network (i.e. linear, non-linear, unidirectional, time variant, time invariant).
- It is based on law of conservation of energy.

34. (d)

For *R*-*L*-*C* series circuit:

$$\text{Quality factor } (Q) = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{2}\sqrt{\frac{10^{-4}}{10^{-4}}} = \frac{1}{2}$$

$$\text{Damping ratio } (\xi) = \frac{1}{2Q} = 1$$

If $\xi = 1$, then system is critically damped.

Note:

- For $0 < \xi < 1 \Rightarrow$ system is underdamped.
- For $\xi > 1 \Rightarrow$ system is overdamped.
- For $\xi = 0 \Rightarrow$ system is undamped.

35. (b)

Hybrid parameters are defined as:

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0} \Rightarrow \text{Reverse voltage gain}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0} \Rightarrow \text{Forward current gain}$$

36. (c)

A dual network is a concept in electrical engineering where one circuit's mesh equations are the same as its counterpart is nodal equations, with variable like voltage and current interchanged.

37. (b)

$$\text{Number of branches} = 10$$
$$\text{Number of nodes} = 7$$
$$\text{Number of loops} = B - N + 1$$
$$= 10 - 7 + 1 = 4$$

38. (d)

Statement 1 is wrong.

39. (a)

When S_1 is opened and S_2 is closed at steady state let the voltage across capacitor combination is V_C

Using conservation of charge

$$V_C \cdot C_1 + V_C \cdot C_2 = V_{C1}(0^+) \times C_1$$
$$V_C[1 + 2] = 6 \times 1$$
$$V_C = 2\ \text{V}$$

40. (c)

At $\omega \to \infty$, Capacitor $\to$ Short circuited

$$\frac{V_0}{V_i} = 0$$

At $\omega \to 0$, Capacitor $\to$ Open circuited

$$\frac{V_0}{V_i} = 0$$

So frequency response of the circuit will be bandpass filter.

41. (b)

In a series resonant circuit, the inductive reactance and capacitive reactance cancel each other. As a result:

- The circuit behaves like a purely resistive circuit.
- The power factor becomes unity.
- The impedance is minimum, so the current is maximum.

42. (a)

When two inductors L_1 and L_2 are connected in parallel and their magnetic field oppose each other,

$$L_{eq} = \frac{L_1L_2 - M^2}{L_1 + L_2 + 2M}$$

43. (c)

At half power frequencies the current is $\frac{1}{\sqrt{2}}$ times the resonant current.

44. (c)

Statement-I is correct as,

$$Q = \frac{\omega_0}{\text{B.W.}}$$

Whereas for statement-II is incorrect.

45. (d)

Reciprocity does not guarantee symmetricity.

Section B : Digital Electronics + Microprocessors

46. (c)

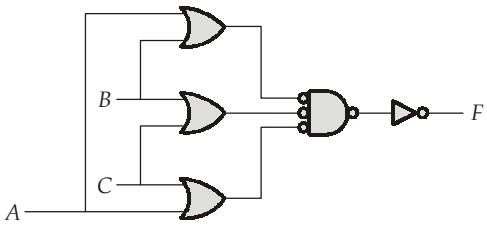
$$(64)_8 = 6 \times 8 + 4 = (52)_{10}$$

$$(-64)_{10} + (52)_{10} = (-12)_{10}$$

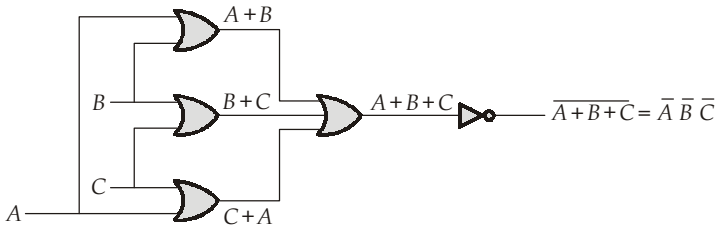
thus $X = -12$

47. (d)

The circuit can be redrawn as,



which can be redrawn as,



48. (c)

$$f = \bar{C}\bar{D} + \bar{A}BC\bar{D} + CD\bar{A}$$

AB \ CD	00	01	11	10
00	1	0	1	0
01	1	0	1	1
11	1	0	0	0
10	1	0	0	0

thus, $F = \bar{A}BC + \bar{A}CD + \bar{C}\bar{D}$

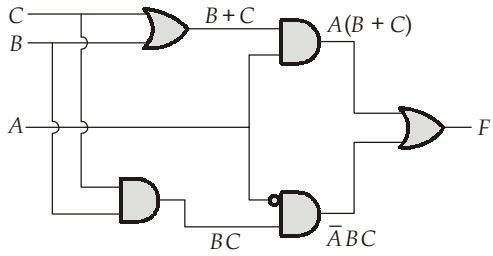
but F can also be expressed as

$$F = \bar{A}BC + \bar{A}CD + \bar{C}\bar{D}(A + \bar{A})$$

$$= \bar{A}BC + \bar{A}CD + \bar{A}\bar{C}\bar{D} + A\bar{C}\bar{D}$$

49. (c)

The circuit can be redrawn as,



Thus, $F = A(B+C)+\bar{A}BC = AB+AC+\bar{A}BC = B(A+\bar{A}C)+AC$

$= B(A + C) + AC = AB + AC + BC$

50. (b)

Given the initial state to be zero, thus the state sequence table can be given as

Q_n	$J = (1)$	$K = (\bar{Q}_n)$	Q_{n+1}
0	1	1	1
1	1	0	1
1	1	0	1
⋮	⋮	⋮	⋮

51. (c)

STAX R_p, LDAX R_p instructions should be used only with BC and DE register pairs.

In option (c), LDAX is used with HL pair, which is invalid.

52. (b)

AB \ CD	00	01	11	10
00	×	1	1	×
01		×	1	
11			1	
10			1	

$\therefore \quad Y = \bar{A}\bar{B}+CD$

53. (a)

$\because \quad X_1 = Y_1$

$X_2 = Y_1 \oplus Y_2$

54. (a)

For a JK-flip-flop to function as *T*-flip-flop, $J = K$. If the flip-flop belongs to a *TTL* family, then $J = K = 1$.

55. (a)

Master-slave configuration is used in flip-flops to store one bit of information.

56. (d)

Half adder output is

$$\begin{aligned} \text{Sum} &= A \oplus B \\ \text{Carry} &= AB \\ f &= \bar{C}(A \oplus B) + ABC \\ &= \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\ f &= \Sigma m(2, 4, 7) \end{aligned}$$

57. (c)

$$\% \text{ Resolution} = \frac{1}{2^N - 1} \times 100\% = \frac{1}{2^4 - 1} \times 100\% = \frac{100}{15} = 6.67\%$$

58. (c)

The base of the number is 7.

$\therefore$ It can use digits from 0 to 6.

Hence, using 9 is invalid for this number system.

59. (a)

Six bit representation of +10 is 001010

Taking 2's complement $\rightarrow$ 110101

$$\begin{array}{r} +1 \\ \hline 110110 \end{array}$$

60. (c)

ECL is a non-saturated logic family.

62. (d)

For 4-bit Johnson counter, state table is as below:

Clock	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

$\therefore$ Invalid state is 1001.

63. (c)

0	1	1	0	CLK pulse
1	1	0	1	(1)
1	0	1	1	(2)
0	1	1	0	(3)

64. (a)

MOD-1000 ripple-up counter is constructed using 10-flip flops.

The MSB i.e., Q_9 will have 50% duty cycle if it is MOD-1024 ripple up counter.

But for MOD-1000, Q_9 will be '0' for 512 clock pulses and will be '1' for 488 clock pulses.

Hence, $$\text{Duty cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$\%\,\text{Duty cycle} = \frac{488\,T_{CLK}}{1000\,T_{CLK}} \times 100 = 48.8\%$$

65. (d)

A compiler converts the entire source code into machine code before execution, making the program run faster compared to an interpreter.

66. (b)

The instruction LHLD address loads the contents of the specified address into register L and the next address into register H. Hence, LHLD 2050H → L ← [2050H], H ← [2051H].

67. (b)

$$\text{Total capacity} = \text{Tracks} \times \text{Sectors/track} \times \text{Byte}$$

$$256000 = 100 \times N \times 256$$

$$N = 10$$

Hence, the disk has 10 sectors per track.

68. (d)

Some instructions do not require address of the operand as they directly operate on the content of the accumulator.

Ex RLC, CMA

69. (d)

LXI H, XX 65H

Flag resister value unknown

MVI M, FFH

INR M

Value of M is 00H

$\Rightarrow$ $Z = 1$

INR does not affect the carry flag.

70. (b)

Format of PUSH instruction is PUSH register pair/PSW.

PUSH PSW copy content of Accumulator and flag on to stack.

71. (b)

In the 8085 microprocessor, the lower 8-bits of the address bus are shared with the data bus. These lines are used for address during the first part of the cycle and for data during the second part-hence, they are multiplexd.

73. (d)

- For RLC and RRC instructions, final result does not depend on initial state of CY.
- For RAL and RAR instructions, final result depends on initial state of CY.
- RLC, RRC, RAL, RAR all these instructions will affect CY.

75. (c)

By using the combination of NAND and NOR gates, we can realize any Boolean function but not with the minimum number of logic gates. Hence. Statement(II) is incorrect.

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