DETAILED SOLUTIONS

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ESE 2025 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 6

Section A : Electronic Devices & Circuits + Analog Circuits

Section B : Control Systems-1 + Microprocessors and Microcontroller-1

Section C : Network Theory-2 + Digital Circuits-2

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2.	(d)	17.	(c)	32.	(d)	47.	(c)	62.	(c)
3.	(d)	18.	(d)	33.	(d)	48.	(d)	63.	(d)
4.	(a)	19.	(c)	34.	(d)	49.	(b)	64.	(c)
5.	(c)	20.	(a)	35.	(a)	50.	(c)	65.	(d)
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9.	(a)	24.	(a)	39.	(c)	54.	(c)	69.	(a)
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DETAILED EXPLANATIONS
Section A : Electronic Devices & Circuits + Analog Circuits

1. (c)

The forward current in a p-n junction diode is given by

$$I_D = I_0\left(e^{\frac{V_D}{\eta V_T}} - 1\right) \approx I_0 e^{\frac{V_D}{\eta V_T}}$$

where I_0 is the reverse saturation current, η is the ideality factor and V_D is the forward voltage across the diode.

We have, $$V_D = \eta V_T \ln\left(\frac{I_D}{I_0}\right)$$

For 'Ge' diode, $V_G = V_T \ln\left(\frac{I}{I_G}\right)$ → (i) ($\because \eta = 1$)

For 'Si' diode, $V_S = \eta V_T \ln\left(\frac{I}{I_S}\right)$ → (ii) ($\because$ Ideality factor is η)

By applying KVL,

$$V = V_G + V_S$$
$$= V_T \ln\left(\frac{I}{I_G}\right) + \eta V_T \ln\left(\frac{I}{I_S}\right) \quad (\because \text{Using equations (i) and (ii)})$$
$$= V_T \ln\left(\frac{I}{I_G}\right) + V_T \ln\left(\frac{I}{I_S}\right)^{\eta}$$
$$= V_T \ln\left(\frac{I^{\eta+1}}{I_G I_S^{\eta}}\right)$$

$$\Rightarrow \quad \frac{V}{V_T} = \ln\left(\frac{I^{\eta+1}}{I_G I_S^{\eta}}\right) \quad \Rightarrow \quad I^{\eta+1} = I_G I_S^{\eta}\, e^{V/V_T}$$

2. (d)

Given, $I_{C1} = 0.5$ mA when $V_{CE1} = 5$ V

$I_{C2} = 1$ mA when $V_{CE2} = 20$ V

Due to early effect, collector current increases with increasing V_{CE}, for a fixed value of V_{BE}, given by

$$I_{C2} = I_{C1}\left[1 + \frac{\Delta V_{CE}}{V_A}\right]$$
$$1 = 0.5\left[1 + \frac{15}{V_A}\right]$$

$$2 = 1 + \frac{15}{V_A}$$

$\therefore$ $V_A = 15\ \text{V}$

3. (d)

We know,

Reverse saturation current $\propto$ Area

For discrete bipolar transistors, $I_{S_{dis}} \propto A_{dis}$

For integrated devices, $I_{S_{int}} \propto A_{int}$

$$\therefore \quad \frac{I_{S_{int}}}{I_{S_{dis}}} = \frac{A_{int}}{A_{dis}}$$

$$\Rightarrow \quad \frac{I_{S_{int}}}{I_{S_{dis}}} = \frac{0.8 \times 0.4}{100 \times 100} = 32 \times 10^{-6}$$

4. (a)

1. **Flatband:** For $V = 0$, all bands remain flat and the semiconductor and its majority and minority carriers are in thermal equilibrium. The energy band diagram 'A' represents the flatband condition.
2. **Accumulation:** When a positive voltage is applied at the contact, there is an accumulation of the majority carriers (electrons) near the interface. The conduction band E_c bends down towards the Fermi level E_f that is set constant in the semiconductor where no current flows. The energy band diagram 'B' represents the Accumulation condition.
3. **Depletion:** Under a small negative voltage, the majority carriers are repelled from the interface, involving that the bands are bend up. The intrinsic energy E_i gets closer to E_f. The energy band diagram 'C' represents the Depletion condition.
4. **Inversion:** When further increasing the negative voltage, this bending continues and once E_i crosses E_f, the minority carriers (holes) exceed the majority carriers at the interface. Hence, this case is called inversion, as the interface is inverted. The energy band diagram 'D' represents the Inversion condition.

5. (c)

Given, $\left(\frac{\sigma_p}{\sigma_n}\right) = \frac{1}{2}$

$$\left(\frac{L_p}{L_n}\right) = \frac{5}{2}$$

The hole diffusion current, $I_p \propto \frac{1}{L_p \sigma_n}$

The electron diffusion current, $I_n \propto \frac{1}{L_n \sigma_p}$

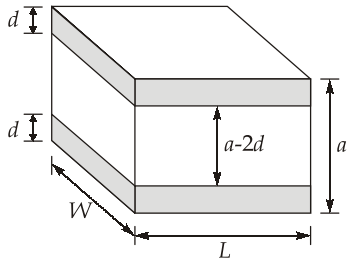
The ratio of Hole diffusion current to electron diffusion current crossing the junction is given by,

$$\frac{I_p}{I_n} = \left(\frac{\sigma_p}{\sigma_n}\right)\times\left(\frac{L_n}{L_p}\right)$$

$$= \left(\frac{1}{2}\right)\times\left(\frac{2}{5}\right) = \frac{1}{5} = 0.2$$

6. (b)

Given, $d = 0.5\ \mu m$



$\therefore$ Channel area $= (W\times(a-2d)) = (100\times10^{-6})\left[(5\times10^{-6})-(2\times0.5\times10^{-6})\right]$

$\Rightarrow$ Channel area $= 4\times10^{-10}\ m^2$

$$\text{Channel resistance, } R = \frac{\rho L}{A} = \frac{L}{N_D\mu_n qA}$$

$$= \frac{(16\times10^{-6})}{10^{22}\times0.5\times1.6\times10^{-19}\times4\times10^{-10}} = 50\ \Omega$$

7. (c)

We know that, for a JFET, $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$

Given $V_{GS} = \frac{V_P}{2}$ then,

$$I_D = I_{DSS}\left[1-\frac{(V_P/2)}{V_P}\right]^2$$

$$I_D = I_{DSS}\left[1-\frac{1}{2}\right]^2 = \frac{I_{DSS}}{4}$$

Thus, option (c) is correct.

8. (b)

We know that, for a pnp transistor,

$$\tau_t = \frac{W_B^2}{2D_P}$$

where, τ_t = Base Transit time i.e. Time taken by holes to travel from emitter junction to collector junction

W_B = Width of base region

D_P = Diffusion constant of holes in base region

On substituting the given data, we get

$$50 \times 10^{-9} \text{ sec} = \frac{(10\times10^{-6})^2 (m^2)}{2D_P}$$

$$D_P = \frac{(10\times10^{-6})^2}{2\times50\times10^{-9}}\left(\frac{m^2}{\text{sec}}\right) = \frac{100\times10^{-12}}{100\times10^{-9}}\left(\frac{\text{m}^2}{\text{sec}}\right)$$

$$D_P = 10^{-3} \text{ m}^2/\text{sec}$$

$$D_P = (10^{-3}) \times 10^4 \text{ cm}^2/\text{sec}$$

$$D_P = 10 \text{ cm}^2/\text{sec}$$

9. (a)

We know that,

Width of depletion region, $W = K\sqrt{V_{bi} + V_R}$,

where V_{bi} is the built-in voltage and V_R is the applied reverse bias voltage

Given: For $V_{R1} = 1.2$ V; $W_1 = 2$ μm and

For $V_{R2} = 7.2$ V; $W_2 = 4$ μm

$\therefore$

$$\frac{W_1}{W_2} = \frac{K\sqrt{V_{bi} + V_{R1}}}{K\sqrt{V_{bi} + V_{R2}}}$$

$$\frac{2}{4} = \frac{K\sqrt{V_{bi} + 1.2}}{K\sqrt{V_{bi} + 7.2}}$$

$$\frac{1}{2} = \frac{\sqrt{V_{bi} + 1.2}}{\sqrt{V_{bi} + 7.2}}$$

$$\frac{1}{4} = \frac{V_{bi} + 1.2}{V_{bi} + 7.2}$$

$$V_{bi} + 7.2 = 4V_{bi} + 4.8$$

$$3V_{bi} = 2.4$$

$$V_{bi} = 0.8 \text{ Volt}$$

10. (b)

- When JFET is used as a voltage variable resistor, it operates in the Ohmic Region and the resistance of the JFET can be varied by adjusting the gate-to-source voltage (V_{GS}).
- As V_{DS} is increased, the depletion regions on both sides in a JFET meet near the drain which essentially pinch off the channel. When this happens, current I_D is saturated and does not increase significantly with further increase in V_{DS}.

Thus, only statement 2 is correct.

11. (c)

Given, $V_{oc} = 0.8\ V$

$I_{sc} = 100\ mA$

$P = 50\ mW/cm^2$

$A = 5\ cm^2$

Fill factor = 0.5

We have, $\text{Fill factor} = \dfrac{P_{out(max)}}{V_{oc} \times I_{SC}}$

$\Rightarrow$ Maximum output power, $P_{out(max)}$ = Fill factor x V_{oc} x I_{SC}

$\therefore \quad \eta_{max} = \dfrac{P_{out(max)}}{P_{in}} \times 100$

$$= \frac{\text{Fill factor} \times V_{oc} \times I_{sc}}{\text{Total power per unit area} \times \text{Total area}} \times 100$$

$$= \frac{0.5 \times 0.8 \times 100 \times 10^{-3}}{50 \times 10^{-3} \times 5} \times 100$$

$\Rightarrow \quad \eta_{max} = 16\%$

12. (b)

Built-in potential, ψ_0 = Area of electric field profile in the depletion region

$$= \left[(0.5 \times 10^6) \times 1 \times 10^{-6}\right] + \left[\frac{1}{2} \times 10^{-6} \times 0.5 \times 10^6\right]$$

$= 0.5 + 0.25$

$= 0.75\ V$

13. (b)

$$\frac{L_p}{L_n} = \frac{\sqrt{D_p \tau_p}}{\sqrt{D_n \tau_n}} = \sqrt{\frac{5 \times 10^{-4} \times 0.1 \times 10^{-6}}{20 \times 10^{-4} \times 10 \times 10^{-6}}}$$

$$\Rightarrow \quad \frac{L_p}{L_n} = \sqrt{\frac{0.5}{200}} = \sqrt{25 \times 10^{-4}} = 5 \times 10^{-2} = 0.05$$

14. (a)

Given, $\tau_r = 50\ ns$

$\tau_{nr} = 100\ ns$

$$\eta_{int} = \frac{\tau}{\tau_r} \times 100 = \frac{\left[\dfrac{\tau_{nr}\tau_r}{\tau_{nr} + \tau_r}\right]}{\tau_r} \times 100$$

$$\Rightarrow \quad \eta_{int} = \frac{\tau_{nr}}{\tau_{nr} + \tau_r} \times 100 = \frac{100}{100 + 50} \times 100$$

$= 66.67\%$

15. (c)

Linearity is the main characteristics of the photodiode. The photodiodes are generally designed to have a linear response to incident light intensity, within their operating range i.e. the output current is directly proportional to the light intensity.

16. (b)

We know, $$\beta = \frac{\alpha}{1-\alpha}$$

$$\Rightarrow \quad \partial\beta = \frac{\partial\alpha}{(1-\alpha)^2}$$

$$\Rightarrow \quad \frac{\partial\beta}{\beta} = \frac{1}{1-\alpha}\cdot\frac{\partial\alpha}{\alpha}$$

$$\Rightarrow \quad \left(\frac{\partial\beta}{\beta}\right)\% = \left(\frac{1}{1-0.8}\right)\times(0.008\%)$$

$$= 5 \times 0.008\% = 0.04\%$$

17. (c)

- Einstein equation relates carrier diffusion constant and mobility,

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$$

- Diffusion current is proportional to the carrier concentration gradient,

$$J_n = qD_n\frac{dn}{dx}$$

- The continuity equation is a differential equation that governs the relation of the carrier concentration, both with time and distance.

$$\frac{\partial p}{\partial t} = \frac{p_0 - p}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{q\partial x}$$

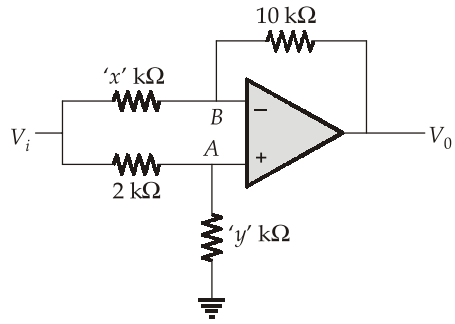
- Poisson's Equation relates spatial variation of the electric field intensity with the space charge density,

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s}$$

18. (d)

Except photodiode, all the given diodes works under forward biased condition.

19. (c)



Now, using voltage division rule,

$$\text{Voltage, } V_A = \frac{V_i \times y}{y+2} \qquad \text{...(i)}$$

Using virtual short concept,

$$V_A = V_B = \frac{V_i y}{2+y}$$

Now, on applying KCL at B, we get

$$\frac{V_B - V_i}{'x'\,k} + \frac{V_B - V_0}{10\,k} = 0$$

$$\frac{\frac{V_i y}{2+y} - V_i}{x\,k} + \frac{\frac{V_i y}{(2+y)} - V_0}{10k} = 0$$

As $V_0 = 0$, then

$$\frac{V_i y - V_i(2+y)}{(2+y)x} + \frac{V_i y}{(2+y)10} = 0$$

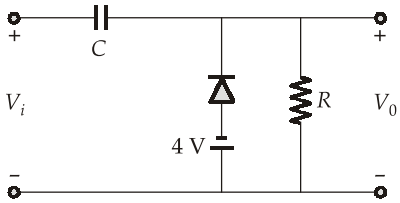
$$\frac{-2V_i}{x} = \frac{-V_i y}{10}$$

$$xy = 20$$

From the given options, $x = 2.5$ and $y = 8$ satisfies the above relation.

20. (a)

Considering option (a),



For $V_i < -4$ V, diode conducts and capacitor charges as

$$V_c = V_i + 4 \text{ V}$$

For $V_i = -9$ V, the capacitor charges to a maximum value of

$$V_c = -9 + 4 = (-5) \text{ volt}$$

Considering R as very large, now the diode remains reverse biased. We get,

$$V_0 = V_i - V_c$$

$$V_0 = V_i + 5$$

For $V_i = 9$ V, $V_0 = 9 + 5 = 14$ V

For $V_i = -9$ V, $V_0 = -9 + 5 = -4$ V

Thus, option (a) is our answer.

21. (d)

We know that, for a full wave rectifier,

$$V_{DCNL} = \frac{2V_m}{\pi}, \text{ where } V_m = \text{peak value of the sinusoidal input}$$

$$V_{DCNL} = \frac{2V_m}{\pi} = 28.28$$

$$V_m = \frac{28.28\pi}{2} \text{ V}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{28.28\pi}{2\times\sqrt{2}} = \frac{28.28\pi}{2\times 1.414}$$

$$V_{rms} = 10\pi = 31.4 \text{ volt}$$

22. (b)

- The oscillator circuits rely on positive feedback to generate self-sustaining oscillations.
- Transistor parameters like β vary with temperature and aging.
- In the oscillator circuits, feedback networks are typically passive. They consist of passive components like resistors, capacitors, and inductors, to provide the necessary phase shift to achieve positive feedback.

Thus, all the statements are correct. Therefore, option (b) is correct.

23. (a)

Feedback Topology	Input impedance	Output impedance
Voltage series	Increases	Decreases
Voltage shunt	Decreases	Decreases
Current series	Increases	Increases
Current shunt	Decreases	Increases

24. (a)

Power amplifier supplies large AC single power to load by internally converting a part of the DC power drawn from biasing supply into AC power.

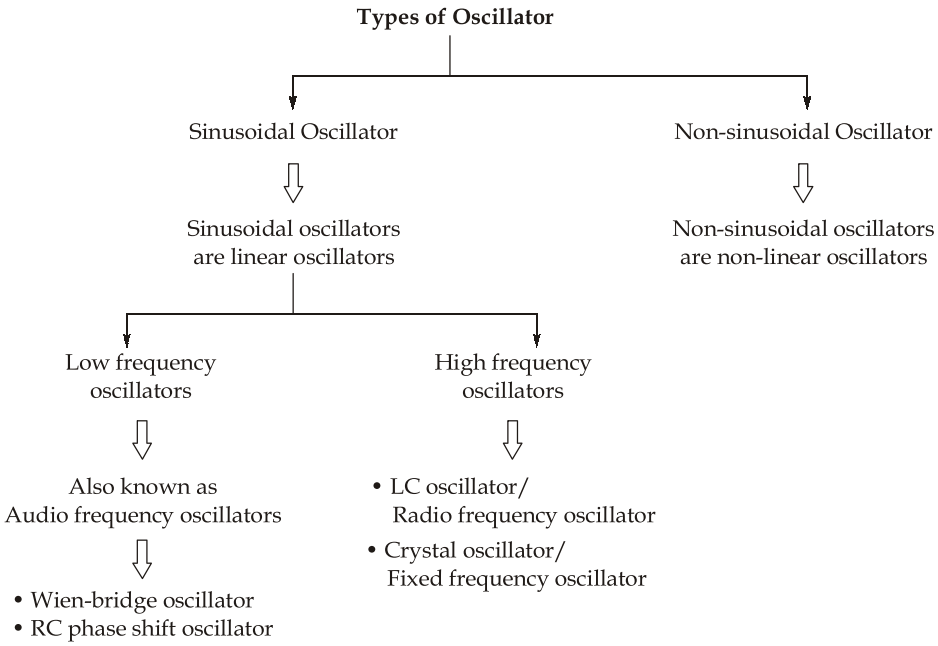
25. (d)

- In a superheterodyne receiver, RF amplifiers uses single tuned amplifiers to achieve more selectivity.
- When 'N' identical single tunned amplifier are cascaded then overall $BW = BW_1\sqrt{2^{1/N} - 1}$.

- When 'N' identical double tunned amplifier are cascaded then overall BW is given as $BW = BW_1\sqrt[4]{(2^{1/N}-1)}$.

26. (d)

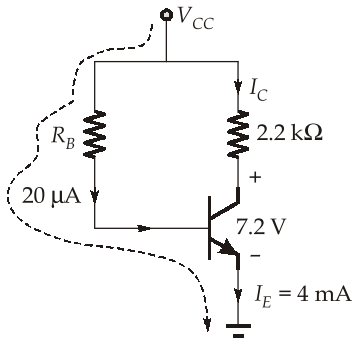
Oscillator is an electronic circuit which generates AC waveform without using AC input.



27. (a)

Due to its ability to generate a single output pulse of a specific duration, the Monostable multivibrator is commonly used as a delay circuit.

28. (a)



On applying KVL in the base emitter loop, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$V_{CC} = (20 \times 10^{-6})R_B + 0.7 \quad \text{...(i)}$$

As,

$$I_E = I_C + I_B$$

$$I_C = I_E - I_B$$

$$I_C = (4 \times 10^{-3} - 20 \times 10^{-6})$$

$$I_C = 3.98 \text{ mA} \quad \text{...(ii)}$$

Now, on applying KVL in the collector-emitter loop, we get

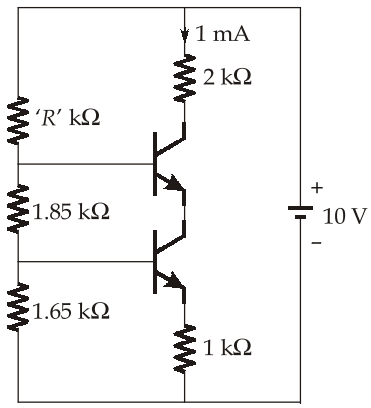
$$V_{CC} = V_{CE} + 2.2\,kI_C$$
$$V_{CC} = 7.2 + (2.2k)(3.98 \times 10^{-3})$$
$$V_{CC} = 15.956 \text{ volt}$$

Substituting $V_{CC} = 15.956$ V in equation (i), we get

$$15.956 = (20 \times 10^{-6})R_B + 0.7$$
$$R_B = \frac{15.956 - 0.7}{20 \times 10^{-6}}$$
$$R_B = 762.8 \text{ k}\Omega$$

29. (a)

We have circuit,



Given that 'β' is very large; it implies $I_E \approx I_C$ ($\because I_B \approx 0$)

So, $I_B = 0$

We have, $$V_{1.65} = \frac{10 \times 1.65}{1.65 + 1.85 + R}$$

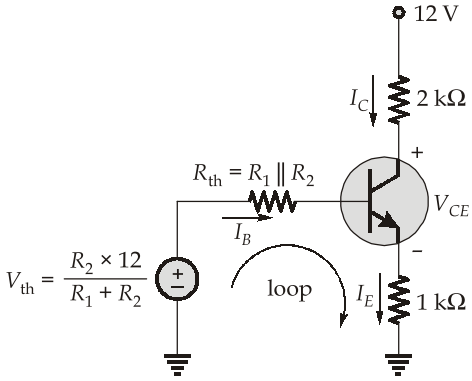
$$V_{1.65} = \frac{16.5}{3.5 + R} \quad \text{...(i)}$$

On applying KVL in input mesh, we get

$$V_{1.65} = V_{BE} + I_E R_E$$
$$\frac{16.5}{3.5 + R} = 0.65 + (1 \times 10^{-3} \times 1 \times 10^{+3})$$
$$\frac{16.5}{0.65 + 1} = 3.5 + R$$
$$R = 6.5\ \Omega$$

30. (b)

The Thevenin equivalent circuit can be drawn as below,



As quiescent point is (6, 0.002) i.e.,

$$V_{CE} = 6 \text{ V and } I_C = 0.002 \text{ A}$$

On applying KVL in base loop, we get

$$-V_{th} + R_{th} I_B + 1000 I_E = 0$$

As β is too large i.e., $I_B \approx 0$ and $I_E \approx I_C$, we get

$$-V_{th} + R_{th}(0) + 1000 I_C = 0$$

$$V_{th} = 1000 I_C$$

$$V_{th} = 1000 \times 0.002$$

$$V_{th} = 2 \text{ V}$$

Since, $$V_{th} = \frac{R_2}{R_1 + R_2} \times 12 = 2$$

$$\frac{R_2}{R_1 + R_2} = \frac{2}{12}$$

$$12R_2 = 2R_1 + 2R_2$$

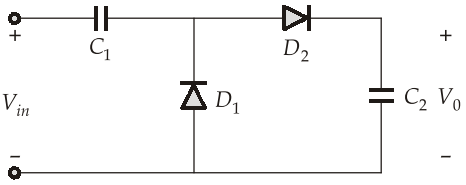
$$10R_2 = 2R_1$$

$$\frac{R_1}{R_2} = 5$$

$$R_1 = 5R_2$$

31. (d)

- A center-tapped rectifier relies on a center-tapped transformer to create two equal but opposite-phase voltage sources, necessary for its operation.
- Full-wave voltage doubler consists of 2 diodes and 2 capacitors as shown:



- In bridge rectifier, 4 diodes are used whereas in full wave centre tapped rectifier, 2 diodes are used. Therefore, statement (iii) is incorrect.

32. (d)

During positive cycle, capacitor is charged upto V_m = 5 Volt. But when input 'V_s' reduces below V_m, diode is reverse biased and is switched-off.

$$V_{out} = V_m = 5 \text{ volt}$$

For negative peak anode is at $-V_m = -5$ volt.

At this instant voltage across diode is maximum. Thus,

$$PIV = V_m - (-V_m) = 2\,V_m$$
$$PIV = 2\,V_m = 2 \times 5 = 10 \text{ volt}$$

33. (d)

Method-I:

Amplifier gain after first feedback $\beta_1 = 2.5 \times 10^{-3}$ is

$$A_{CL_1} = \frac{A_{OL}}{1+\beta_1 A_{OL}}$$

$$A_{CL_1} = \frac{1000}{1+(2.5\times10^{-3}\times1000)} = \frac{1000}{3.5}$$

And, on applying second feedback with feedback factor, $\beta_2 = 3.5 \times 10^{-3}$, the amplifier gain becomes

$$A_{CL_2} = \frac{A_{CL_1}}{1+\beta_2 A_{CL_1}}$$

$$A_{CL_2} = \frac{\left(\frac{1000}{3.5}\right)}{1+\frac{1000}{3.5}\times3.5\times10^{-3}} = \frac{1000}{3.5\times2} = \frac{1000}{7}$$

Considering the overall feedback factor as β_{net}, we have

$$A_{CL_2} = \frac{A}{1+\beta_{net}A}$$

$$\frac{1000}{7} = \frac{1000}{1+\beta_{net}(1000)}$$

$$1 + \beta_{net}(1000) = 7$$
$$\beta_{net}(1000) = 6$$
$$\beta_{net} = 6 \times 10^{-3}$$

Method-II:

We know that for simultaneous feedback, overall feedback factor (β) is given as,

$$\beta_N = \pm\beta_1 \pm \beta_2$$

Here, both are negative feedback. We have,

$$\beta_N = \beta_1 + \beta_2$$
$$\beta_N = (2.5 \times 10^{-3}) + (3.5 \times 10^{-3}) = 6 \times 10^{-3}$$

34. (d)

There are four possible combinations for Voltage and Current with which we can sample at the output and mix the feedback to the input.

We know that,

Input	Output
⇓	⇓
Mixing	Sampling
⇓	⇓
• Voltage mixing (Series mixing)	• Voltage sampling (Shunt sampling)
• Current mixing (Shunt mixing)	• Current sampling (Series sampling)

Now, let see each column one by one,

P.

Shunt	Series feedback	
⇓	⇓	
Input	Output	.....(1)
⇓	⇓	
Current mixing	Current sampling	

Q.

Voltage	Series feedback	
⇓	⇓	
Output	Input	.....(3)
⇓	⇓	
Voltage sampling	Voltage mixing	

R.

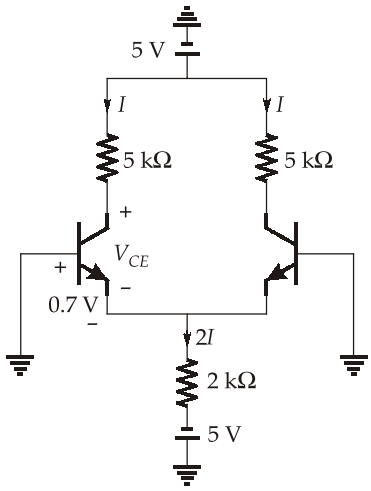
Current	Series feedback	
⇓	⇓	
Output	Input	.....(4)
⇓	⇓	
Current sampling	Voltage mixing	

S.

Shunt	Sampling and shunt mixing	
⇓	⇓	
Output	Input	.....(2)
⇓	⇓	
Voltage sampling	Current mixing	

35. (a)

For $V_1 = V_2 = 0$, the circuit can be drawn as below,



On apply KVL in collector loop, we get

$$-5 + 5kI + V_{CE} + 4kI - 5 = 0$$

$$9kI = 10 - V_{CE} \quad \text{...(i)}$$

Similarly on applying KVL in base loop, we get

$$+0.7 + 4kI - 5 = 0$$

$$I = \frac{4.3}{4k} = 1.075 \text{ mA}$$

and using equation (i), we get

$$V_{CE} = 10 - 9\text{k}(1.075 \times 10^{-3})$$

$$V_{CE} = 0.325 \text{ volt}$$

The current through 2 kΩ resistance is $2I = 2.15$ mA and the current through 5 kΩ resistance is $I = 1.075$ mA.

Hence, option (a) is correct.

36. (b)

We have,

$$V_{i1} = 180 \text{ μV and}$$

$$V_{i2} = 150 \text{ μV}$$

The output voltage is given by, $V_0 = A_d V_d + A_{CM} V_c$

where, A_d = differential gain = 4000

Differential input, $V_d = V_{i1} - V_{i2}$

$$V_d = 180 - 150 = 30 \text{ μV}$$

V_c = Common mode input

$$= \frac{V_{i1} + V_{i2}}{2} = \frac{150 + 180}{2} = 165 \text{ μV}$$

We know that, $\text{CMRR} = \frac{A_d}{A_{CM}}$, where A_{CM} = common-mode gain

$$100 \times 10^3 = \frac{4000}{A_{CM}}$$

$$A_{CM} = \frac{4000}{100 \times 10^3} = \frac{1}{25}$$

Now,

$$V_0 = A_d V_d + A_{CM} V_c$$

$$V_0 = (4000 \times 30 \times 10^{-6}) + \left(\frac{1}{25} \times 165 \times 10^{-6}\right)$$

$$V_0 \approx 0.12 \text{ Volt}$$

37. (b)

The flat-band voltage (VFB) is defined as the applied gate voltage such that there is no band bending (or no electric field) in the semiconductor and, as a result, zero net space charge in the region. However, the flat-band voltage shift due to the trapped charge density at the dielectric-semiconductor interface. Hence, both Statement (I) and Statement (II) are true but Statement (II) is not the correct explanation of Statement (I).

38. (a)

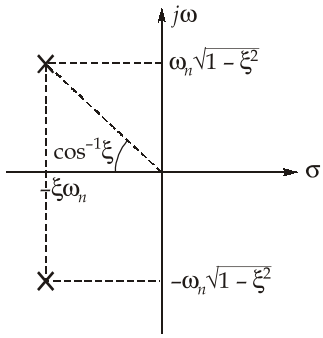
Because of the fixed depletion region, PIN diode has low transit time and low RC time constant and hence, short response time.

Section B : Control Systems-1 + Microprocessors and Microcontroller-1

39. (c)

We know that, the poles of closed loop system for $\xi < 1$ (underdamped system) is given as

$$s_{1,2} = -\xi\omega_n \pm j\omega_n\sqrt{1-\xi^2}$$



Now, from given plot, we get

$$\cos^{-1}\xi = 60°$$

$$\xi = \cos 60° = \frac{1}{2}$$

and $-\xi\omega_n = -5$ i.e.,

$$\xi\omega_n = 5$$

$$\omega_n = \frac{5}{\xi} = \frac{5}{\left(\frac{1}{2}\right)} = 10 \text{ rad/sec}$$

Now, closed loop transfer function is

$$\frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} = \frac{100}{s^2 + 10s + 100}$$

Thus, closed loop poles are at $s_{1,2} = (-5 \pm j5\sqrt{3})$

Thus, the open loop transfer function is given as

$$G(s)H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s} = \frac{\omega_n^2}{s(s + 2\xi\omega_n)}$$

Substituting ω_n = 10 rad/sec and ξ = 0.5, we get

$$G(s)H(s) = \frac{100}{s(s+10)}$$

Then, the open loop poles are at s = 0 and s = –10.

40. (b)

The output of a standard second order system for unit step input is given as

$$y(t) = 1 - \frac{e^{-\xi\omega_n t}}{\sqrt{1-\xi^2}}\sin(\omega_d t + \theta)$$

From given data,

$$y(t) = 1 - \frac{2}{\sqrt{3}}e^{-5t}\sin\left(5\sqrt{3}t - \frac{\pi}{6}\right)$$

On comparison, we get

$$-\xi\omega_n = -5$$

$$\alpha = \xi\omega_n = 5 \quad \text{...(i)}$$

$$\omega_d = \omega_n\sqrt{1-\xi^2} = 5\sqrt{3} \text{ rad/sec} \quad \text{...(ii)}$$

$$\omega_n = \sqrt{\alpha^2 + \omega_d^2}$$

$$\omega_n = \sqrt{(5)^2 + (5\sqrt{3})^2}$$

$$\omega_n = \sqrt{25+75} = 10 \text{ rad/sec}$$

Now, on substituting ω_n = 10 rad/sec in equation (i), we get

$$\xi = 0.5$$

The time for first undershoot is

$$t_p = \frac{2n\pi}{\omega_d}\text{sec} \qquad \text{(For first undershoot, } n = 1\text{)}$$

$$t_p = \frac{2\pi}{5\sqrt{3}}\text{sec}$$

$$t_p = 0.72 \text{ sec}$$

Therefore, time taken for first undershoot t_p = 0.72 sec and damping ratio, ξ = 0.5. Hence, option (b) is correct.

41. (b)

- A critically damped system moves as quickly as possible towards equilibrium without oscillations, and thus takes minimum time to reach its final output. Therefore, statement 1 is correct.
- The steady-state error is inversely proportional to the gain. Therefore, it can be reduced by increasing the system gain. Therefore, statement 2 is correct.

For a critically damped system ($\xi = 1$), the open loop transfer function is

$$G(s)H(s) = \frac{\omega_n^2}{s(s+2\xi\omega_n)} = \frac{\omega_n^2}{s(s+2\omega_n)}$$

The open loop poles of a critically damped closed loop system is $s = 0$ and $s = -2\omega_n$. However, the closed loop poles of a critically damped closed loop system are at $s = -\omega_n$ i.e. real, equal and negative.

Therefore, statement 3 is incorrect.

42. (a)

We have,

undamped natural frequency, $\omega_n = 5$ rad/sec ...(i)

Percentage peak overshoot, $\%M_p = 4.3\%$

We know that,

$$\%M_p = e^{-\left(\frac{\pi\xi}{\sqrt{1-\xi^2}}\right)} \times 100$$

$$\frac{4.3}{100} = e^{-\left(\frac{\pi\xi}{\sqrt{1-\xi^2}}\right)}$$

$$\ln\left(\frac{4.3}{100}\right) = \frac{-\pi\xi}{\sqrt{1-\xi^2}}$$

$$-\pi = \frac{-\pi\xi}{\sqrt{1-\xi^2}}$$

$$\sqrt{1-\xi^2} = \xi$$

$$1 - \xi^2 = \xi^2$$

$$2\xi^2 = 1$$

$$\xi = \frac{1}{\sqrt{2}} \quad \text{...(ii)}$$

Now,

Time period for damped oscillations, $T = \frac{2\pi}{\omega_d} = \frac{2\pi}{\omega_n\sqrt{1-\xi^2}}$

$$T = \frac{2\pi}{5\sqrt{1-\left(\frac{1}{\sqrt{2}}\right)^2}} = \frac{2\pi\times\sqrt{2}}{5}\text{sec}$$

The settling time for 2% tolerance band is given by

$$t_s = \frac{t_s}{T} = \frac{4}{\xi\omega_n}$$

So, number of cycles completed before the output get settled within 2% of its final value

$$= \frac{4}{\xi\omega_n T} = \frac{4\times5}{\left(\frac{1}{\sqrt{2}}\right)\times5\times2\pi\times\sqrt{2}} = \frac{2}{\pi} = 0.63 \text{ cycles}$$

43. (b)

- The complex conjugate poles and zeros of the open-loop transfer function have no effect on the root-loci on the real axis because angle contribution of such a pair of conjugate poles or zeros is 2π radians on the real axis. Therefore, statement 1 is correct.
- Root loci is drawn using open loop transfer function. The plot gives the locus of the closed loop poles as the system gain 'k' is varied from 0 to ∞ and thus, can be used to determine the stability of closed loop system for different values of k.
  Therefore, statement 2 is incorrect.
- The addition of open loop zeros pulls the root-loci away from the $j\omega$-axis and therefore, system become more stable. Therefore statement 3 is correct.

44. (c)

The characteristic equation of the system is given as

$$P(s) = 1 + G(s)H(s) = 0$$

$$\Rightarrow \quad s(s-2)(s+5) + ks + k = 0$$
$$s(s^2 + 3s - 10) + ks + k = 0$$
$$s^3 + 3s^2 - 10s + ks + k = 0$$
$$s^3 + 3s^2 + s(k-10) + k = 0$$

Using Routh-Hurwitz criteria,

s^3	1	$k-10$
s^2	3	k
s^1	$\frac{3(k-10)-k}{3}$	
s^0	k	

Now, for stable system, there should be no sign change in the first column of Routh array. Hence,

$$\frac{3k-30-k}{3} > 0 \text{ and } k > 0 \qquad \text{...(ii)}$$

$$2k > 30$$

$$k > 15 \qquad \text{...(i)}$$

Therefore, for stable system, $k > 15$.

45. (b)

- Feedback introduces the possibility of instability as it controls the dynamics by adjusting the poles.
- Feedback reduces sensitivity to parameter variations, reduces non-linear behavior, improves transient response, minimize the effect of disturbance signal.
- It increases bandwidth of system.
- It reduces the gain of the system.

Thus, statements 2 and 3 are correct.

Effect of feedback on system are given below,

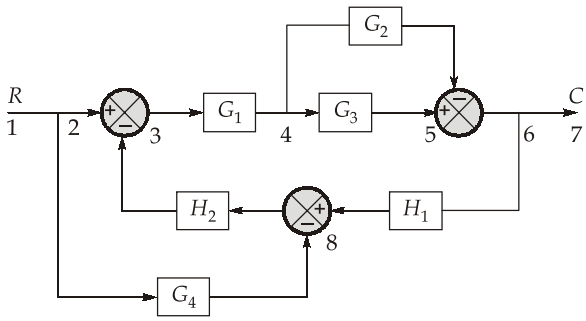
	Negative feedback	Positive feedback
Gain	↓	↑
Bandwidth	↑	↓
Time constant	↓	↑
Speed	↑	↓
Sensitivity	↓	↑
Stability	↑	↓

Decrease ↓; increase ↑

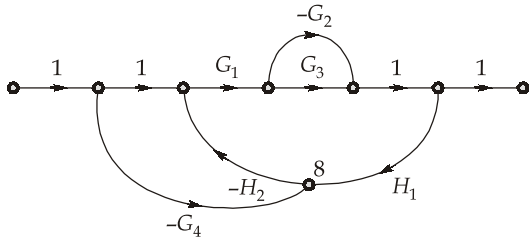
46. (c)

47. (c)

The nodes are assigned at input, output of every summing point and branch point as shown in figure.



The signal flow graph for the above block diagram is obtained as below,



- Forward path gains:
  There are four forward paths; $k = 4$
  Gain of forward paths, $P_1 = G_1G_3$
  $P_2 = -G_1G_2$
  $P_3 = G_1G_3G_4H_2$
  $P_4 = -G_1G_2G_4H_2$
- Individual loop gains:
  There are two individual loops, let individual loop gain be P_{11} and P_{21}.
  We have,
  $P_{11} = -G_1G_3H_1H_2$
  $P_{21} = G_1G_2H_1H_2$
  There are no non-touching loops.
  Transfer function, T by Mason's gain formula

$$T = \frac{1}{\Delta}\sum_K P_k\Delta_k = \frac{P_1 + P_2 + P_3 + P_4}{\Delta}$$

where, Δ = 1 – (sum of individual loop gains) + (sum of product of two non-touching loop gains) – ....

$$= 1 - [P_{11} + P_{21}] + 0$$

$$= 1 + G_1G_3H_1H_2 - G_1G_2H_1H_2$$

$$T = \frac{G_1G_3 - G_1G_2 + G_1G_3G_4H_2 - G_1G_2G_4H_2}{1 + G_1G_3H_1H_2 - G_1G_2H_1H_2}$$

$$T = \frac{G_1(G_3 - G_2)(1 + G_4H_2)}{1 + G_1H_1H_2(G_3 - G_2)} = \frac{1 + G_4H_2}{H_1H_2 + \dfrac{1}{G_1(G_3 - G_2)}}$$

Hence, statements 1, 2 and 4 are correct.

48. (d)

Important registers used in 8085 are:

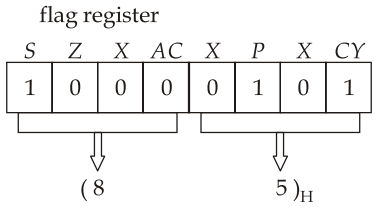
- Accumulator (8 bit)
- Register B, C, D, E, H and L (8 bit)
- Flag register (8-bit)
- Program counter (16-bit)
- Stack pointer (16-bit)

The stack pointer in the 8085 microprocessor is a 16-bit register that stores the address of the top of stack memory. Hence, option (b) is correct.

49. (b)

- Flag register is a 8-bit register, in which if an arithmetic operation results in carry, the carry bit is set, otherwise it is reset. Thus, statement (1) is incorrect.
- If parity bit in a flag register is 1; it implies that the resultant after an arithmetic operation has an even number of 1's. Thus, statement (2) is correct.

- $(85)_H$ stored in flag register can be expressed as,



It implies carry bit, CY as 1. Thus, statement (3) is also correct.

50. (c)

READY-Active low signal, input to 8085 as an external request from slow peripheral to indicate that peripheral is not yet ready for data transfer between processor and peripheral devices. A low READY signal tells the CPU to enter wait states. The CPU will wait for READY to go high for completing the operation.

51. (c)

PUSH	a	⇒	Put a on the stack
PUSH	b	⇒	Put b on the stack
PUSH	c	⇒	Put c on the stack
POP	AX	⇒	Store c in AX
POP	BX	⇒	Store b in BX
SUB	AX, BX	⇒	Store (c – b) in AX
POP	BX	⇒	Store a in BX
ADD	AX, BX	⇒	Store c – b + a in AX

Finally after execution of the program, the content of AX is (c – b + a).

52. (a)

The general purpose registers of 8085 are: B, C, D, E, H and L. They are all 8-bit registers but can also be used as 16-bit register pairs—BC, DE and HL. These registers are also known as scratch pad registers used for temporary storage of data during program execution. *W* and *Z* registers are internal registers not accessible to the user and thus, does not belong to scratch pad registers.

53. (c)

- The output of an assembler is typically machine code (binary), and the output of a compiler is often machine code or an intermediate representation like object code or bytecode and is usually not in mnemonic form. Thus, statement 1 is correct and statement 2 is not correct.
- High-level languages and their compilers generally offer more sophisticated debugging tools and features than assemblers. Therefore, statement 3 is correct.

54. (c)

A typical assembly language statement consists of the following fields:

- Label: (Optional) A symbolic name for a memory location.
- Mnemonic (Opcode): The instruction to be executed (e.g., MOV, ADD, JMP).
- Operand(s): The data or memory addresses that the instruction operates on.
- Comment: (Optional) Explanatory notes.

55. (b)

Instruction cycle is combination of fetch cycle and execute cycle. The fetch cycle is responsible for retrieving the instruction from memory, while the execution cycle is responsible for executing the instruction.

56. (b)

There are 8 software interrupts in 8085, RSTn (n = 0 to 7). These interrupts are enabled following the execution of EI instruction. The interrupts allow the processor to suspend its current execution and jump to a specific memory location (interrupt service routine) to handle a specific event or task which may include communication with peripheral devices. Thus, both the statements are true. But, statement-II is not the explanation of statement-II.

Section C : Network Theory-2 + Digital Circuits-2

57. (c)

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = R_1 \qquad \text{[Due to virtual short, } V_- = V_+ = 0 \text{ V]}$$

$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = 0$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = -R_2$$

$$Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = 0$$

[The current through input terminals of op-amp is zero. Since $I_1 = 0$, hence the current through resistance R_2 is zero. Thus, $V_2 = 0$]

$\therefore$ The z-parameters are, $[z] = \begin{bmatrix} R_1 & 0 \\ -R_2 & 0 \end{bmatrix}$

As $|z| = 0$, $[z]^{-1}$ does not exist.

Since $[z]^{-1}$ does not exist, $[y]$ does not exist.

The circuit is not reciprocal because of the active element (op-amp).

58. (c)

Substituting the given z-parameters into the z-parameter equations, we get,

$$V_1 = Z_{11}I_1 + Z_{12}I_2 = 6I_1 - j4I_2 \qquad \text{...(i)}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 = -j4I_1 + 8I_2 \qquad \text{...(ii)}$$

From the given circuit, $V_2 = 0$

From equation (ii), $0 = -j4I_1 + 8I_2$

$\Rightarrow$ $8I_2 = j4I_1$

$$I_2 = j0.5I_1 \qquad \text{...(iii)}$$

Substituting equation (iii) in equation (i)

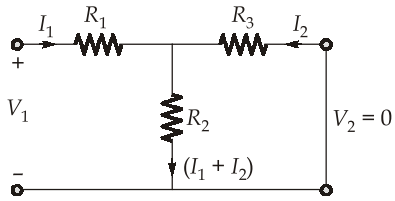
$$V_1 = 6I_1 - j4(j0.5I_1)$$
$$V_1 = 6I_1 + 2I_1 = 8I_1$$

Applying KVL to input-loop,

$$-v_s + 2I_1 + V_1 = 0$$
$$-v_s + 2I_1 + 8I_1 = 0$$
$$v_s = 10I_1$$

$$\therefore \quad z_{in} = \frac{v_s}{I_1} = 10\,\Omega$$

59. (c)



$$B = \left.\frac{-V_1}{I_2}\right|_{V_2 = 0}$$

To obtain the parameter 'B', short-circuit the output port i.e. $V_2 = 0$.

Applying KVL to input-port,

$$-V_1 + R_1I_1 + R_2(I_1 + I_2) = 0$$
$$-V_1 + (R_1 + R_2)I_1 + R_2I_2 = 0 \qquad \text{...(i)}$$

Applying KVL to output-port,

$$I_2R_3 + (I_1 + I_2)R_2 = 0$$
$$I_1R_2 + (R_2 + R_3)I_2 = 0$$

$$\Rightarrow \quad I_1 = \frac{-(R_2 + R_3)}{R_2}I_2 \qquad \text{...(ii)}$$

Substituting equation (ii) in equation (i),

$$-V_1 + (R_1 + R_2)\left[\frac{-(R_2 + R_3)}{R_2}\right]I_2 + R_2I_2 = 0$$

$$-V_1 - \left[\frac{R_1(R_2 + R_3)}{R_2} + R_3\right]I_2 = 0$$

$$\Rightarrow \quad B = \frac{-V_1}{I_2} = R_3 + \frac{R_1(R_2 + R_3)}{R_2}$$

60. (c)

The valid relationships between parameters are,

$$[y] = \begin{bmatrix} \frac{z_{22}}{\Delta_z} & \frac{-z_{12}}{\Delta_z} \\ \frac{-z_{21}}{\Delta_z} & \frac{z_{11}}{\Delta_z} \end{bmatrix} = [z]^{-1}$$

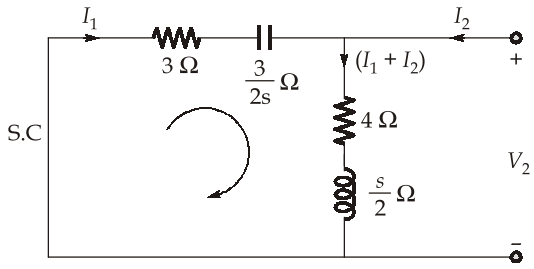
$$[g] = \begin{bmatrix} \frac{h_{22}}{\Delta_h} & \frac{-h_{12}}{\Delta_h} \\ \frac{-h_{21}}{\Delta_h} & \frac{h_{11}}{\Delta_h} \end{bmatrix} = [h]^{-1}$$

$$[t] = \begin{bmatrix} \frac{D}{\Delta_T} & \frac{B}{\Delta_T} \\ \frac{C}{\Delta_T} & \frac{A}{\Delta_T} \end{bmatrix} \neq [T]^{-1}$$

61. (d)

We know, $Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0}$

Making port-1 short circuited, the equivalent circuit in s-domain is obtained as,



Apply KVL around loop,

$$\left(3+\frac{3}{2s}+4+\frac{s}{2}\right)I_1 + \left(4+\frac{s}{2}\right)I_2 = 0$$

$$\Rightarrow \quad I_2 = \frac{-\left(3+\frac{3}{2s}+4+\frac{s}{2}\right)}{\left(4+\frac{s}{2}\right)} I_1 \qquad \ldots(i)$$

The voltage, $V_2 = (I_1 + I_2)\left(4+\frac{s}{2}\right)$

Using equation (i), $V_2 = \left(I_1 - \frac{\left(3+\frac{3}{2s}+4+\frac{s}{2}\right)}{\left(4+\frac{s}{2}\right)} I_1\right)\left(4+\frac{s}{2}\right)$

$$V_2 = \left[\left(4+\frac{s}{2}\right) - \left(3+\frac{3}{2s}+4+\frac{s}{2}\right)\right] I_1$$

$$\Rightarrow \quad V_2 = -\left(3+\frac{3}{2s}\right) I_1$$

$$\therefore \quad Y_{12} = \frac{I_1}{V_2} = -\frac{1}{3\left(1+\frac{1}{2s}\right)} = \frac{-2}{3}\left(\frac{s}{2s+1}\right) \text{℧}$$

62. (c)

The tie-set matrix is of the order $(b - n + 1) \times b$. Thus, we have number of branches, $b = 5$ and number of nodes, $n = 4$. Here, B = [$I_{2\times2}$: B_t], then we have $Q_l = -[B_t]^T$. Thus,

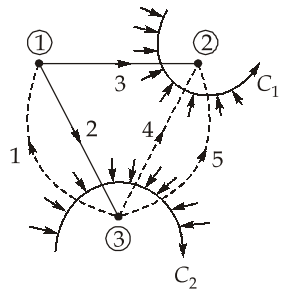
$$Q_l = \begin{bmatrix} -1 & 1 & 0 \\ -1 & 0 & 1 \end{bmatrix}^T = \begin{bmatrix} 1 & 1 \\ -1 & 0 \\ 0 & -1 \end{bmatrix}$$

The cut-set matrix is of the order $(n - 1) \times b$ i.e. 3×5 given as below"

$$[Q] = [Q_l : I_{3\times3}] = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 & 1 \end{bmatrix}$$

63. (d)

Since branches 1, 4 and 5 are links, the branches 2 and 3 constitute a tree.



In the figure shown, C_1 and C_2 are fundamental cut-sets. We take the matrix element as +1 when the corresponding branch is oriented in the same direction as cut-set. Otherwise the element is –1 when the orientation of the cut-set and branch is opposite.

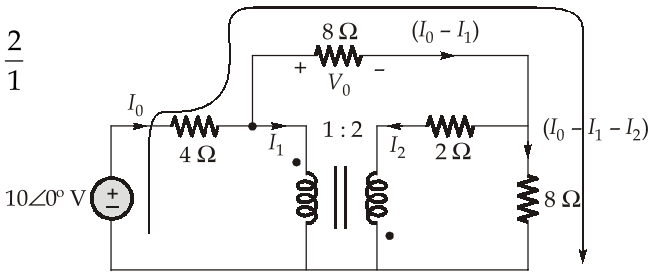
The cut-set matrix is,

$$[Q] = \begin{matrix} \\ C_1 \\ C_2 \end{matrix} \begin{matrix} \begin{matrix} 1 & 2 & 3 & 4 & 5 \end{matrix} \\ \begin{bmatrix} 0 & 0 & 1 & 1 & 1 \\ -1 & 1 & 0 & -1 & -1 \end{bmatrix}_{2\times5} \end{matrix}$$

64. (c)

Using dot convention, $\dfrac{I_1}{I_2} = \dfrac{N_2}{N_1} = \dfrac{2}{1}$

$\Rightarrow$ $I_2 = \dfrac{I_1}{2}$



Apply KVL around the outer loop,

$-10\angle0° + 4I_0 + 8(I_0 - I_1) + 8(I_0 - I_1 - I_2) = 0$

$-10\angle0° + 4I_0 + 16(I_0 - I_1) - 8I_2 = 0$

$$-10\angle0° + 4I_0 + 16(I_0 - I_1) - 8\times\frac{I_1}{2} = 0 \quad \text{...(i)}$$

We have, $V_0 = 8[I_0 - I_1]$

From equation (i),

$$-10\angle 0° + 4(I_0 - I_1) + 16(I_0 - I_1) = 0$$

$$-10\angle 0° + 20(I_0 - I_1) = 0$$

$$(I_0 - I_1) = \frac{10\angle 0°}{20} = 0.5\angle 0°$$

Using equation (ii), $\frac{V_0}{8} = 0.5\angle 0°$

$\Rightarrow$ $V_0 = 4\angle 0°$ V

65. (d)

The characteristic equation of JK Flip flop is given as,

$$Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$$

For $J = D$ and $K = \overline{D}$, we obtain

$$Q_{n+1} = D\overline{Q_n} + DQ_n = D(\overline{Q_n} + Q_n) = D$$

which is the characteristic equation for D flip-flop. Hence, statement 1 is correct.
Similarly, the characteristic equation of SR Flip flop is given as,

$$Q_{n+1} = S + \overline{R}Q_n$$

For $S = D$ and $R = \overline{D}$, we obtain

$$Q_{n+1} = D + DQ_n = D(1 + Q_n) = D$$

which is the characteristic equation for D flip-flop. Hence, statement 2 is correct.

66. (a)

The truth table of J-K flip-flop is given as,

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

$$Q(t+1) = J\overline{Q(t)} + \overline{K}Q(t)$$

The excitation table can, thus be obtained as

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

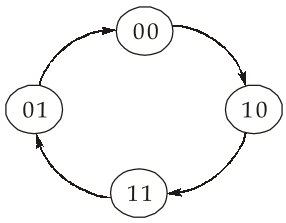
Hence, option (a) is correct.

67. (b)

The state table of the given sequential circuit is obtained as below,

J_1	K_1	J_0	K_0	$Q_1(t+1)$	$Q_0(t+1)$
$\overline{Q_0}$	Q_0	Q_1	$\overline{Q_1}$	0	0
1	0	0	1	1	0
1	0	1	0	1	1
0	1	1	0	0	1
0	1	0	1	0	0

State Diagram:



Hence, it works as a MOD 4 counter.

68. (c)

- ECL (Emitter Coupled Logic) is the fastest logic family. It achieves its high-speed operation by operating in the active region and preventing the transistors from entering the saturation region. ECL circuits usually operate with negative power supplies to minimize the influence of the power supply variations on the logic levels.
- CMOS circuits have almost zero static power dissipation and draws negligible current. Whereas ECL has a power dissipation three to 10 times higher than that of TTL.

Thus, statements 2, 3 and 4 are correct.

69. (a)

PAL ⇒ Programmable AND array and fixed OR array
PLA ⇒ Programmable AND array and programmable OR array
PROM ⇒ A type of ROM that can be programmed once.
ROM ⇒ Can't be programmed; and has a predefined logic

70. (b)

For an n-bit ADC, the range of digital output values is from 0 to $2^n - 1$. The digital output can be calculated using the formula

$$\text{Digital output} = \frac{\text{Analog input voltage}}{\text{Reference voltage}} \times (2^n - 1)$$

On substituting the given data, we get

$$128 = \frac{2.5}{5} \times (2^n - 1)$$

$$\frac{128 \times 5}{2.5} = 2^n - 1$$

$$2^n - 1 = 256$$
$$2^n = 257$$

'n' must be greater than '8'.

Therefore option (b) is correct.

71. (d)

	Mealy Machine	Moore Machine
Output Dependency	Output depends on both the current state and the input.	Output depends only on the current state.
State Transitions	Output can change during state transitions based on the input.	Output changes only when the state changes.
Output Change frequency	Output can change more frequently (because it depends on input and state).	Output changes only when the state transitions
Number of states	Typically requires fewer states to represent the same functionality.	Typically requires more states for the same functionality.
Design Complexity	Slightly more complex due to output dependency on both state and input.	Simpler to design, as the output depends only on the state.
Timing Diagram	Output changes in response to both input and state transitions.	Output changes only on state transitions.
Examples	Used in systems where outputs need to react immediately to inputs (e.g., control systems, data encoding).	Used in simpler systems where output is less dependent on the input (e.g., counters, sequence detectors).
Output Stability	Output can change asynchronously with the input.	Output is more stable, as it only changes when entering a new state.

72. (b)

The incidence matrix has n rows, one for each node and b columns, one for each branch. The elements of the incidence matrix $[A] = [a_{ij}]_{n\times b}$ are given by

- $a_{ij} = 1$, if j^{th} branch is incident at i^{th} node and oriented away from the node.
- $a_{ij} = -1$, if j^{th} branch is incident at i^{th} node and oriented towards the node.
- $a_{ij} = 0$, if j^{th} branch is not incident at i^{th} node.

Thus, in an incidence matrix, the unit entries (1 or –1) made in a row, identify the branches incident at a node. The number of branches incident at the node of a graph is called degree of the node.

Hence, Both Statement (I) and Statement (II) are true but Statement (II) is not a correct explanation of Statement (I).

73. (d)

In synchronous sequential circuits, the state transition is always synchronized with the clock signal. However, the output may change asynchronously. In Mealy machine, the output depends on both the current state and the present input. Thus, the output can change whenever the inputs change, even between the clock edges. Thus, Statement (I) is false but Statement (II) is true.

74. (c)

Flash A/D converter is fastest because the conversion is performed simultaneously through a set of comparators. However, hardware requirement is more as for n bit conversion, 2^{n-1} comparators and 2^n resistors are required. Therefore, Statement (I) is true but Statement (II) is false.

75. (a)

In DRAM, Data is stored in the form of charge in the capacitors which tends to leak away with time. It requires periodic refreshing to avoid the same.

■■■■