DETAILED SOLUTIONS

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ESE 2025 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 4

Section A : Control Systems + Microprocessors and Microcontroller

Section B : Network Theory-1

Section C : Digital Circuits-1

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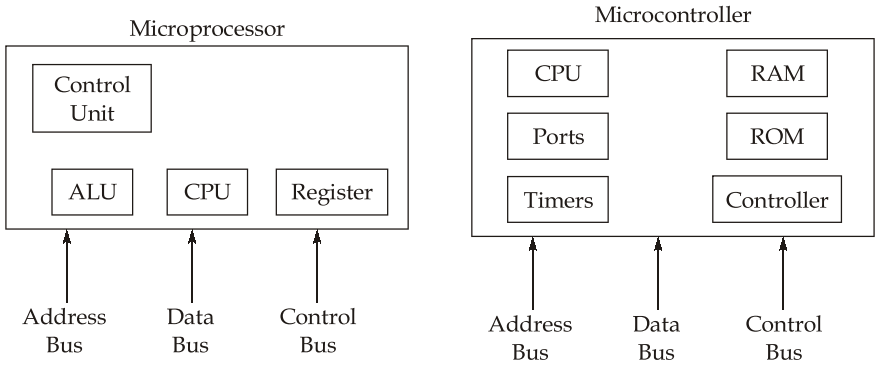
DETAILED EXPLANATIONS
Section A : Control Systems + Microprocessors and Microcontroller

1. (b)

- Micro-controller like micro-processor has Von-Neumann or Hardvard architecture. The instruction set can be CISC or RISC. However, microcontroller can be a stand alone system used in embedded system.
- Micro-controller has on-chip memory as well as on chip ports.



- Microcontrollers are designed for embedded applications where reliability and fault tolerance are critical. Since they have an integrated memory, I/O, and processing capabilities, they are resilient to faults compared to microprocessor-based designs, which rely more on external components and can be more complex and prone to failure.

2. (a)

- Many programmers prefer assembly level programming over machine language programming because assembly language is simple and easily understandable. It uses easier-to-remember mnemonic codes making it easier to write codes.
- Machine level language is directly understood by the machine.

Thus, option (a) is correct.

3. (d)

8085 microprocessor:

- It is manufactured using NMOS technology.
- It is upward compatible with 8080A.
- It is a 40 Pin (dual in line package) chip.
- It is a 8-bit processor.
- It has total 16 address lines with addressing capacity of 2^{16} Bytes = 64 kB.

4. (d)

S_1	S_0	Microprocessor operation
0	0	Halt (no operation)
0	1	Write operation
1	0	Read operation
1	1	Opcode fetch

5. (d)

Hardware interrupts:

The 8085 microprocessor has 5 hardware interrupt signals that can be used to interrupt a program execution.

It is also used to accept interrupts from the external devices.

In 8085 microprocessor, TRAP, RST 4.5, RST 5.5, RST 6.5, INTR are the hardware interrupts. Further, There are 8 software interrupts; RST 0-7. Therefore, all the given options are hardware interrupts. Hence, option (d) is correct.

6. (b)

The temporary registers *W* and *Z* are used to store data/address temporarily. These are only used by microprocessor to perform internal operations during the programme execution. These registers are also called invisible registers because they are not accessible to user during programme. Therefore, statements 2 and 3 are correct.

7. (d)

Initial address of the memory = 5000 H, and

Final address of the memory = 7FFF H

Then, size of the memory = (7FFF)H – (5000)H + 1

$= (3000)_H$

As, $(3000)_H = (12288)_{10}$

Let 'n' be the number of address lines, then the number of memory locations that can be addressed is given by 2^n. Thus,

$$2^n \geq 12288$$

$$n = 14$$

Minimum of 14 address lines are required.

Therefore, number of address lines is 14.

As in the memory location 5000H, eight bit of data (0110 1010) is present. Thus, number of data lines required is 8.

8. (a)

For I/O mapped I/O interfacing, the number of T-states needed is 10 T-states whereas for memory-mapped I/O, 13, T-states (STA, LDA) or 7 T-states (MOV M, R) is needed.

9. (d)

We know that, XRA A is the instruction through which we clear the accumulator.

XRA A ; [A] ← 00 H

MOV L, A ; [L] ← 00 H

MOV H, L ; [H] ← 00 H

INX H ; [HL] ← [HL] + 0001 H

DAD H ; [HL] ← [HL] + [HL] = 0001 H + 0001 H = 0002 H

∴ Content of HL pair after execution of the program = 0002 H

10. (a)

All the statements are correct.

11. (d)

- The 8086 microprocessor has two functional units: Execution unit (EU) and Bus interface unit (BIU).
- The BIU interface the 8086 to the outside world. It fetches, reads data from memory and ports, and writes data to memory and I/O ports.
- EU receives program instruction codes and data from the BIU, executes these instructions.
- EU and BIU function independently, whenever the execution unit starts decoding and executing fetched instructions, the BIU fetches additional instructions to the queue from the code memory for execution.

Thus, all the statements are correct.

12. (c)

TF → In 8086, if TRAP flag is set then microprocessor can be used in single step mode for debugging.

13. (b)

In 8086 microprocessor, TYPE 2 interrupt represents non-maskable interrupt (NMI). The interrupt vector address of the interrupt is found by multiplying the type by 4. Thus, for NMI, interrupt vector address is $2 \times 4 = 8_{10} = 00008$ H

14. (c)

Addressing Modes of 8086:

1. Immediate Addressing Mode: The operand is specified in the instruction itself.
   ⇒ MOV BX, 3598 H
2. Direct Addressing Mode: The effective address of the operand is written directly in the instruction.
   ⇒ ADD BL, [0103]
3. Register Addressing Mode: The operand is stored in the register.
   ⇒ MOV AX, CX
4. Register Indirect Addressing Mode: The operand's offset in the segment is stored in the register.
   ⇒ MOV BX, [BP]
5. Register Relative Addressing Mode: The operand's offset in the segment is obtained by adding an 8-bit or 16-bit displacement to the contents stored in any one of the registers BX, BP, SI and DI.
   ⇒ MOV CL, [BX + 05 H]
6. Indexed Addressing Mode: The operand's offset in the segment is the sum of the content of an index register SI or DI and an 8 bit or 16 bit displacement.
   ⇒ MOV BX, [SI + 1528 H]
7. Based Index Addressing Mode: The operand's offset in the segment is sum of the content of a base register BX and an index register SI or DI.
   ⇒ ADD CX, [BX + SI]

8. Relative Based Indexed Addressing Mode: The operand's offset in the segment is sum of the content of a base register BX, an index register SI or DI and an 8 bit or 16 bit displacement.
   ⇒ MOV AX, [BX + SI + 1234 H]

15. (c)

In the HL register pair, 'H' is the higher order register containing the higher order byte "15 H" and 'L' is the lower order register containing the lower order byte "EF H".
i.e., [H] ← 15 H and [L] ← EF H
When INR H is executed, it increments the content of H register by 01 H i.e.
[H] ← 15 + 01 i.e., [H] ← 16 H and [L] ← EF H
∴ Content of HL pair = $(16EF)_H$
Therefore, option (c) is correct.

16. (b)

We know that,
open loop transfer function for standard second order system is given as

$$G(s)H(s) = \frac{\omega_n^2}{s(s+2\xi\omega_n)}$$

Now,

$$\text{Velocity error coefficient, } k_v = \lim_{s\to 0} sG(s)H(s)$$

$$= \lim_{s\to 0} s\frac{\omega_n^2}{s(s+2\xi\omega_n)} = \frac{\omega_n}{2\xi}$$

$$e_{ss} = \frac{1}{k_V} = \frac{2\xi}{\omega_n}$$

17. (d)

- ORA R (OR register with accumulator) ⇒ All flags are affected and CY = 0, AC = 0.
- XRA M (EXOR memory with accumulator) ⇒ All flags are affected and AC = 0, CY = 0.
- ANA M (AND memory with accumulator) ⇒ All flags are affected and AC = 1, CY = 0.

18. (a)

We know that,

At 3 dB frequency, $|G(j\omega)| = \frac{1}{\sqrt{2}}$ times of maximum magnitude. (valid for both closed loop and open loop stable system)

Case-I: For open loop system,

$$|G(j\omega)| = \left|\frac{k}{(j\omega + A)}\right| = \frac{k}{\sqrt{\omega^2 + A^2}}$$

$|G(j\omega)|_{max}$ occurs at ω = 0 i.e., $|G(j\omega)|_{max} = \frac{k}{A}$

Now, from above mentioned definition, at 3 dB frequency,

$$\frac{k}{\sqrt{A^2+\omega^2}} = \frac{k}{A}\times\frac{1}{\sqrt{2}}$$

$$A^2 + \omega^2 = 2A^2$$

As $\omega = 1$ rad/sec,

$$A^2 + 1 = 2A^2$$

$$A^2 = 1$$

$$A = \pm 1$$

($A = -1$ is discarded; because for $A = -1$, system become unstable)

Hence, we get $A = 1$

Case-II: For closed loop system,

For unity feedback closed loop system, transfer function becomes

$$\text{T.F} = \frac{k}{s+A+k}$$

$$|G(j\omega)| = \frac{k}{\sqrt{\omega^2+(k+A)^2}}$$

or $|G(j\omega)|_{\max}$ at $\omega = 0$ i.e., $|G(j\omega)|_{\max} = \dfrac{k}{\sqrt{(k+A)^2}} = \dfrac{k}{(k+A)}$

Now, using the above mentioned definition, at 3 dB frequency,

$$\frac{k}{\sqrt{\omega^2+(k+A)^2}} = \frac{k}{(k+A)}\times\frac{1}{\sqrt{2}}$$

$$\sqrt{2}(k+A) = \sqrt{\omega^2+(k+A)^2}$$

On squaring both sides,

$$2(k + A)^2 = \omega^2 + (k + A)^2$$

As 3 dB frequency, $\omega = 2$ rad/sec and $A = 1$,

$$2(k + 1)^2 = (2)^2 + (k + 1)^2$$

$$(k + 1)^2 = 4$$

$$k + 1 = \pm 2$$

$$k = \pm 2 - 1$$

$$k = 1 \text{ or } -3$$

For $k = -3$, the system becomes unstable. Hence, $k = -3$ is discarded.

Thus, $k = 1$ and $A = 1$.

19. (c)

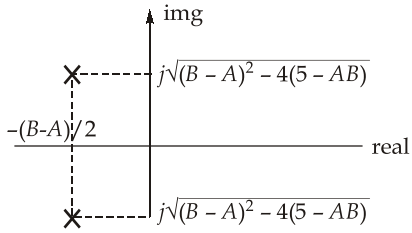
From the given block diagram,

$$\frac{C(s)}{R(s)} = \frac{5}{(s-A)(s+B)+5} = \frac{5}{s^2+s(B-A)+(5-AB)} \quad \ldots(i)$$

Now, from the characteristic equation, we get poles of the system as

$$s_{1,2} = \frac{-(B-A)\pm\sqrt{(B-A)^2-4(5-AB)}}{2}$$

Now, real part of poles, $s_{1,2} = \dfrac{-(B-A)}{2} = \dfrac{-1}{2}$



It is given that poles are symmetric about $s = -1/2$, thus,

$$\frac{-(B-A)}{2} = -\frac{1}{2} \qquad \text{...(ii)}$$

Also, we have open loop transfer function as $\dfrac{5}{(s-A)(s+B)}$. Thus, open loop DC gain of the system is obtained by putting $s = 0$ as $\dfrac{-5}{AB}$. It is given that, $\dfrac{-5}{AB} = -\dfrac{5}{2}$

Hence, $AB = 2$ ...(iii)

Now from equation (ii) and (iii) we get $A = 1$ and $B = 2$.

Thus, characteristic equation of the system is $s^2 + s(B - A) + 5 - AB = 0$ i.e. $s^2 + s + 3 = 0$. Therefore, option (c) is correct.

20. (c)

PI controller is used to overcome the problem of steady state error. Therefore, option (c) is correct.

21. (b)

We know that,

$|sI - A|$ gives the characteristic equation of the system. Therefore, option (b) is correct.

22. (c)

Nyquist plot intersects unit circle at $(-1, j0)$, which gives the gain cross-over frequency

$$\text{Phase Margin, PM} = \angle G(j\omega)H(j\omega)\big|_{\omega=\omega_{gc}} + 180°$$

where, ω_{gc} = gain crossover frequency

Here, at gain crossover frequency (ω_{gc}), phase angle of open loop transfer function is –180°. Thus,

$$\text{PM} = -180° + 180°$$

$$\text{PM} = 0 \text{ degree}$$

23. (a)

We know that, for an LTI system,

$$x(t) = A\cos(\omega_0 t + \phi_1) \longrightarrow \boxed{G(j\omega)} \longrightarrow y(t) = B\cos(\omega_0 t + \phi_2)$$

$$x(t) = A\cos(\omega_0 t + \phi_1)$$

then, $B = A\left|G(j\omega)\right|_{\omega=\omega_0}$

$$\phi_2 = \phi_1 + \angle G(j\omega)\big|_{\omega=\omega_0}$$

Now, on comparison, we get

$$B = 1;\ A = \frac{\sqrt{3}}{2}$$

We have, $$|G(j\omega)| = \frac{B}{A}$$

$$|G(j\omega)|_{\text{at } \omega = 2 \text{ rad/sec}} = \frac{2}{\sqrt{3}}$$

As $\phi_2 = -\frac{\pi}{3}$ and $\phi_1 = -\frac{\pi}{2}$ then, $\angle G(j\omega)_{\omega = 2 \text{ rad/sec}} = \phi_2 - \phi_1$

$$= -\frac{\pi}{3} - \left(-\frac{\pi}{2}\right) = \frac{\pi}{6}$$

Since the system has one pole and one zero, let the Transfer function of the system be

$$G(s) = \frac{Ks}{(s + A)}$$

$$G(j\omega) = \frac{j\omega K}{(j\omega + A)}$$

$$|G(j\omega)|_{\omega = 2 \text{ rad/sec}} = \left|\frac{2jK}{(j2 + A)}\right| = \frac{2K}{\sqrt{A^2 + 4}} = \frac{2}{\sqrt{3}} \quad \text{...(i)}$$

$$\angle G(j\omega)|_{\omega = 2} = \frac{\pi}{2} - \tan^{-1}\frac{\omega}{A} = \frac{\pi}{6}$$

$$\frac{\pi}{2} - \frac{\pi}{6} = \tan^{-1}\left(\frac{2}{A}\right)$$

$$\tan\frac{\pi}{3} = \frac{2}{A}$$

$$A = \frac{2}{\sqrt{3}}$$

Now, substituting $A = \frac{2}{\sqrt{3}}$ in equation (i), we get

$$\frac{2K}{\sqrt{\frac{4}{3} + 4}} = \frac{2}{\sqrt{3}}$$

$$2\sqrt{3}K = 2\sqrt{\frac{16}{3}}$$

$$2\sqrt{3}K = \frac{2 \times 4}{\sqrt{3}}$$

$$\frac{2 \times \sqrt{3} \times \sqrt{3}}{8} = \frac{1}{K}$$

$$K = \frac{4}{3}$$

Therefore, $$T(s) = \frac{\frac{4}{3}s}{s+\frac{2}{\sqrt{3}}}$$

24. (c)

- Initial slope of –40 dB/dec implies double poles at origin, thus the transfer function has the term

$$\frac{K}{s^2} = \frac{K}{(j\omega)^2} \quad \text{...(i)}$$

The initial slope of the line intersects the ω axis at ω = 8 rad/sec. Thus,

$$|H(j\omega)| = 20\log K - 20\log \omega^2 = 0 \quad \text{... at } \omega = 8 \text{ rad/sec}$$

$$20\log K = 20\log (8)^2$$

$$K = 64 \quad \text{...(ii)}$$

- At ω = 3 rad/sec, slope changes to –20 dB/dec, it shows the presence of zero at ω = 3.

Thus, the term $\left(1+\frac{s}{3}\right)$ ...(iii)

- At ω = 15 rad/sec, slopes changes to –18 dB/oct

We know that, –20 dB/dec = –6 dB/oct

–18 dB/oct = –60 dB/dec

Thus, the slope changes by (–60 + 20) = –40 dB/dec indicating, presence of two poles at ω = 15,

thus the term $\frac{1}{\left(1+\frac{s}{15}\right)^2}$ ...(iv)

Now, on combining (i), (ii), (iii) and (iv), we get

$$T(s) = 64\frac{\left(\frac{s}{3}+1\right)}{\left(\frac{s}{15}+1\right)^2 s^2}$$

25. (c)

We have closed loop transfer function as,

$$T(s) = \frac{a_{n-1}s + a_n}{s^n + a_1 s^{n-1} + \ldots + a_{n-1}s + a_n}$$

As the system has unity feedback, then open loop transfer function is given as

$$G(s)H(s) = \frac{a_{n-1}s + a_n}{s^n + a_1 s^{n-1} + \ldots + (a_{n-1}s + a_n) - (a_{n-1}s + a_n)}$$

$$G(s)H(s) = \frac{a_{n-1}s + a_n}{s^n + a_1 s^{n+1} + \ldots . a_{n-2}s^2}$$

Now, error coefficients,

$$k_p = \lim_{s\to 0} G(s)H(s) \; ; k_v = \lim_{s\to 0} sG(s)H(s)$$

$$k_p = \lim_{s\to 0} \frac{(a_{n-1}s + a_n)}{s^2(s^{n-2} + a_1 s^{n-3} \ldots + a_{n-2})} = \infty ;$$

$$k_v = \lim_{s\to 0} \frac{s(a_{n-1}s + a_n)}{s^2(s^{n-2} + a_1 s^{n-3} \ldots + a_{n-2})} = \infty ;$$

$$k_a = \lim_{s\to 0} s^2 G(s)H(s) = \lim_{s\to 0} \frac{s^2(a_{n-1} + a_n)}{s^2\left(s^{n-2} + a_1 s^{n-3} + \ldots + a_{n-2}\right)}$$

$$k_a = \left(\frac{a_n}{a_{n-2}}\right)$$

Now, steady state error for

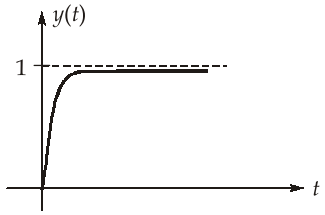
$$\text{Step input} = \frac{A}{k_p} = \frac{A}{\infty} = 0$$

$$\text{ramp input} = \frac{A}{k_v} = \frac{A}{\infty} = 0$$

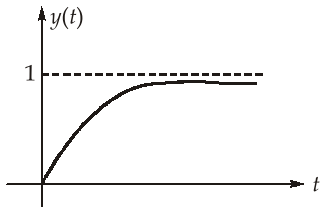
$$\text{parabolic input} = \frac{A}{k_a} = \frac{A}{\left(\frac{a_n}{a_{n-2}}\right)} = \frac{A(a_{n-2})}{a_n}$$

26. (b)

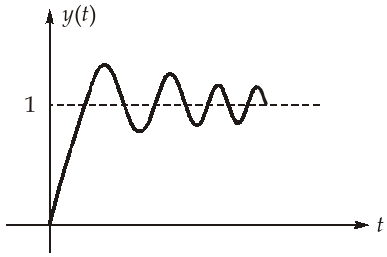
- For critically damped system, $\xi = 1 \Rightarrow$ roots are real and equal



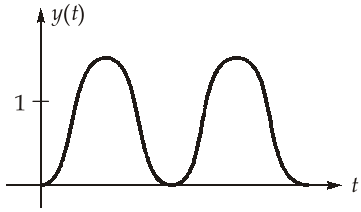
- For over damped system, $\xi > 1 \Rightarrow$ roots are real and unequal



- For underdamped system, $\xi < 1 \Rightarrow$ roots are complex conjugate



- For undamped system, $\xi = 0 \Rightarrow$ roots are symmetric to $j\omega$-axis



27. (d)

All the statments are correct.

28. (d)

Phase margin is calculated at gain crossover frequency. Thus, statement 2 is not correct.

29. (a)

We know that,

$$\angle G(j\omega)H(j\omega) = -\tan^{-1}\left(\frac{\omega A}{2}\right) - \tan^{-1}\left(\frac{\omega A}{1}\right) - \tan^{-1}\left(\frac{3\omega A}{1}\right)$$

At $\omega = \omega_{pc}$, $\quad \angle G(j\omega)H(j\omega)\big|_{\omega=\omega_{pc}} = -180°$

$$-\tan^{-1}\left(\frac{\omega_{pc}A}{2}\right) - \tan^{-1}(\omega_{pc}A) - \tan^{-1}(3\omega_{pc}A) = -180°$$

As, $\omega_{pc} = 1$ rad/sec, then

$$\tan^{-1}\left(\frac{A}{2}\right) + \tan^{-1}(A) + \tan^{-1}(3A) = 180°$$

$$\tan^{-1}\left(\frac{A}{2}\right) + \tan^{-1}\left(\frac{4A}{1-3A^2}\right) = 180°$$

$$\tan^{-1}\left(\frac{\frac{A}{2} + \frac{4A}{1-3A^2}}{1 - \frac{2A^2}{1-3A^2}}\right) = 180°$$

$$\frac{\frac{A}{2} + \frac{4A}{1-3A^2}}{1 - \frac{2A^2}{1-3A^2}} = 0$$

$$\frac{A}{2} + \frac{4A}{1-3A^2} = 0$$

$$A(1 - 3A^2) + 8A = 0$$

$$A - 3A^3 + 8A = 0$$

$$9A = 3A^3$$

$$3A^2 = 9$$
$$A^2 = 3$$
$$A = \sqrt{3};\ -\sqrt{3}$$

$A = -\sqrt{3}$ is discarded as for $A = -\sqrt{3}$, the system become unstable. Thus, $A = \sqrt{3}$.

30. (d)

31. (b)

- Gain Margin 0 dB, it implies
$$-20 \log a = 0$$
$$a = 1$$
For $a < 1$, system is stable
$a > 1$, system is unstable
$a = 1$, system is marginally stable
Thus, statement (i) is correct.
- Phase margin is determined at gain cross over frequency ω_{gc}, which depends on system gain. The gain cross-over frequency is determined by
$$|G(j\omega)H(j\omega)|_{\omega = \omega_{gc}} = 1$$
Phase angle at $\omega = \omega_{gc}$ is $\angle G(j\omega_{gc})H(j\omega_{gc})$, thus we have
$$PM = \angle G(j\omega_{gc})H(j\omega_{gc}) + 180°$$
Thus, statement (ii) is incorrect.

32. (b)

The characteristic equation of the system is $P(s) = s^4 + 8s^3 + 24s^2 + 32s + k$
Now, forming Routh-Hurtwitz table,

s^4	1	24	k
s^3	8	32	
s^2	$\frac{24\times8-32}{8} = 20$	k	
s^1	$32 - \frac{8k}{20}$		
s^0	k		

Now, for stable system

$$k > 0 \quad \text{...(i)}$$

and
$$32 - \frac{8k}{20} > 0$$
$$32 \times 20 - 8k > 0$$
$$\frac{32\times20}{8} > k$$
$$80 > k$$

Thus, for stable system, k must be less than 80.

33. (d)

We know that, in a root locus plot,

centroid lies on real axis only i.e., imaginary axis coordinate is zero. And the real axis coordinate is given as

$$\sigma = \frac{\Sigma \text{ real part of all the poles} - \Sigma \text{ real part of all the zeros}}{(\text{number of poles}) - (\text{number of zeros})}$$

Now, zeros = $-A$; Number of zeros, $Z = 1$

Poles = 0, $-B$, -1 and -1; Number of poles, $P = 4$

$$\text{centroid} = \frac{(0 - B - 1 - 1) - (-A)}{4 - 1} = -5$$

$$-B - 2 + A = -15$$

$$A - B = -13$$

Therefore, option (d) is correct.

34. (d)

- The instrument used for plotting the root locus is called spirule.
- The root locus must be symmetrical with respect to the real axis of the s-plane because complex roots appear as complex conjugate pairs.
- The root locus shows the locus of the poles of the closed loop system with variation of open loop gain k. Thus, it could be used to determine the range of k for which the system is stable i.e. the roots lie on the left side of the $j\omega$ axis.

Thus, all the given statements are correct.

35. (d)

In an 8085 microprocessor, PUSH operations requires more clock cycles than POP operation. In a PUSH operation, the stack pointer needs to be pre-decremented before writing registers, whereas a POP operation uses the address already in the stack pointer. PUSH instruction takes 1 T-state (6 clock cycles) for fetch and decoding operation and 2 T-states (6 clock cycles) for write operation; whereas POP instruction takes 4 clock cycles for fetch and decoding operation and 2 T-states (6 clock cycles) for read operation. Hence, Statement (I) is false and Statement (II) is correct.

36. (b)

The 8085 microprocessor uses multiplexed address/data lines (AD7-AD0). The ALE (Address Latch Enable) is a signal used to demultiplex the address and data lines, using an external latch. ALE is a positive going pulse generated when a new operation is started by microprocessor. When the pulse goes high i.e. ALE = 1, it makes address bus enable and when ALE = 0, it makes data bus enable. Both Statement (I) and Statement (II) are true but Statement (II) is not the correct explanation of Statement (I).

37. (c)

Phase margin gives the better estimate of damping ratio than the gain margin. Hence, Statement (II) is not correct.

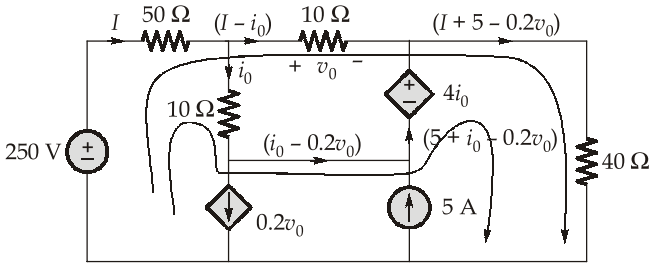
38. (c)

Statement (I) is correct as a stable system might become unstable on giving negative feedback to it. And, a system's gain always decreases on giving feedback (negative) to it. Therefore, Statement-(II) is incorrect.

Section B : Network Theory-1

39. (c)

Let V_1 be the node voltage.



Applying KVL around the outer loop,

$-250 + 50I + 10(I - i_0) + 40(I + 5 - 0.2v_0) = 0$

$100I - 10i_0 - 8v_0 = 50$ [Here, $v_0 = 10(I - i_0)$]

$100I - 10i_0 - 80\,(I - i_0) = 50$

$\Rightarrow \quad 2I + 7i_0 = 5$ ...(i)

On applying KVL,

$-250 + 50I + 10i_0 - 4i_0 + 40(I + 5 - 0.2v_0) = 0$

$90I + 6i_0 + 200 - 8v_0 = 250$

$90I + 6i_0 + 200 - 80(I - i_0) = 250$

$I + 8.6i_0 = 5$

$\Rightarrow \quad I = 5 - 8.6i_0$

Using equation (i),

$2(5 - 8.6i_0) + 7i_0 = 5$

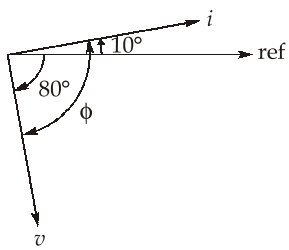
$\Rightarrow \quad i_0 = 0.49$ A

40. (b)

Given, $v = 100\cos(100t - 80°)$V

$i = 10\cos(100t + 10°)$A

The vector diagram is



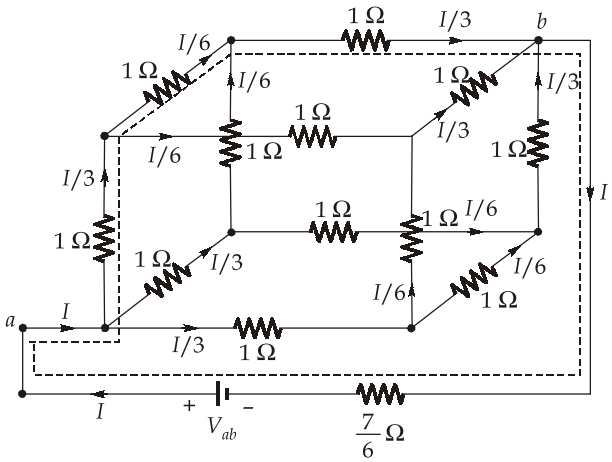
As $\phi = 90°$ and i leads V, it implies that the element is capacitor.

$$X_C = \frac{V_m}{I_m} = \frac{100}{10} = 10\ \Omega$$

$$\therefore \quad C = \frac{1}{\omega X_C} = \frac{1}{100 \times 10} = 1 \times 10^{-3} = 1\ \text{mF}$$

41. (d)

Since the path resistance between a and b are equal in all the paths, we can apply current division rule and then obtain the equivalent resistance by ohm's law.



Apply KVL in the shown path,

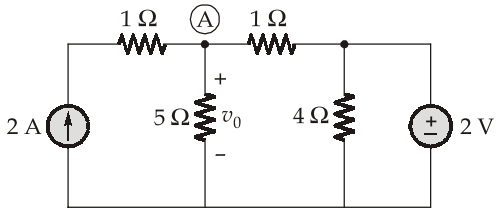
$$-V_{ab} + \left(\frac{I}{3} \times 1\right) + \left(\frac{I}{6} \times 1\right) + \left(\frac{I}{3} \times 1\right) + \left(\frac{7}{6} \times I\right) = 0$$

$$V_{ab} = \left(\frac{5}{6} + \frac{7}{6}\right) I = \frac{12}{6} I = 2I$$

$$\Rightarrow \quad V_{ab} = 2I$$

42. (a)

At steady state, the inductances would behave as short circuit against d.c. excitation at $t = \infty$. Similarly, capacitor would act as open circuit against d.c. excitation at $t = \infty$. At steady state, the equivalent circuit can be obtained as below:



Apply KCL at node (A),

$$-2 + \frac{v_0}{5} + \frac{v_0 - 2}{1} = 0$$

$$v_0\left(\frac{1}{5} + 1\right) = 2 + 2$$

$$v_0\left(\frac{6}{5}\right) = 4$$

$$\Rightarrow \quad v_0 = \frac{20}{6} = \frac{10}{3} = 3.333 \text{ V}$$

43. (c)

The input impedance of the given circuit is given by

$$Z_{in} = 3 + [1 \| j2] = 3 + \frac{(1 \times j2)}{(1 + j2)} = 3 + \frac{j2(1 - j2)}{5} = 3 + j0.4 + 0.8$$

$$\Rightarrow \quad Z_{in} = 3.8 + j0.4\ \Omega$$

The input current will be in phase with the supply voltage provided the reactive part of the impedance does not exist after inserting the capacitor in series.

$$\Rightarrow \quad \frac{j}{\omega C} = j0.4$$

$$\Rightarrow \quad C = \frac{1}{\omega \times 0.4} = \frac{1}{100 \times 0.4} = 0.025$$

$$\Rightarrow \quad C = 25 \text{ mF}$$

44. (d)

$$Y_R = \frac{1}{R}\angle 0° = (0.5 + j0) \text{ mho}$$

$$Y_C = \frac{1}{X_C}\angle 90° = \frac{1}{1.25}\angle 90° = 0.8\angle 90° = j0.8 \text{ mho}$$

$$\therefore \quad \text{Net admittance, } Y = Y_R + Y_C$$

$$= (0.5 + j0.8) \text{ mho}$$

$$\Rightarrow \quad I = EY = 5\angle 0° \times (0.5 + j0.8)$$

$$= (2.5 + j4)\text{A}$$

45. (c)

The input impedance is,

$$Z_{in} = 5 + [-j4 \| (2 + j2)]$$

$$= 5 + \frac{-j4(2 + j2)}{-j4 + 2 + j2}$$

$$= 5 + \frac{8 - 8j}{2 - 2j}$$

$$= 5 + \frac{(8 - 8j)(2 + 2j)}{8}$$

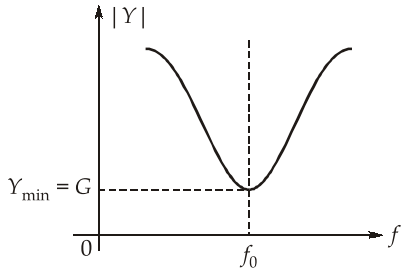
$$= 5 + \frac{16 + 16j - 16j + 16}{8}$$

$$\Rightarrow \quad Z_{in} = 9\ \Omega$$

As the input impedance is purely resistive, the p.f. would be unity.

46. (a)

- The admittance of a parallel RLC circuit is given as $Y = G + j(B_C - B_L)$. At resonance, $B_C = B_L$, thus the net susceptance is zero and the the net admittance is minimum; $Y_{min} = G$.



- Since net admittance is minimum, the net impedance is maximum and purely resistive. Thus, the current is minimum and in phase with the applied voltage.

Hence, statements 1, 2 and 3 are correct.

47. (a)

At resonance, imaginary part of input impedance must be zero.

We have,
$$Z_{in} = \frac{-j}{2\omega} + [j\omega \| 1] = \frac{-j}{2\omega} + \frac{j\omega}{1+j\omega}$$
$$= \frac{-j}{2\omega} + \frac{j\omega(1-j\omega)}{1+\omega^2}$$
$$= \frac{-j}{2\omega} + \frac{j\omega}{1+\omega^2} + \frac{\omega^2}{1+\omega^2}$$

At resonance,
$$\frac{-1}{2\omega} + \frac{\omega}{1+\omega^2} = 0$$
$$\frac{\omega}{1+\omega^2} = \frac{1}{2\omega}$$
$$2\omega^2 = 1 + \omega^2$$
$$\Rightarrow \quad \omega = 1 \text{ rad/sec}$$

48. (d)

- For series RL circuit, $Q = \frac{X_L}{R} = \frac{\omega L}{R}$
- For series RC circuit, $Q = \frac{X_C}{R} = \frac{1}{\omega RC}$
- For parallel RL circuit, $Q = \frac{R}{X_L} = \frac{R}{\omega L}$
- For parallel RC circuit, $Q = \frac{R}{X_c} = \omega RC$

49. (d)

Given, $v_L = 300 \sin(1000t)$ V

$R = 20\ \Omega$

$\phi = 45°$

$V_{L(max)} = 2V_{C(max)}$

$\sqrt{2}V_L = 2\sqrt{2}V_C$

$I \times X_L = 2I \times X_C$

$X_L = 2X_C$ ...(i)

We have, $\cos\phi = \dfrac{R}{Z}$

$\Rightarrow \cos 45° = \dfrac{20}{Z}$

$\Rightarrow Z = 20\sqrt{2}\ \Omega$

For series R-L-C circuit,

$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

Using equation (i),

$$20\sqrt{2} = \sqrt{(20)^2 + (2X_C - X_C)^2}$$

$$800 = 400 + X_C^2$$

$$X_C^2 = 400$$

$\Rightarrow X_C = 20\ \Omega$

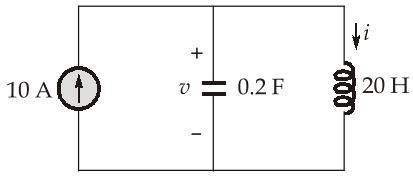
50. (b)

For $t < 0$, $10\,u(t) = 0$. At $t = 0^-$, since the circuit is source-free, the capacitor is uncharged.

$\therefore v(0^-) = 0$ V

Similarly, $i(0^-) = 0$ A

For $t > 0$, $10u(t) = 10$, so the equivalent circuit is,



Since the inductor current and capacitor voltage cannot change abruptly,

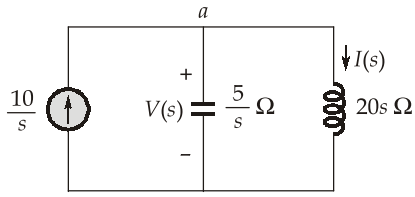
$i(0^+) = i(0^-) = 0$ A

$v(0^+) = v(0^-) = 0$ V

$\therefore v(0) = \dfrac{L di(0)}{dt}$

$\Rightarrow \dfrac{di(0)}{dt} = \dfrac{v(0)}{L} = 0$ A/s

The s-domain equivalent of the above circuit is,



Applying KCL at node *a*,

$$\frac{-10}{s}+\frac{V(s)}{\left(\frac{5}{s}\right)}+\frac{V(s)}{20s}=0$$

$$V(s)\left[\frac{s}{5}+\frac{1}{20s}\right]=\frac{10}{s}$$

$$\Rightarrow \quad V(s)\times\left[\frac{4s^2+1}{20}\right]=10$$

$$\Rightarrow \quad V(s)=\left[\frac{50}{s^2+\left(\frac{1}{2}\right)^2}\right]$$

Taking inverse Laplace transform on both sides,

$$v(t)=\frac{50}{\left(\frac{1}{2}\right)}\times\sin\left(\frac{1}{2}t\right)=100\sin(0.5t)\text{ V}$$

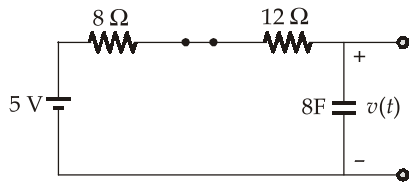
51. (c)

At $t = 100^-$, it is given that $v(100^-) = -3$ V.

Since the voltage across the capacitor cannot change instantaneously, $v(100^-) = v(100^+) = -3$ V.

The switching takes place at time $t = 100$.

For $t \geq 100$:



The voltage across the capacitor is,

$$v(t) = v(\infty) + [v(100) - v(\infty)]e^{-(t-100)/\tau} \qquad \ldots(i)$$

After a long time, the circuit reaches steady state and capacitor acts like an open circuit.

$$\therefore \quad v(\infty) = 5 \text{ V}$$

The thevenin resistance across the capacitor terminals is,

$$R_{Th} = 8 + 12 = 20\ \Omega$$

and the time constant is,

$$\tau = R_{Th}C = 20 \times 8 = 160 \text{ sec}$$

Thus, from equation (i),

$$v(t) = 5 + [-3 - 5]e^{-(t-100)/160}$$
$$v(t) = 5 - 8e^{-(t-100)/160}\ \text{V}$$

At $t = 200$ seconds,

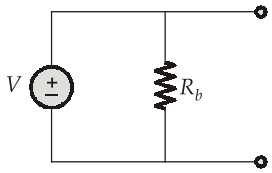
$$v(200) = 5 - 8e^{-(200-100)/160} = (5 - 8e^{-5/8})\ \text{V}$$

52. (b)

- Any resistance in series with current source is redundant.

$\Rightarrow$ "R_a" is redundant element.

- Any resistance in parallel with voltage source is redundant.



$\Rightarrow$ "R_b" is redundant element.

53. (c)

From circuit P; we get

$$\frac{E}{R} = 0.5\ \text{A} \Rightarrow E = 0.5R \quad \ldots(\text{i})$$

From circuit Q, we get $\dfrac{E}{R_1} = 0.4\ \text{A} \Rightarrow E = 0.4R_1$

$\therefore$ $R_1 = R + R'$ i.e., $E = 0.4(R + 5)$

$$E = 0.4R + 2 \quad \ldots(\text{ii})$$

From circuit R, we get,

$$\frac{E}{R_2} = 0.2 \Rightarrow E = 0.2R_2$$

$\therefore$ $R_2 = R_1 + R'' = R + 5 + R''$

$$E = 0.2(R + 5 + R'') = 0.2R + 1 + 0.2R'' \quad \ldots(\text{iii})$$

From equation (i) and (ii), we get

$$0.5R = 0.4R + 2$$
$$0.1R = 2$$
$$R = 20\ \Omega \quad \ldots(\text{iv})$$

On substituting $R = 20\ \Omega$ in equation (i) we get $E = 10$ volt. ...(v)

Using (iv), and (v) in equation (iii), we get

$$10 = (0.2 \times 20) + 1 + 0.2R''$$
$$10 = 4 + 1 + 0.2R''$$
$$\frac{5}{0.2} = R''$$
$$R'' = 25\ \Omega \quad \ldots(\text{vi})$$

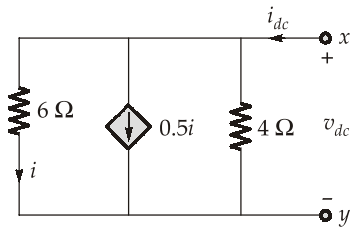
Now, in circuit 'Q' is $E \times I = 10 \times 0.4 = 4$ Watt

Therefore, Q is matched to 1.

Now, in circuit '*P*' value of $R_{th} = 20\ \Omega$ and in circuit '*R*', total extra resistance added is '$(R_2 - R)$' i.e.,

$$\left(50 - \frac{10}{0.5}\right)\Omega = 30\ \Omega$$

54. (c)



The current, $$i_{dc} = \frac{v_{dc}}{4} + 0.5i + i$$

$$i_{dc} = 0.25\ v_{dc} + 1.5i \quad \text{...(i)}$$

But $$i = \frac{v_{dc}}{6}$$

From equation (i), $$i_{dc} = 0.25v_{dc} + 1.5\left(\frac{v_{dc}}{6}\right)$$

$$i_{dc} = 0.25v_{dc} + 0.25v_{dc}$$

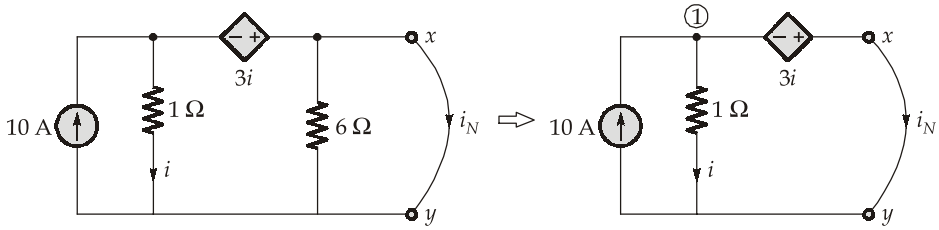
$$i_{dc} = 0.5v_{dc}$$

$\Rightarrow$ $$R_{Th} = \frac{v_{dc}}{i_{dc}} = \frac{1}{0.5} = 2\ \Omega$$

55. (a)

56. (c)

To determine Norton's equivalent current source, we consider short circuit across *x*-*y* terminal as shown in figure.



Apply KCL at node (1),

$$-10 + i + i_N = 0 \quad \text{...(i)}$$

Apply KVL at node (1),

$$-i - 3i = 0$$

$\Rightarrow$ $$i = 0$$

From equation (i), $$-10 + 0 + i_N = 0$$

$\Rightarrow$ $$i_N = 10\ \text{A}$$

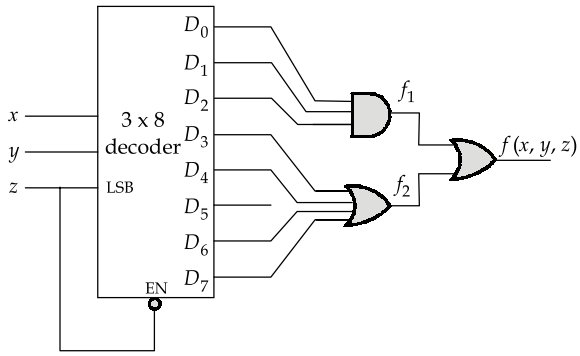
57. (a)

The power supply which is actually consumed in an AC circuit is called Active Power.

Section C : Digital Circuits-1

58. (c)

The given 3 × 8 decoder is active low output type. The circuit can be redrawn as shown in the figure below:



If $z = 1$, then decoder is disabled and all outputs D_0-D_7 are 0. If $z = 0$, then EN = 1 (Since input LSB = 0, we will get output only for even values)

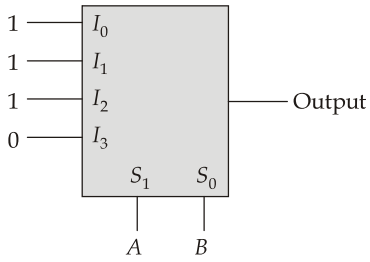
The outputs D_0, D_2, D_4 and D_6 are active and outputs D_1, D_3, D_5 and D_7 are inactive.

We have, $f_1 = D_3 + D_4 + D_6 + D_7$. Since D_3 and D_7 remain inactive, we have, $f_1 = \Sigma m(4, 6)$.

Here, $f_2 = 0$ because all three inputs D_0, D_1 and D_2 can never be 1 at the same time.

Thus, $f(x, y, z) = f_1 + f_2 = \Sigma m(4, 6)$

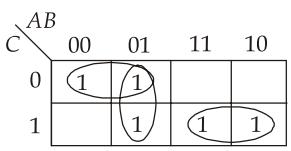
59. (c)



$$\text{Output} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B$$
$$= \bar{A} + \bar{B}$$

60. (a)

$$F = (A+B)(A+\bar{A}+\bar{B})C + \bar{A}(B+\bar{C}) + \bar{A}B + ABC$$
$$= AC + BC + \bar{A}B + \bar{A}\bar{C} + \bar{A}B + ABC$$
$$= AC + BC + \bar{A}(B+\bar{C})$$



Using K-map, we get $F = AC + \bar{A}B + \bar{A}\bar{C}$

61. (d)

$\because$ Both the inputs of the Ex-NOR gate can never be equal since only one output of the decoder circuit will be active at a time. So, f is always equal to zero.

62. (d)

Two TTL gates with "open-collector" outputs directly connected together, function as a "wired AND" logic gate.

Thus, $$f = (\overline{AB})(\overline{CD}) = (\bar{A} + \bar{B})(\bar{C} + \bar{D})$$

63. (d)

Given that,

$$f(A, B, C) = \Pi M(1, 3, 4, 5) = \Sigma m(0, 2, 6, 7)$$

Now,

	I_0	I_1	I_2	I_3	
$\bar{A}$	⓪	1	②	3	
A	4	5	⑥	⑦	
	$\bar{A}$	0	1	A	⇒Corresponding MUX Inputs

$\therefore$ Required inputs are, $I_0 = \bar{A}$, $I_1 = 0$, $I_2 = 1$ and $I_3 = A$

64. (b)

$$(09)_{10} \xrightarrow{\text{Excess-3}} 1001 + 0011 = 1100$$

$$(09)_{10} \xrightarrow{\text{BCD}} 1001$$

$$(10)_{10} \xrightarrow{\text{Gray Code}} 1111$$

$$(10)_{10} \xrightarrow{\text{Binary Code}} 1010$$

65. (b)

From the given 8 × 1 MUX,

$$Y(A, B, C) = \bar{A}\bar{B}\bar{C}(1) + \bar{A}\bar{B}C(1) + \bar{A}\bar{B}C\bar{D} + \bar{A}BC(0) + A\bar{B}\bar{C}(1) + A\bar{B}C(0) + AB\bar{C}(\bar{D}) + ABC(0)$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C} + AB\bar{C}\bar{D}$$

$$Y(A, 1, C) = \bar{A}\bar{C}\bar{D} + A\bar{C}\bar{D} = \bar{C}\bar{D}$$

66. (c)

A reflexive code is a code where the code for 9 is the complement of code for 0 and so on.

Ex:

Excess-3 code for 9 : 1001 + 0011 = 1100

Excess-3 code for 0 : 0000 + 0011 = 0011 which is complement of code for 9.

A sequential code is a code where each succeeding code is one binary number more than the preceeding code. Excess-3 code satisfies both these properties.

67. (b)

Given, $F(P, Q) = ((0 + P) \oplus (1 + Q)) \oplus ((1 + Q) \oplus (P \oplus Q))$

$= (P \oplus \bar{Q}) \oplus (\bar{Q} \oplus (P \oplus Q))$

$= (P \oplus \bar{Q}) \oplus ((\bar{Q} \oplus P) \oplus (\bar{Q} \oplus Q))$

$= (P \oplus \bar{Q}) \oplus ((\bar{Q} + P) \oplus 1)$

$= (P \oplus \bar{Q}) \oplus \overline{(P \oplus \bar{Q})}$

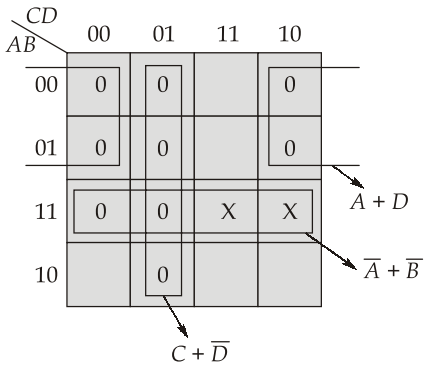
$F(P, Q) = 1$

$\therefore \quad \bar{F}(P, Q) = 0$

68. (d)

Given, $f(A, B, C, D) = \Sigma m\{3, 7, 8, 10, 11\} + \Sigma d\{14, 15\}$

$= \pi(0, 1, 2, 4, 5, 6, 9, 12, 13)\ \pi d\{14, 15\}$



$f = (A + D)(\bar{A} + \bar{B})(C + \bar{D})$

69. (c)

Given, $F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$

$\bar{F} = \overline{(X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)}$

$= (\overline{X + Y + Z}) + (\overline{\bar{X} + Y}) + (\overline{\bar{Y} + Z})$

$= \bar{X}\bar{Y}\bar{Z} + X\bar{Y} + Y\bar{Z}$

$= \bar{Y}(X + \bar{X}\bar{Z}) + Y\bar{Z}$

$= \bar{Y}(X + \bar{Z}) + Y\bar{Z} = X\bar{Y} + \bar{Z}$

70. (c)

$Z = a(b + \bar{c})$

$Z = ab + a\bar{c}$

Representing the Boolean expression on K-Map,

a \ bc	00	01	11	10
0				
1	1		1	1

$\therefore \quad Z(a, b, c) = \Sigma m(4, 6, 7)$

71. (d)

Let output of XOR gate be f',

$\therefore \quad f' = f_1 \oplus f_2$

$= \Sigma m(0, 1, 4, 8, 13) \oplus \Sigma m(2, 6, 14, 15)$

$f' = \Sigma m(0, 1, 2, 4, 6, 8, 13, 14, 15)$

The output of EXNOR gate,

$f = f_1 \odot f_3$

$= \Sigma m(0, 1, 2, 4, 6, 8, 13, 14, 15) \odot \Sigma m(4, 8, 13, 15)$

$f = \Sigma m(4, 8, 13, 15)$

72. (c)

Excess-3 code can be obtained by adding 3 to each decimal digit, and obtain the corresponding 4-bit binary number.

Given, Excess-3 number,

$$\underbrace{1100}_{C}\ \underbrace{1010}_{A}\ \underbrace{0011}_{3} \cdot \underbrace{0111}_{7}\ \underbrace{0101}_{5}$$

The binary code from given Excess-3 code can be obtained as,

$$\begin{array}{ccccc} 1100 & 1010 & 0011 & 0111 & 0101 \\ -0011 & -0011 & -0011 & -0011 & -0011 \\ \hline 1001 & 0111 & 0000 & 0100 & 0010 \end{array}$$

$\therefore$ The decimal equivalent is $(100101110000 \cdot 01000010)$

$= (970.42)_{10}$

73. (c)

Truth Table for 2-to-4 decoder:

A	B	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$\therefore \quad Y_0 = \bar{A}\bar{B}; \quad Y_1 = \bar{A}B$

$Y_2 = A\bar{B}; \quad Y_3 = AB$

$F(A, B, C, D) = \bar{S_1}\bar{S_0} I_0 + \bar{S_1} S_0 I_1 + S_1 \bar{S_0} I_2 + S_1 S_0 I_3$

$= \bar{C}\bar{D}(\bar{A}\bar{B}) + \bar{C}D(0) + C\bar{D}(1) + CD(AB)$

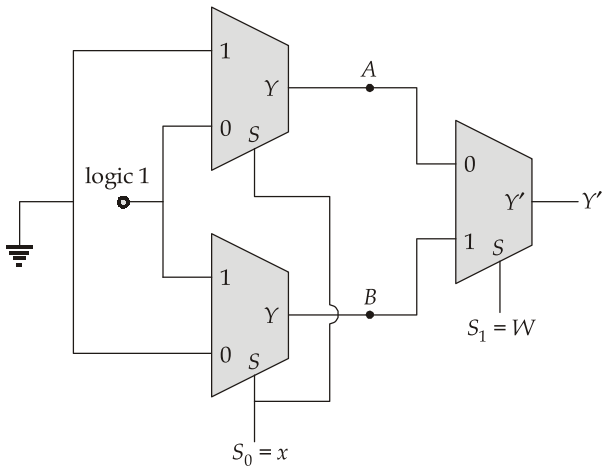
$= \bar{A}\bar{B}\bar{C}\bar{D} + C\bar{D} + ABCD$

By using 4-variable K-map,

AB \ CD	00	01	11	10
00	1			1
01				1
11			1	1
10				1

$\therefore$ $F(A, B, C, D) = \Sigma m(0, 2, 6, 10, 14, 15)$

74. (d)



output, $A = \overline{S}_0(1) + S_0(0) = \overline{x}(1) = \overline{x}$

output, $B = \overline{S}_0(0) + S_0(1) = x$

output $Y' = \overline{S_1}A + S_1B = \overline{W}\,\overline{x} + W\,x$

$Y' = W \odot x$, which represents XNOR logic.

75. (b)

ROM is a non-volatile memory which retains its data even when power is turned off. Both statement (I) and (II) are correct and statement (II) is not the correct explanation of statement (I).

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