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# ESE 2024 : Prelims Exam
CLASSROOM TEST SERIES

# E & T ENGINEERING

**Test 6**

**Section A :** Electronic Devices & Circuits + Analog Circuits

**Section B :** Control Systems-1 + Microprocessors and Microcontroller-1

**Section C :** Network Theory-2 + Digital Circuits-2

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1. | (c) | 16. | (b) | 31. | (c) | 46. | (c) | 61. | (b) |
| 2. | (a) | 17. | (a) | 32. | (a) | 47. | (c) | 62. | (c) |
| 3. | (d) | 18. | (b) | 33. | (d) | 48. | (d) | 63. | (a) |
| 4. | (c) | 19. | (c) | 34. | (a) | 49. | (a) | 64. | (c) |
| 5. | (a) | 20. | (b) | 35. | (b) | 50. | (a) | 65. | (d) |
| 6. | (c) | 21. | (a) | 36. | (c) | 51. | (b) | 66. | (a) |
| 7. | (b) | 22. | (c) | 37. | (c) | 52. | (c) | 67. | (a) |
| 8. | (d) | 23. | (d) | 38. | (b) | 53. | (d) | 68. | (b) |
| 9. | (c) | 24. | (c) | 39. | (a) | 54. | (a) | 69. | (a) |
| 10. | (b) | 25. | (b) | 40. | (a) | 55. | (b) | 70. | (d) |
| 11. | (d) | 26. | (c) | 41. | (b) | 56. | (a) | 71. | (a) |
| 12. | (a) | 27. | (d) | 42. | (a) | 57. | (b) | 72. | (c) |
| 13. | (c) | 28. | (c) | 43. | (c) | 58. | (a) | 73. | (c) |
| 14. | (c) | 29. | (b) | 44. | (b) | 59. | (c) | 74. | (b) |
| 15. | (d) | 30. | (a) | 45. | (d) | 60. | (c) | 75. | (b) |

## DETAILED EXPLANATIONS
### Section A : Electronic Devices & Circuits + Analog Circuits

**1. (c)**

At flat-band condition, there is no band bending in the semiconductor and, as a result, zero net space charge within the semiconductor region.

**2. (a)**

For $p^+n$ junction,

$$\frac{1}{C_{dep}^2} = \frac{W_{dep}^2}{A^2 \epsilon_s^2} = \frac{2(\phi_{bi} + V_r)}{qN_d \epsilon_s A^2}$$

$$\therefore \quad \text{slope} = \frac{2}{qN_d \epsilon_s A^2} = 2 \times 10^{23} F^{-2} V^{-1}$$

$$\therefore \quad N_d = \frac{2}{2 \times 10^{23} \times 1.6 \times 10^{-19} \times 12 \times 8.85 \times 10^{-14} \times 10^{-8}}$$

$$\therefore \quad N_d = 5.88 \times 10^{15} \text{ cm}^{-3}$$

**3. (d)**

According to space charge neutrality, the total negative space charge per unit area in p-side is equal to total positive space charge per unit area in n-side.

$$\therefore \quad \frac{1}{2}\left[0.8 \times 8 \times 10^{14}\right] = x_n \times 3 \times 10^{14}$$

$$\therefore \quad x_n = 1.067 \ \mu\text{m}$$

The depletion width, $W = x_n + x_p$

$$\therefore \quad W = 1.067 + 0.8 = 1.867 \ \mu\text{m}$$

**4. (c)**

We know that,

$$\text{Resistance, } R = \frac{\rho l}{A}$$

$$R \propto \rho \propto \frac{1}{N_D q \mu_n + N_A q \mu_p}$$

$$\therefore \quad R_1 \propto \frac{1}{N_D q \mu_n}; 0.5R_1 \propto \frac{1}{N_A q \mu_p}$$

From Eienstein relation, $\frac{D}{\mu} = V_T$

$$D = \mu V_T$$

$$\therefore \quad D \propto \mu$$

$$\frac{D_p}{D_n} = \frac{\mu_p}{\mu_n} = \frac{1}{50}$$

$$\therefore \quad \frac{R_1}{0.5R_1} = \frac{N_A q\mu_p}{N_D q\mu_n}$$

$$\Rightarrow \quad 2 = \frac{N_A}{N_D} \times \frac{1}{50}$$

$$\therefore \quad N_A = 100\, N_D$$

**5. (a)**

The overall mobility, $\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2}$

$$\therefore \quad \frac{1}{\mu} = \frac{1}{250} + \frac{1}{500}$$

$$\therefore \quad \mu = 167\ \text{cm}^2/\text{V-s}$$

**6. (c)**

For a n-type MOSFET having p-type substrate, in the depletion mode for $V_{GS} > V_{FB}$, the holes will be depleted with the increase in electrons causing band bending in the downward direction. In the accumulation mode for $V_{GS} < V_{FB}$, more holes are moved toward the interface causing band bending in the upward direction. Hence, option(c) is correct.

**7. (b)**

For an ideal transistor,

$$\alpha = \gamma = 0.999$$

$$\therefore \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.999}{1-0.999} = 999$$

$$\therefore \quad I_C = (1+\beta)I_{CBO} + \beta I_B$$
$$= (1 + 999) \times 10 \times 10^{-6}$$
$$I_C = 10 \times 10^{-3} = 10\ \text{mA}$$

Since, $I_B = 0$, hence $I_E = I_C = 10$ mA

**8. (d)**

Given, $D_p = 100\ \text{cm}^2/\text{s}$

$\tau_p = 3 \times 10^{-7}$ sec

base width, $W = 2\ \mu\text{m}$

We know that, diffusion length, $L_p = \sqrt{D_p \tau_p}$

$$L_p = \sqrt{100 \times 3 \times 10^{-7}} = 54.77\ \mu\text{m}$$

The common emitter current gain,

$$\beta \cong \frac{2L_p^2}{W^2} = \frac{2 \times (54.77 \times 10^{-4})^2}{(2 \times 10^{-4})^2}$$

$$\therefore \quad \beta = 1500$$

**9. (c)**

Given $D_n = 22.5\ \text{cm}^2/\text{s}$

We know that, diffusion current density,

$$J_{n,\text{ diff}} = qD_n\frac{dn}{dx} = qD_n\frac{\Delta n}{\Delta x}$$

$$= 1.6\times10^{-19}\times22.5\times\frac{1\times10^{18}-7\times10^{17}}{0.1}$$

$\therefore$ $J_{n,\text{ diff}} = 10.8\ \text{A/cm}^2$

**10. (b)**

Given, $G_L = 10^{16}\ \text{cm}^{-3}\text{s}^{-1}$

$\tau_n = \tau_p = 10\ \mu\text{s}$

$N_D = 10^{15}\ \text{cm}^{-3}$

excess carrier concentration under illumination,

$$\Delta n = \Delta p = \tau_p G_L = \tau_n G_L = 10\times10^{-6}\times10^{16}$$

$\therefore$ $\Delta n = \Delta p = 10^{11}\ \text{cm}^{-3}$

electron concentration, $n = n_{n0} + \Delta n$

$= N_D + \Delta n$

$= 10^{15} + 10^{11} \simeq 10^{15}\ \text{cm}^{-3}$

hole concentration, $p = \dfrac{n_i^2}{N_D} + \Delta p = \dfrac{(10\times10^{10})^2}{10^{15}} + 10^{11} = 10^{11}\ \text{cm}^{-3}$

**11. (d)**

**12. (a)**

We know that, $V_T = V_{FB} + 2\psi_B + \dfrac{\sqrt{2\epsilon_s qN_A(2\psi_B)}}{C_{ox}}$

$$= -1.1 + 0.84 + \frac{\sqrt{2\times11.9\times8.85\times10^{-14}\times1.6\times10^{-19}\times10^{17}\times0.84}}{6.9\times10^{-7}}$$

$= -0.016\ \text{V} \approx -0.02\ \text{V}$

**13. (c)**

In stimulated emission, an incoming photon of a specific frequency interact with an excited atomic electron, causing it to drop to a lower energy level emitting a photon.

**14. (c)**

We know that,

Conductivity, $\sigma = nq\mu_n + pq\mu_p$

Before illumination, $n_n = n_{n0}$

$p_n = p_{n0}$

After illumination, $n_n = n_{n0} + \Delta n = n_{n0} + \tau_n G$

$p_n = p_{n0} + \Delta p = p_{n0} + \tau_p G$

$\therefore$ $\Delta\sigma = (q\mu_n(n_{n0} + \tau_n G) + q\mu_p(p_{n0} + \tau_p G) - (q\mu_n n_{n0} + q\mu_p p_{n0}))$

$\Delta\sigma = q(\mu_n + \mu_p)\tau_n G \quad (\because \tau_n = \tau_p)$

**15. (d)**

Given, $$\tau_r = \frac{10^9}{N} = \frac{10^9}{10^{19}}\text{sec}$$

$$\tau_{nr} = 10^{-7}\text{ s}$$

We know that, cutoff frequency,

$$f_c = \frac{1}{2\pi\tau}$$

where, $$\frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}} = \frac{1}{10^{-7}} + \frac{10^{19}}{10^9} = 10^{10}$$

$\therefore$ $$\tau = 10^{-10}\text{ sec}$$

$\therefore$ $$f = \frac{1}{2\pi \times 10^{-10}} = 1.6\text{ GHz}$$

**16. (b)**

When the solar cell is exposed to the solar spectrum, a photon with energy less than the bandgap energy, $E_g$ will have no effect on the electrical output power of the solar cell.

**17. (a)**

In a photodetector, carriers are generated in the depletion region . As the width of the depletion region is increased, it allow more photons to be absorbed and generate more electron-hole pairs, thereby increasing the photodetector's sensitivity.

**18. (b)**

For a full-wave rectifier with capacitor filter,

$$\text{Ripple factor, } r = \frac{1}{4\sqrt{3}fCR_L}$$

Also, $$\text{Ripple voltage} = \frac{I_{DC}}{fC}$$

Since a low ripple factor is desired, therefore the capacitor filter should be used when $R_L$ is high and load current is low.

**19. (c)**

% Regulation for a half wave rectifier can be given as

$$\%\text{ regulation} = \frac{R_f}{R_L} \times 100 = \frac{12}{750} \times 100$$

$$= \frac{8}{5} = 1.6\%$$

**20. (b)**

At low frequency, the low internal capacitances offers very high impedance acting as open circuit and the high external bypass and coupling capacitors offers finite impedance, thereby affecting the frequency response of FET transistor at low frequency. At high frequency, the response is affected by the internal capacitances.

**21. (a)**

For negative feedback.

$$(B.W)_f > (B.W)$$

Also, the gain of the amplifier decreases due to negative feedback.

**22. (c)**

$$I_B = \frac{I_C}{\beta} = \frac{4\times10^{-3}}{50} = 0.08\ \text{mA}$$

$$V_C = R_B I_B + 0.7\ \text{V} \qquad [\because V_{CE} = V_C - V_E = V_C]$$

$$R_B = \frac{V_C - 0.7}{I_B} = \frac{2.5-0.7}{0.08}\times10^3$$

$$= \frac{1.80}{0.08}\times10^3 = \frac{180}{8}\times10^3 = 22.5\ \text{k}\Omega$$

$$I_0 = I_E = (1+\beta)I_B = I_C + I_B = 4 + 0.08 = 4.08\ \text{mA}$$

$$R_B \propto \frac{1}{I_B} \propto \frac{1}{I_0}$$

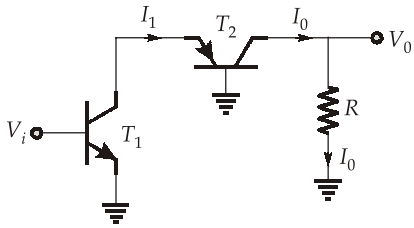
**23. (d)**

The common mode gain of BJT differential amplifier is given as

$$A_{cm} = \frac{-R_C}{2R_E}$$

Since, the resistance of ideal current source is very high, hence $A_{cm}$ decreases and the CMRR of the amplifier is increased.

**24. (c)**




$$g_{m1} = \frac{I_1}{V_i}$$

$$I_0 = \alpha I_1 \cong I_1$$

$$g_m = \frac{I_0}{V_i} \cong \frac{I_1}{V_i} = g_{m1}$$

**25. (b)**

Given that, $A_{OL} = 400$

$A_{CL} = 200$

We know that, $A_{CL} = \dfrac{A_{OL}}{1+\beta A_{OL}} = 200$

$$\Rightarrow \quad \frac{400}{1+\beta\times 400} = 200$$

$$1 + 400\beta = 2$$

$$\beta = \frac{1}{400} = 0.0025$$

**26. (c)**

- Staggered tuning is a technique used in the design of multi-stage tuned amplifiers whereby each stage is tuned to a slightly different frequency. In comparison to synchronous tuning (where each stage is tuned identically), it produces a wider bandwidth at the expense of reduced gain.
- To prevent instability, neutralizing capacitor is connected externally in tuned amplifier.

**27. (d)**

Given data, $V_1 = 80\ \mu V;\ V_2 = -40\ \mu V$

$$\text{CMRR} = 50$$

$$A_{dM} = 40 \times 10^3$$

$$\text{CMMR} = 50 = \frac{A_{dM}}{A_{cM}}$$

$$A_{cM} = \frac{40000}{50} = 800$$

$$V_{dM} = V_1 - V_2 = [80 - (-40)] \times 10^{-6}$$
$$= 120 \times 10^{-6}\ V$$

$$V_{cM} = \frac{V_1 + V_2}{2} = \frac{80 - 40}{2} = 20\ \mu V$$

$$V_0 = VA_{dM} + A_{cM}\, V_{cM}$$
$$= 120 \times 10^{-6} \times 4 \times 10^4 + 800 \times 20 \times 10^{-6}$$
$$= 480 \times 10^{-2} + 1.6 \times 10^{-2} = 481.6 \times 10^{-2}$$
$$= 4.816\ V$$

**28. (c)**

For non-interacting stages, $f_H' = f_H\sqrt{\left(2^{1/n} - 1\right)}$

$$= 30\times 10^3\sqrt{2^{1/3} - 1}$$
$$= 30 \times 10^3 \times 0.5098 = 15.2947 \times 10^3$$
$$= 15.2947\ \text{kHz}$$

$$f_L' = \frac{f_L}{\sqrt{2^{1/n} - 1}} = \frac{25}{\sqrt{2^{1/3} - 1}}$$
$$= 25 \times 1.9614 = 49.036\ \text{Hz}$$

**29. (b)**

The low frequency response is affected by the bypass and coupling capacitor with the lower cut-off frequency inversely proportional to the capacitance. Hence, the lower frequency response of an RC coupled amplifier can be improved by increasing both the bypass and coupling capacitor.

**30. (a)**

$$V_0 \text{ (offset due to } V_{I0}) = V_{I0}\left(\frac{R_1 + R_f}{R_1}\right)$$
$$= 5\text{ mV}\left(\frac{10\text{ k}\Omega + 400\text{ k}\Omega}{10\text{ k}\Omega}\right)$$
$$= \frac{410}{10} \times 5\text{ mV} = 205\text{ mV}$$
$$V_0 \text{ (offset due to } I_{I0}) = I_{I0} R_f$$
$$= (160\text{ nA})\ (400\text{ k}\Omega)$$
$$= 64\text{ mV}$$
$$V_0 \text{ (total offset)} = V_0(\text{offset due to } V_{I0}) + V_0 \text{ (offset due to } I_{I0})$$
$$= (205 + 64)\text{ mV}$$
$$= 269\text{ mV}$$

**31. (c)**

| Feedback topology | Input impedance | Output impedance |
|---|---|---|
| Voltage series | increases | decreases |
| Voltage shunt | decreases | decreases |
| Current series | increases | increases |
| Current shunt | decreases | increases |

**32. (a)**

A 25-V peak signal across a 16-Ω load provides a peak load current of

$$I_L(P) = \frac{V_L(P)}{R_L} = \frac{25}{16} = 1.5625\text{ A}$$

The dc value of the current drawn from the power supply is then

$$I_{dc} = \frac{2}{\pi}(I_L(P)) = \frac{2}{\pi} \times 1.5625$$
$$= 0.9947\text{ A}$$

The input power delivered by the supply voltage is

$$P_i(\text{dc}) = V_{CC} I_{dc} = 40 \times 0.9947$$
$$= 39.788\text{ W}$$

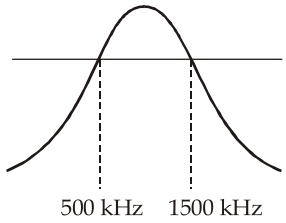
The output power delivered to the load is

$$P_0(\text{ac}) = \frac{V_L^2(P)}{2R_L} = \frac{25 \times 25}{2 \times 16} = 19.53125\text{ W}$$

Efficiency of amplifier,

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100 = \frac{19.53125}{39.788} \times 100$$
$$= 49.0883\%$$
$$\cong 49.09\%$$

**33. (d)**




$$f_H = \frac{1}{2\pi\sqrt{LC_L}} = \frac{1}{2\pi\sqrt{120\times10^{-6}\times C_L}} = 1500\times10^3$$

$$C_L = \frac{1}{(1500\times10^3\times2\pi)^2\times120\times10^{-6}}$$

$$= \frac{1}{4\pi^2\times225\times10^{10}\times120\times10^{-6}}$$

$$= \frac{10^{-5}}{4\times12\times225\pi^2} = 93.85\text{ pF}$$

$$f_L = \frac{1}{2\pi\sqrt{LC_H}} = 500\times10^3$$

$$C_H = \frac{1}{(2\pi\times500\times10^3)^2\times120\times10^{-6}}$$

$$= \frac{1}{4\pi^2\times25\times10^{10}\times120\times10^{-6}}$$

$$= \frac{10^{-5}}{4\pi^2\times25\times12} = \frac{10^7}{4\pi^2\times25\times12}\text{ pF}$$

$$= 844.34\text{ pF}$$

**34. (a)**

$$R_0 = \left(\frac{1}{g_m}\right) \| R_L \| r_{ds}$$

$$= \left(\frac{3}{5}\right) \| 2k \| 150k$$

$$= 460\ \Omega$$

**35. (b)**

For $V_i > V_r + V_{z1} = 8.7$ V, Zener diode $Z_1$ will be forward-bias and $Z_2$ will be in break-down region.

Hence, $V_0 = V_r + V_{z2} = 8.7$ V, for $V_i > 8.7$ V

For, $V_i < -V_r - V_{z2} = -8.7$ V; i.e., for $V_i < -8.7$ V $Z_2$ will be forward bias and $Z_1$ will be in break down region.

Hence, $V_0 = -V_r - V_{z1} = -8.7$ V; for $V_i < -8.7$ V

For $-8.7\text{ V} \le V_i \le 8.7$ V, the reverse-biased zener diode is not in break-down region and hence, doesn't conduct current.

$$V_0 = V_i \text{ for } -8.7 \le V_i \le 8.7 \text{ V}$$

i.e., $$V_0 = V_i \text{ for } |V_i| \le 8.7 \text{ V}$$

**36. (c)**

In lattice scattering, the frequency of events increases as the temperature increases, since the thermal agitation of the lattice becomes greater.

**37. (c)**

In a BJT as the emitter doping becomes very high, $E_g$ reduces significantly and also, $n_i$ increases significantly. Therefore, we have to consider the bandgap narrowing effect.

**38. (b)**

- When negative feedback is applied to ideal op-amp, the differential i/p voltage is zero due to virtual short.
- There is no current flow into either input terminals of ideal opamp as $Z_i = \infty$.

## Section B : Control Systems-1 + Microprocessors and Microcontroller-1

**39. (a)**

$$GH(s) = \frac{3K}{2s+1}$$

The closed loop transfer function,

$$H(s) = \frac{3K}{2s+1+3K} = \frac{3K/(1+3K)}{1+\frac{2}{1+3K}s}$$

Comparing with first-order transfer function,

$$H(s) = \frac{1}{1+\tau s}$$

We get, $$\text{Time constant} = \frac{2}{3K+1}$$

given $\tau < 0.2$

$$\frac{2}{3K+1} < \frac{1}{5}$$

$$10 < 3K + 1$$

$$9 < 3K$$

$$K > 3$$

**40. (a)**

For non-oscillatory response, the poles of the closed-loop system should be real and on left half side of s-plane. Hence, from the given root locus plot, the response to step input is non-oscillatory for $0 < K < 0.4$.

**41. (b)**

$$G(s) = \frac{1}{s^2+2s+1}$$

$$G(s) = \frac{1}{(s+1)^2},\ R(s) = \frac{1}{s}$$

Hence, $$C(s) = G(s)R(s) = \frac{1}{s(s+1)^2}$$

Using partial fraction expansion, we get

$$C(s) = \frac{A}{s} + \frac{B}{s+1} + \frac{C}{(s+1)^2}$$

$$1 = A(s^2 + 2s + 1) + B(s^2 + s) + Cs$$

$$A + B = 0,\quad 2A + B + C = 0,\ A = 1$$

From above, we get $B = -A = -1$. Also,

$$2A + B + C = 0$$

$$2 + (-1) + C = 0$$

$$C = -1$$

$$C(s) = \frac{1}{s} + \frac{-1}{(s+1)} + \frac{-1}{(s+1)^2}$$

$$c(t) = [1 - e^{-t} - te^{-t}]u(t)$$

The output value at steady state is equal to

$$\lim_{t\to\infty} c(t) = 1$$

At $t = 4.6$s,

$c(t = 4.6) = 0.94$ i.e. 94% of the steady-state value.

For a causal system, the output or response at any time instant depends only on the present and past values of the input but not on the future values.

**42. (a)**

The gain of the forward paths,

$G_2G_4G_6$, $G_3G_5G_7$, $G_2G_1G_7$, $G_3G_8G_6$, $G_2G_1(-H_2)G_8G_6$, $G_3G_8(-H_1)G_1G_7$ [Six forward paths]

Individual loops: $-G_4H_1$, $-G_5H_2$, $G_1(-H_2)\ G_8(-H_1)$ [Three individual loops]

**43. (c)**

$$y(t) = 1 - \frac{2}{\sqrt{3}} e^{-t} \cos\left(\sqrt{3}t - \frac{\pi}{6}\right)$$

On comparing the above expression with

$$y(t) = 1 - \frac{e^{-\xi\omega_n t}}{\sqrt{1-\xi^2}} \sin(\omega_d t - \theta)$$

$$\xi\omega_n = 1 \quad \ldots(1)$$

$$\omega_d = \sqrt{3}\ \text{rad/sec}$$

$$\omega_d = \omega_n\sqrt{1-\xi^2}$$

$$\sqrt{3} = \omega_n\sqrt{1-\xi^2} \quad \ldots(2)$$

from (1) and (2), we get $\omega_n = 2$ rad/sec

$$\xi = \frac{1}{2} = 0.5$$

$\therefore$ Transfer function $T(s) = \dfrac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} = \dfrac{4}{s^2 + 2s + 4}$

The overshoot does not occur in overdamped systems ($\xi > 1$), hence statement 2 is also correct.

**44. (b)**

$$q(s) = s^6 + 3s^5 + 4s^4 + 6s^3 + 5s^2 + 3s + 2$$

| | | | | |
|---|---|---|---|---|
| $s^6$ | 1 | 4 | 5 | 2 |
| $s^5$ | 1 | 2 | 1 | 0 |
| $s^4$ | 2 | 4 | 2 | 0 |
| $s^3$ | 1 | 1 | 0 | 0 |
| $s^2$ | 1 | 1 | 0 | 0 |
| $s^1$ | 2 | 0 | 0 | 0 |
| $s^0$ | 1 | | | |

Hence, the system is unstable.

$$A_1(s) = 2s^4 + 4s^2 + 2 = 2(s^2 + 1)^2$$

$$\frac{dA_1(s)}{ds} = 8s^3 + 8s$$

$$A_2(s) = s^2 + 1$$

$$\frac{dA_2(s)}{ds} = 2s$$

The roots from the Auxiliary equation are given by $s = j, j, -j, -j$. Hence, out of 6, atleast four roots are imaginary and also, more than one root lies in the right half of $s = -1$.

**45. (d)**

The gain margin is the inverse of the intersection of the root loci plot to the imaginary axis and if it does not intersect, then the gain margin will be infinite.

**46. (c)**

$$G(s) = \frac{K}{s(s+2)}$$

$$\text{T.F} = \frac{Y(s)}{X(s)} = \frac{G}{1+GH} = \frac{K}{s^2 + 2s + K}$$

$$X(s) = \frac{1}{s}$$

$$Y(s) = \frac{K}{s(s^2 + 2s + K)} = \frac{A}{s} + \frac{Bs + C}{s^2 + 2s + K}$$

$$= \frac{(A+B)s^2 + (2A + C)s + AK}{s(s^2 + 2s + K)}$$

$A = 1, B = -1, C = -2$

$$Y(s) = \frac{1}{s} - \frac{s+2}{s^2+2s+K} = \frac{1}{s} - \frac{(s+1)+1}{(s+1)^2+(K-1)}$$

$$= \frac{1}{s} - \frac{(s+1)}{(s+1)^2+(\sqrt{K-1})^2} - \frac{1}{(\sqrt{K-1})}\frac{(\sqrt{K-1})}{(s+1)^2+(\sqrt{K-1})^2}$$

$$y(t) = u(t) - e^{-t}\cos(\sqrt{K-1})t - \frac{1}{(\sqrt{K-1})}e^{-t}\sin(\sqrt{K-1})t$$

$$\text{output frequency} = \sqrt{K-1}$$

$$\therefore \quad \frac{\omega(\text{for } K=33)}{\omega(\text{for } K=17)} = \sqrt{\frac{32}{16}} = \sqrt{2} = 1.41$$

**47. (c)**

MVI B, 82 H ⇒ B ← 82 H
MOV A, B ⇒ A ← B
MOV C, A ⇒ C ← A
CMP B ⇒ Flags are affected on the basis of operation [A] – [B]
After executing the instruction OUT PORT 1, the output at PORT 1 is the contents of accumulator i.e. 82 H.

**48. (d)**

MVI A, 8F H ⇒ A ← 8F H
SUI 67 H ⇒ A ← 8F – 67 = 28 H [CY = 0]
OUT PORT 1 ← 28 H
Hence, output at PORT 1 is 28 H

**49. (a)**

**50. (a)**

READY signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high and hence, can be used to insert wait states.

**51. (b)**

- 8085 provides 8 user-defined software interrupts RST 0 to RST 7.
- All other options are hardware interrupt. 8085 has five hardware interrupts: INTR, RST 7.5, RST 6.5, RST 5.5 and TRAP.

**52. (c)**

READY is input signal to microprocessor used to synchronize slow peripherals with the microprocessor.

**53. (d)**

**54. (a)**

Instruction cycle is the time required to complete one instruction. First, the opcode is fetched from a stored memory location which is then decoded by the microprocessor to find out which operation

it needs to perform. If an instruction contains data, it is read from the effective address and thereafter, the execution is performed.

**55. (b)**

MVI A, AA H → A = 1010 1010
ORI FFH → A = 1111 1111
RRC → A = 1111 1111 ⇒ CY = 1
RRC → A = 1111 1111 ⇒ CY = 1
CMC → CY = 0
INR A → A = 0000 0000 ⇒ AC = 1, S = 1, P = 1

A = 00 00 00 00 = 00 H

Flag Register → F = 01 01 01 00 = 54 H

**56. (a)**

Complex poles and zeros exists in pair. They don't have any effect on root locus on real axis as the angle contribution on real axis by the pair is $2\pi$ radian angle which means 0° angle. Hence, it cannot change the phase of the system.

## Section C : Network Theory-2 + Digital Circuits-2

**57. (b)**

$$Z(s) = \frac{1}{s} + \frac{s\left(\frac{1}{s}+s\right)}{s+\frac{1}{s}+s} = \frac{1}{s} + \frac{(1+s^2)s}{(2s^2+1)} = \frac{2s^2+1+s^2(1+s^2)}{2s^3+s}$$

$$Z(s) = \frac{s^4+3s^2+1}{2s^3+s}$$

**58. (a)**

For transmission parameter matrix,

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2$$
$$\text{Parameter, } D = \frac{-Y_{11}}{Y_{21}}$$

**59. (c)**

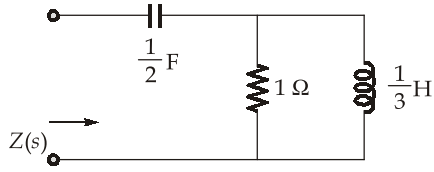
Given, $Z(s) = \frac{s^2+2s+6}{s(s+3)}$

Let $Z_1$ be the unknown element,

from the given network, $Z(s) = Z_1 + \frac{s}{s+3}$

By partial fraction expansion,

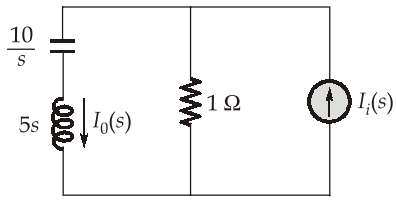
$$Z(s) = \frac{2}{s} + \frac{s}{s+3}$$




∴ The element is capacitor, $C = \frac{1}{2}\text{F}$.

**60. (c)**

Convert the given circuit in s-domain,




Apply current division rule;

$$I_0(s) = I_i(s) \times \frac{1}{1 + \frac{10}{s} + 5s}$$

$$\frac{I_0(s)}{I_i(s)} = \frac{s}{5s^2 + 10 + s}, \text{ where } s = j\omega$$

**61. (b)**

As we know that, $[Z] = \begin{bmatrix} \frac{A}{C} & \frac{\Delta T}{C} \\ \frac{1}{C} & \frac{D}{C} \end{bmatrix}$

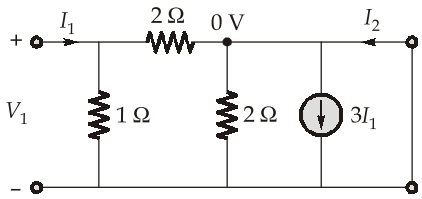
∴ $Z_{22} = \frac{D}{C} = \frac{4C/3}{C} = \frac{4}{3}\Omega$

**62. (c)**

The short circuit admittance parameter

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2 = 0}$$

We have, $Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2 = 0} = \frac{1}{1 \| 2} = \frac{3}{2} = 1.5\,\text{℧}$



$$-I_2 + 3I_1 + \frac{0 - V_1}{2} = 0$$

but $I_1 = 1.5\ V_1$

$$-I_2 + 3(1.5)V_1 - \frac{V_1}{2} = 0$$

$$I_2 - 4.5V_1 + 0.5V_1 = 0$$

$$I_2 = 4V_1$$

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2 = 0} = 4\ \mho$$

**63. (a)**

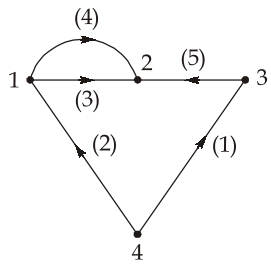
Given reduced incidence matrix is,

$$A = \begin{bmatrix} 0 & -1 & 1 & 1 & 0 \\ 0 & 0 & -1 & -1 & -1 \\ -1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

By writing the complete incidence matrix from the matrix $A$ such that the sum of all entries in each column of $A_a$ will be zero, we get

$$A_a = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \end{array} \begin{array}{c} \begin{array}{ccccc} 1 & 2 & 3 & 4 & 5 \end{array} \\ \begin{bmatrix} 0 & -1 & 1 & 1 & 0 \\ 0 & 0 & -1 & -1 & -1 \\ -1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 \end{bmatrix} \end{array}$$

The oriented graph can be drawn as




**64. (c)**

There exists orthogonal relationship between reduced incidence matrix, tie-set matrix and cut-set matrix, hence

$$BA^T = AB^T = 0$$

**65. (d)**

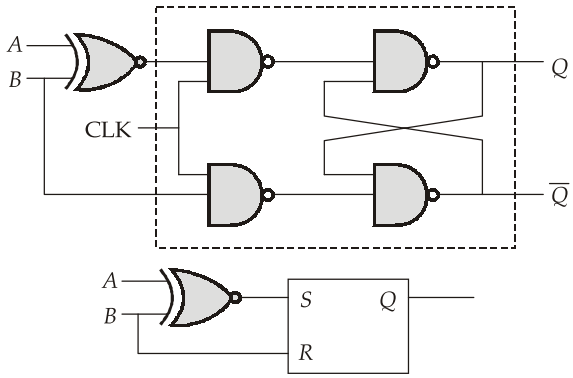
A cut-set should contain only one tree branch.

**66. (a)**

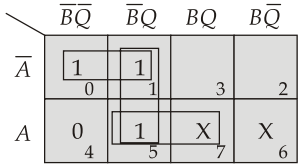
In the ripple counter, the first flip flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flops. Hence, statement (2) is incorrect.

Design and implementation of ripple counter is very simple as it requires less number of logic gates. Decoding errors in the ripple counter are due to propagation delay of flip-flops. Hence statement (4) is incorrect.

**67. (a)**




| $A$ | $B$ | $Q$ | $S$ | $R$ | $Q^+$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | X |
| 1 | 1 | 1 | 1 | 1 | X |




$$Q^+ = \overline{A}\overline{B} + \overline{B}Q$$

$$Q^+ = \overline{B}(\overline{A} + Q)$$

Also, we can write $$Q^+ = \overline{A}\overline{B} + AQ$$

**68. (b)**

Worst case delay in ripple counter

$$T_{d\max 1} = t_{pdff}(1) + t_{pdff}(2) + t_{pdff}(3)$$
$$T_{d\max 1} = 10 + 20 + 30 = 60 \text{ ns}$$

Worst case delay in synchronous counter,

$$T_{d\max 2} = \max\{t_{pdff}(1),\ t_{pdff}(2),\ t_{pdff}(3)\}$$
$$= \max\{10, 20, 30\}$$
$$= 30 \text{ nsec}$$

Ripple counter suffer from decoding error due to propagation delay. But due to unequal propagation delay of flip-flops, synchronous counter also suffers from decoding errors.

$$f_{\max} = \frac{1}{T_{d\max 2}} = \frac{1}{30 \text{ ns}} = \frac{2}{60 \text{ ns}} = \frac{2}{T_{d\max 1}}$$

$$\Rightarrow \quad f_{\max 2} = 2f_{\max 1}$$

**69. (a)**

The given Mealy machine generates a output '1' whenever two consecutive zeros or three consecutive ones are detected with overlapping sequences allowed.

1 0 1 0 0 0 1 : 2 high state

1 0 0 1 1 0 1 : 1 high state

1 0 1 1 1 1 0 : 2 high state

1 0 1 0 1 0 1 : No high state

**70. (d)**

For logic family *A*,

$$NM_H = V_{OH(\min)} - V_{IH(\min)}$$
$$= 4.6 - 4.4 = 0.2 \text{ V}$$
$$NM_L = V_{IL(\max)} - V_{OL(\max)}$$
$$= 0.6 - 0.1 = 0.5 \text{ V}$$

For logic family *B*,

$$NM_H = 2.4 - 2.0 = 0.4 \text{ V}$$
$$NM_L = 0.8 - 0.4 = 0.4 \text{ V}$$

Since, $[NM_H]_B > [NM_H]_A$, therefore when a high output is driving an input, more noise can be tolerated in logic family *B*.

Since, $[NM_L]_A > [NM_L]_B$, therefore when a low output is driving an input, more noise can be tolerated in logic family *A*.

Low state fanout:

$$n_A = \frac{I_{OL(\max)}}{I_{IL(\min)}} = \frac{8}{0.1} = 80$$

$$n_B = \frac{10}{2} = 5$$

The low state fanout is higher for logic family *A*.

High state fanout:

$$n_A = \frac{I_{OH(\max)}}{I_{IH(\min)}} = \frac{0.4}{0.02} = 20$$

$$n_B = \frac{20}{0.5} = 40$$

The high state fanout is higher for logic family *B*.

**71. (a)**

$$\text{The percentage resolution} = \frac{\text{Step size}}{\text{Full scale output}} \times 100$$

There are 99 steps, since there are two BCD digits. Thus, the full scale output is

$$V_{FS} = 99 \times 0.2 = 19.8 \text{ V}$$

$$\therefore \quad \text{The percentage resolution} = \frac{0.2}{19.8} \times 100 = 1\%$$

$\because$ [step size is the weight of the LSB of the lower significant digit (LSD) = 0.2 V]

**72. (c)**

$$\text{Step size} = 0.5 \text{ V}$$

The step size corresponds to the output pertaining to the least significant bit (LSB). For the input,

$$DC\,BA = 0001$$

The output i.e. step-size is

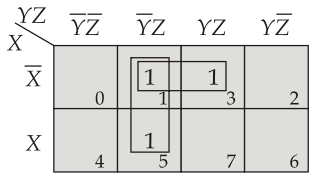
$$\frac{5}{8\,\text{k}\Omega} \times R_F = 0.5$$

$$R_F = 800\ \Omega$$

**73. (c)**

Transistor $Q_1$ will be ON when diodes $D_1$ and $D_2$ are OFF i.e. $X = 1$ and $Y = 1$. The truth table for the circuit can be written as below:

| $X$ | $Y$ | $Z$ | Transistor $Q_1$ | $F$ |
|---|---|---|---|---|
| 0 | 0 | 0 | OFF | 0 |
| 0 | 0 | 1 | OFF | 1 |
| 0 | 1 | 0 | OFF | 0 |
| 0 | 1 | 1 | OFF | 1 |
| 1 | 0 | 0 | OFF | 0 |
| 1 | 0 | 1 | OFF | 1 |
| 1 | 1 | 0 | ON | 0 |
| 1 | 1 | 1 | ON | 0 |




$$F = \overline{X}Z + \overline{Y}Z = Z(\overline{X} + \overline{Y})$$

$$F = \overline{XYZ}$$

**74. (b)**

**75. (b)**

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