DETAILED SOLUTIONS

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ESE 2024 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 4

Section A : Control Systems + Microprocessors and Microcontroller

Section B : Network Theory-1

Section C : Digital Circuits-1

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DETAILED EXPLANATIONS
Section A : Control Systems + Microprocessors and Microcontroller

1. (c)

Derivative controller improves the transient response and integral controller reduces the steady-state error, thereby improving the steady state response of the system.

2. (b)

The Routh array for the characteristic equation is

s^3	1	c
s^2	b	1
s^1	$c-\frac{1}{b}$	0
s^0	1	

For stability, $c > \frac{1}{b}$

$bc > 1$

3. (c)

$$\arg|G(s)H(s)|_{s=-2+j1} = \arg\left[\frac{K(s+3)}{(s+2+j1)}\right]_{s=-2+j1}$$

$$= \arg\left[\frac{K[-2+j1+3]}{[-2+j1+2+j1]}\right] = \arg\left[\frac{K(1+j1)}{(2j)}\right]$$

$$= \frac{\angle 45^\circ}{\angle 90^\circ} = \angle -45^\circ$$

$$\theta_d = 180^\circ + \arg|G(s)H(s)|$$

$$\theta_d = 180^\circ - 45^\circ = 135^\circ$$

4. (b)

The closed loop transfer function with the unity feedback proportional control system is given by

$$\frac{C(s)}{R(s)} = \frac{\frac{2K}{s(s+1)(s+2)}}{1+\frac{2K}{s(s+1)(s+2)}} = \frac{2K}{s(s+1)(s+2)+2K}$$

The characteristic equation

$$s(s+1)(s+2)+2K = 0$$

$$|K| = \left|\frac{s(s+1)(s+2)}{2}\right|$$

$$|K|_{s=j\sqrt{2}} = \left|\frac{\sqrt{2}\times\sqrt{3}\times\sqrt{6}}{2}\right| = 3$$

For $K > 3$, poles lie in the right-half of s-plane. Hence, the maximum possible controller gain, for the system to be stable, is $K = 3$.

5. (c)

From the given transfer function, we get in the frequency domain,

$$G(j\omega)H(j\omega) = \frac{10e^{-jL\omega}}{j\omega}$$

$$= \frac{10}{\omega}\angle(-L\omega - 90°)$$

At phase cross-over frequency ω_p;

$$-L\omega_p - 90° = -180°$$

$$L\omega_p = 90° = \frac{\pi}{2}$$

$$L = \frac{\pi}{2\omega_p} = \frac{\pi}{2\times 5} = \frac{\pi}{10}$$

6. (a)

The corner frequency associated with a pole causes a slope change by –20 dB/decade and the corner frequency associated with a zero causes a slope change by 20 dB/decade. Therefore, from the given bode magnitude plot, we can write

$$T(s) = \frac{K(s+40)}{(s+10)(s+20)}$$

Alsol we have $20\log_{10}K = 40$

$$K = 10^2 = 100$$

$$K = 100$$

$\therefore$ $$T(s) = \frac{100(s+40)}{s(s+10)(s+20)}$$

7. (a)

Since the open loop transfer function has a pole in the RHP, $P = 1$. Now, the Nyquist plot makes one CW encirclement of the critical point. Hence, $N = -1$. Therefore,

$$N = P - Z$$

$$-1 = 1 - Z$$

$$-1 - 1 = -Z$$

$$Z = 2$$

This means that there are two poles in the R.H.P of the closed loop transfer function and therefore, the system is unstable.

8. (b)

A lead compensator has transfer function $G(s) = \frac{K(1+Ts)}{1+\alpha Ts}; \alpha > 1$. The maximum phase shift ϕ_{max} is given by

$$\sin\phi_{max} = \frac{1-\alpha}{1+\alpha}$$

$$G(s) = \frac{5\left[\frac{s}{5}+1\right]}{15\left[\frac{s}{15}+1\right]} = \frac{1}{3}\frac{\left[\frac{s}{5}+1\right]}{\left[\frac{s}{15}+1\right]}$$

where, $\alpha = \frac{1}{3}$

$$\sin\phi_{max} = \frac{1-\frac{1}{3}}{1+\frac{1}{3}} = \frac{\frac{2}{3}}{\frac{4}{3}} = \frac{1}{2}$$

$\therefore \quad \phi_{max} = 30°$

9. (a)

The poles location can be calculated from the transfer function given by $G(s) = C\,[sI - A]^{-1}\,B$.

$$[sI - A] = \begin{bmatrix} s & 0 \\ 0 & s \end{bmatrix} - \begin{bmatrix} 0 & 1 \\ -2 & -3 \end{bmatrix}$$

$$= \begin{bmatrix} s & -1 \\ 2 & s+3 \end{bmatrix}$$

$$\Rightarrow \quad [sI - A]^{-1} = \frac{1}{s(s+3)+2}\begin{bmatrix} s+3 & +1 \\ -2 & s \end{bmatrix}$$

$$G(s) = \frac{1}{s^2+3s+2}\begin{bmatrix}1 & 0\end{bmatrix}\begin{bmatrix} s+3 & 1 \\ -2 & s \end{bmatrix}_{2\times2}\begin{bmatrix}0\\1\end{bmatrix}_{2\times1}$$

$$= \frac{1}{s^2+3s+2}\begin{bmatrix}1 & 0\end{bmatrix}_{1\times2}\begin{bmatrix}1\\s\end{bmatrix}_{2\times1}$$

$$= \frac{1}{s^2+3s+2}[1]_{1\times1}$$

$$= \frac{1}{s^2+3s+2} = \frac{1}{(s+1)(s+2)}$$

$\therefore$ Poles are located at $s = -1$, $s = -2$.

10. (a)

For the system to be controllable, $|A| \neq 0$. Hence, the rank of the matrix must be n.

11. (c)

$$f(0^+) = \lim_{t\to0} f(t) = \lim_{s\to\infty} sF(s)$$

$$= \lim_{s\to\infty} s\cdot\frac{4s+1}{s(s^2+2)} = \lim_{s\to\infty}\frac{4+\frac{1}{s}}{s+\frac{2}{s}} = 0$$

$$f(0^+) = 0$$

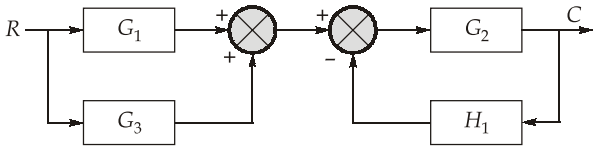
$$L[f'(t)] = sF(s) - f(0^+)$$

$$= s\cdot\frac{4s+1}{s(s^2+2)} - 0 = \frac{4s+1}{(s^2+2)}$$

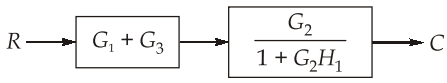
$$f'(0^+) = \lim_{s\to\infty} s\cdot\frac{4s+1}{s^2+2} = \lim_{s\to\infty}\frac{4+\frac{1}{s}}{1+\frac{2}{s^2}} = 4$$

12. (c)

The given block diagram can be redrawn as shown in figure.



The block diagram can further be simplified as below:



$$\frac{C}{R} = \frac{(G_1+G_3)G_2}{1+G_2H_1} = \frac{G_1G_2+G_2G_3}{1+G_2H_1}$$

13. (b)

$$G(s) = \frac{K}{s^2(s+5)}$$

s^2 term will provide a initial roll off by –40 dB/decade (–12 dB/octave). $(s + 5)$ term will further give a roll off by –20 dB/decade, thus from $\omega = 5$ rad/sec, roll-off rate is –60 dB/decade (–18 dB/octave).

14. (c)

For $$G(j\omega) = \frac{1}{\left[(j\omega)^2(1+j\omega\tau)\right]}$$

$\omega = 0^+$ $$G(j0^+) = \frac{1}{\left[(j0^+)^2(1+j0^+\tau)\right]} = \infty\angle -180°$$

$\omega = \infty^+$ $$G(j\infty^+) = \frac{1}{\left[(j\infty)^2(1+j\infty\tau)\right]} = 0\angle -270° = 0\angle 90°$$

15. (d)

- Adding a zero to the forward path transfer function tends to push root locus to the left.
- Adding a pole to the forward path transfer function tends to push root locus to the right.

16. (c)

For characteristic equation,

$$s^3 + 3s^2 + 2s + K = 0$$

$$\xi \propto \frac{1}{\sqrt{K}}, \text{ hence increase } K \text{ with reduce } \xi.$$

For characteristic equation,

$$s^2 + 2s + K(0.2s + 1) = 0$$
$$s^2 + 2s + 0.2sK + K = 0$$
$$s^2 + s(2 + 0.2K) + K = 0$$
$$\xi = \frac{2 + 0.2K}{2\sqrt{K}} = \frac{1}{\sqrt{K}} + 0.1\sqrt{K}$$

For higher valves of K, damping improves if

$$\frac{1}{\sqrt{K}} > 0.1\sqrt{K} \Rightarrow K > 10$$

For $K = 10$, $\xi = 0.63$. Hence, increasing K will improve damping for $\xi > 0.63$.

17. (c)

$$GH(s) = \left(\frac{3s + K_I}{s}\right) \times \frac{2}{(s^3 + 4s^2 + 5s + 2)}$$

$$K_V = \lim_{s \to 0} sGH(s) = \lim_{s \to 0} s \cdot \left[\frac{3s + K_I}{s}\right] \times \left[\frac{2}{s^3 + 4s^2 + 5s + 2}\right]$$

$$K_V = \frac{K_I \times 2}{2} = K_I$$

Given, for unit step input $e_{ss} < 2\%$, therefore

$$\frac{1}{K_I} < \frac{1}{50}$$
$$50 < K_I$$
$$\Rightarrow \quad K_I > 50$$

18. (c)

The characteristic equation of the system,

$$1 + GH(s) = 1 + \frac{1}{(s^2 + s + 1)}\left(\frac{sK_p + 2}{s}\right)$$
$$q(s) = s^3 + s^2 + s(1 + K_p) + 2$$

s^3	1	$(1 + K_p)$
s^2	1	2
s^1	$\frac{(1 + K_p) - 2}{1}$	
s^0	2	

For the system to be stable,

$$1 + K_p - 2 > 0$$
$$K_p - 1 > 0$$
$$K_p > 1$$

19. (a)

$$\frac{G}{1+G} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

$$M_p = e^{-\pi\xi/\sqrt{1-\xi^2}}$$

$$M_r = \frac{A}{2\xi\sqrt{1-\xi^2}}$$

Hence, both peak overshoot to step input and resonant peak of the frequency response is indicative of damping.

20. (d)

The program counter acts as a pointer to the next instruction to be executed and contains the address of the next instruction to be fetched from the main memory when the previous instruction has been successfully completed.

21. (d)

ADI 01 H

$$\begin{array}{rl} \text{FFH} = & 1111\ 1111 \\ + \quad = & \\ \text{01H} = & 0000\ 0001 \\ \hline & \boxed{1}\,0000\ 0000 \\ & \text{CY} \end{array}$$

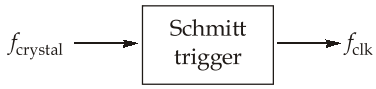
Flag states $S = 0, Z = 1, CY = 1, AC = 1, P = 1$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	X	1	X	1	X	1
S	Z		AC		P		CY

$\Rightarrow$ 01010101 = 55 H

22. (a)

8085 microprocessor uses a divide-by-two circuit to generate its internal clock. Hence, the frequency of the crystal/driving network connected between pin 1 and pin 2 must be twice the desired clock frequency.



23. (d)

After execution of INX H instruction, contents of register pair (HL) are incremented by "0001".

So, [HL] = [HL] + 0001

2	4	F	F
0010	0100	1111	1111
+ 0000	0000	0000	0001
0010	0101	0000	0000
2	5	0	0

∴ Content of HL pair after execution of INX H = 2500 H

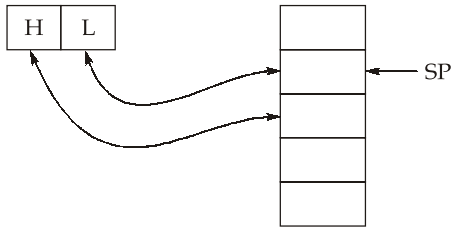
24. (d)

DAA instruction is used in a microprocessor to perform decimal adjust after addition i.e. it is used to correct the result of an arithmetic operation on two decimal numbers that are represented in binary coded decimal (BCD) format. DAA instruction changes the binary values of the contents of accumulator to BCD. This instruction makes use of status of *CY* and *AC* flags.

25. (c)

Let us check each option:

- **PUSH PSW:** It stores the contents of PSW on top of the stack thereby decrementing the contents of stack pointer by 2.
- **CALL addr:** The call instruction is a combination of PUSH + JMP. The current address of the program counter (PC) is pushed onto the stack, and the PC is loaded with the address of the subroutine. So, it also reduces the contents of stack pointer by 2.
- **XTHL:** Exchange the contents of top of stack and HL register pair. There is no effect on content of stack pointer.



- **RSTn:** When RSTn interrupt is received,the processor saves the contents of the PC register onto stack and branches to the specified vector address. So, it changes the contents of stack pointer.

26. (a)

RETURN instruction can be conditional or unconditional in the subroutine as it is used to mark the end of a subroutine and to transfer control back to the calling program.

27. (b)

TRAP is a vectored interrupt having the highest priority and it is both positive edge triggered and positive level triggered as shown below:

28. (d)

- Memory-mapped I/O uses the same address space to address both main memory and I/O devices. The memory and registers of the I/O devices have 16-bit addresses and any arithmetic or logical operations can be directly performed with I/O data as in case of memory eg. MOV, CMP M, etc.
- Since, it uses a 16-bit address, a maximum of 2^{16} = 65536 I/O devices can be connected.
- IN and OUT instruction are used in I/O mapped I/O.

29. (a)

LXI H, 01FF H $\rightarrow$ H $\rightarrow$ 01H
$\rightarrow$ L $\rightarrow$ FFH
SHLD 2050 H $\rightarrow$ 2050 H $\rightarrow$ FFH
2051 H $\rightarrow$ 01H

30. (d)

8259A PIC can manage 8 levels of interrupts. If more levels of interrupts are to be handled, the 8259A is used in cascade mode. In cascade mode, a master 8259A along with eight slaves 8259A can handle upto 64 interrupts.

31. (a)

- The PUSH operation will decrement the content of the SP by two and data is added on to the top of the stack. So, after a PUSH operation, the content of the SP will be less by two than the earlier value.
- The POP operation will increment the content of the SP by two and data is removed from the top of the stack. So, after a POP operation, the content of the SP will be greater by two than the earlier value.

32. (c)

- 8051 microcontroller has 8-bit data bus, hence it is a 8-bit microcontroller.
- There are five specified interrupts in 8051 - two external interrupts (INT0, INT1), two timer interrupts (TF0, TF1) and one serial interrupt (RI/TI).
- 8051 has a 8-bit flag register in which 6 bits are defined as given below and two unused bits are user defined flags:
  1. CY $\rightarrow$ Carry flag
  2. AC $\rightarrow$ Auxilliary carry flag
  3. P $\rightarrow$ parity flag
  4. OV $\rightarrow$ Overflow flag
  5. RS1
  6. RS0

  } Register Select Bits to select register bank

The SCON (Serial Control) register is used to program the start bit, stop bit, and data bits of framing in the serial communication.

33. (c)

LXI B, 0007 H ⇒ B ← 00 H
C ← 07 H
LOOP: DCX B ⇒ 0006 H
MOV A, B ⇒ A ← 00 H
ORA C ⇒ A ← 06 H

The LOOP will be executed 7 times till the value of BC register = 00.

34. (b)

P 3.5 T1 (Timer 1 external input)
P 3.4 T0 (Timer 0 external input)
P 3.2 $\overline{\text{INT0}}$ (External hardware interrupt 0)
P 3.3 $\overline{\text{INT1}}$ (External hardware interrupt 1)

35. (d)

- Non-maskable interrupt (NMI) has the highest priority in 8086 microprocessor.
- TRAP has highest priority in 8085 microprocessor.

36. (c)

- 8257 is a 4-channel programmable DMA controller, each channel incorporates two 16 bits registers i.e., DMA address register and byte count register. These registers are initialized before a channel is enabled.
- In 8259A programmable interrupt controller, all the 8-vector interrupts can be spaced or priorities at an interval of 4-bit or 8-bit locations but it can be 16-bit also if additional 8259 A are cascaded.
- 8285 is widely used programmable parallel I/O device. It can be programmed to transfer data under various conditions from I/O to interrupt I/O.

37. (a)

I and II are true and I is correct explanation as in DMA, data transfer takes place between μP memory and I/O devices at faster rate without intervention of CPU/μP.

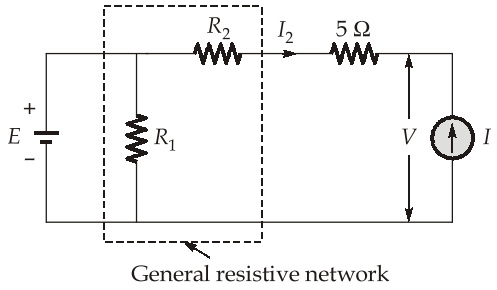
38. (b)

In an I/O mapped I/O device, data is transferred from the accumulator to I/O device and received from I/O device into the accumularor using IN and OUT instructions.

Section B : Network Theory-1

39. (c)

Consider the resistive network as shown below,



When I is removed, $I_2 = 0$.

$\therefore \quad V = E = E_1 = 10\ \text{V}$

$\therefore \quad E_1 = 10\ \text{V}$

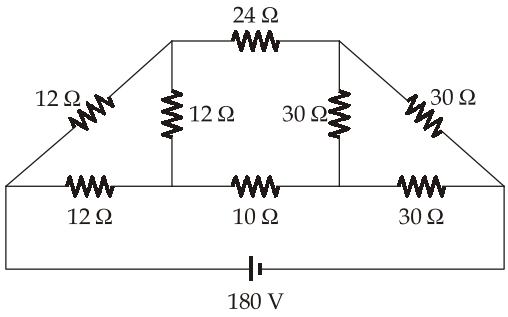
When $E = 0$ and $I = 2$ A, then

$$V = I(R_2 + 5)$$
$$12 = 2(R_2 + 5)$$
$$6 - 5 = R_2$$
$$R_2 = 1\ \Omega$$

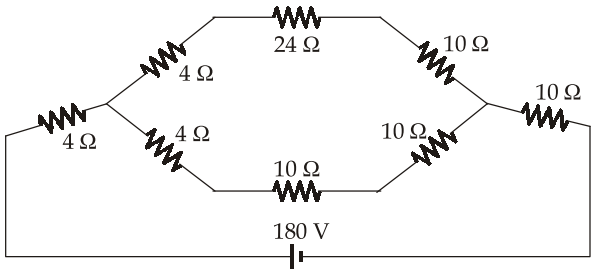
When I is replaced by 10 Ω , and $E = E_1$, we get

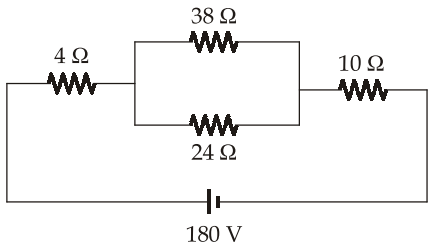
$$E_1 = (R_2 + 5 + 10)I_2$$
$$10 = (R_2 + 15)I_2$$
$$I_2 = \frac{10}{16} = \frac{5}{8}\ \text{A}$$
$$V = \frac{5}{8} \times 10 = \frac{25}{4} = 6.25\ \text{V}$$

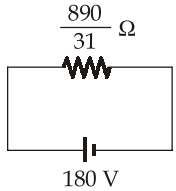
40. (c)



Using delta to star transformation, the circuit can be drawn as below:







$$I = \frac{180 \times 31}{890} = \frac{558}{89}\text{A}$$

$$I_{10\ \Omega} = \frac{558}{89} \times \frac{38}{38+24} = 3.84\ \text{A}$$

41. (a)

For an independent current source, the current through the branches will remain same if all the resistors are equally increased. From Ohm's Law, $V = IR$, hence the value of node voltage become double when value of all resistors are doubled.

42. (b)

$$V(t) = 177 \sin(314t + 10°)\ \text{V}$$
$$i(t) = 14.14 \sin(314t - 20°)\ \text{A}$$

Current $i(t)$ lags behind voltage $V(t)$ by 30°

$$\phi = 30°$$

$$\text{Power factor} = \cos 30° = \frac{\sqrt{3}}{2} \equiv 0.866$$

$$P_{avg} = V_{rms}\, I_{rms} \cos\theta$$
$$= \frac{177}{\sqrt{2}} \times \frac{14.14}{\sqrt{2}} \times 0.866$$
$$= \frac{177 \times 14.14}{2} \times 0.866$$
$$= 1083.70374\ \text{watt}$$

43. (b)

44. (c)

Fewer nodes will give lesser nodal equations than mesh equations, hence better analyzed by nodal analysis.

45. (d)

$$\text{Dynamic resistance} = \frac{L}{RC}$$
$$= \frac{0.2}{100 \times 10^{-6} \times 20} = 100\ \Omega$$

46. (a)

At half power of that at resonance,

$$P = \frac{I^2 R}{2} = \left(\frac{I}{\sqrt{2}}\right)^2 R, \text{ where } I = \frac{V}{R}$$

Hence, the magnitude of current will be reduced by $\sqrt{2}$ times at half power with

$$I = \frac{V}{\sqrt{2}R}$$

47. (b)

Given, $Z = (1 - j)\Omega$

$$Z = \sqrt{2}\angle -45^\circ\ \Omega$$

Given the network has leading power factor, hence

1. R and C circuit
3. R, L and C circuit are possible.

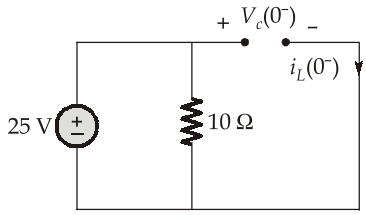
48. (b)

$$I = \sqrt{I_R^2 + I_L^2} = \sqrt{12^2 + 16^2} = \sqrt{144 + 256}$$

$$= \sqrt{400} = 20\ \text{A}$$

49. (d)

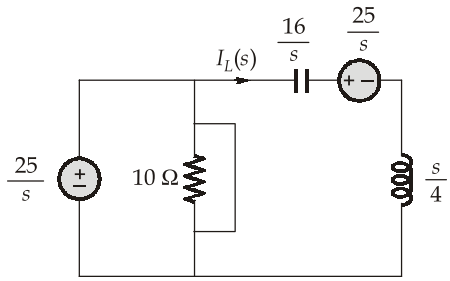
For $t < 0$



$V_c(0^-) = 25\ \text{V} = V_c(0^+)$

$i_L(0^-) = i_L(0^+) = 0\ \text{A}$

For $t > 0$



$$-\frac{25}{s} = I_L(s)\left[\frac{16}{s} + \frac{s}{4}\right]$$

$$I_L(s) = \frac{-25 \times 4s}{s(s^2 + 64)} = \frac{-100}{s^2 + 64} \Rightarrow i_L(t) = \frac{-100}{8}\sin 8t$$

$\therefore$ $$i_L(t) = \frac{-25}{2}\sin 8t\ \text{A}$$

50. (b)

$$i(t) = 10e^{-t}\ \mu A$$

Initial energy stored in 4 μF capacitor

$$E_1 = \frac{1}{2}(4)\times 2^2 = 8\ \mu J$$

Initial energy stored in 8 μF capacitor

$$E_2 = \frac{1}{2}\times 8\times 25 = 100\ \mu J$$

So, net initial energy, $E = E_1 + E_2 = 108\ \mu J$

Net capacitance $\Rightarrow$ $C_{eq} = \frac{4\times 8}{12} = \frac{8}{3}\ \mu F$

$V = 2 + 5 = 7\ V$

Energy delivered to black box,

$$E_B = \frac{1}{2}\times C_{eq}\times V^2$$

$$E_B = \frac{1}{2}\times\frac{8}{3}\times 49$$

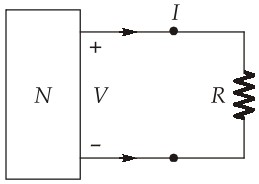
$$= 65.33\ \mu J$$

Energy trapped in capacitor;

$$E_C = E - E_B = 108 - 65.33$$

$$= 42.67\ \mu J$$

51. (d)



Let current be I.

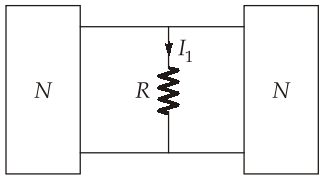
Then $P = I^2R$

Maximum value of current through R is

$I_1 \text{max} = 2I$

i.e., $I_1 < 2I$

but $I_1 > I$

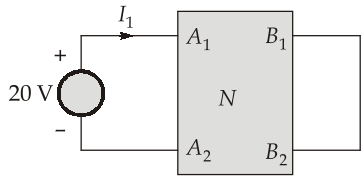


Since, $P_1 = I_1^2R$ i.e, $P_1 < 4I^2R$, i.e., $P_1 < 4P$

and $P_1 > I^2R$ i.e., $P_1 > P$

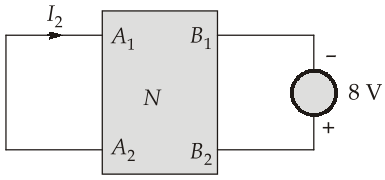
So, $P \le P_1 \le 4P$

52. (c)



Current I_1 due to 20 V source only,

$$I_1 = \frac{4}{12} \times 20 = \frac{20}{3} \text{A}$$



Using reciprocity theorem, current I_2 due to 8 V source is

$$I_2 = \frac{3}{12} \times 8 = 2 \text{ A}$$

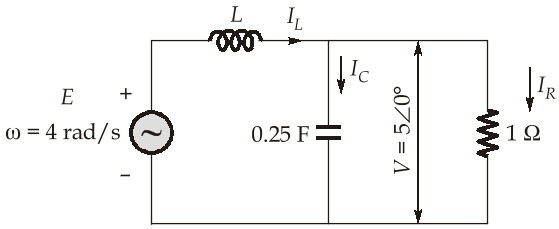
$$\text{Total current, } I = I_1 + I_2 = \frac{20}{3} + 2 = \frac{26}{3} \text{A}$$

53. (b)

- Thevenin Theorem is preferred in a circuit involving voltage source and series connection whereas Norton's theorem is preferred in the circuits involving current source and parallel connections.
- All network theorems are derivable from Kirchhoff's laws.
- Norton current is found after short-circuiting the terminals across which the Norton equivalent is asked.

Hence, statements 2 and 3 are incorrect.

54. (c)



Let current through inductor be $I_L \angle \theta$

$$\therefore \quad I_C = \frac{R}{R + \frac{1}{j\omega C}} \cdot I_L \angle \theta \qquad \text{...(i)}$$

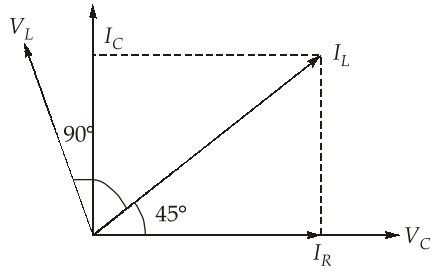
$$I_C = \frac{5\angle 0°}{\frac{1}{j\omega C}} \qquad \text{...(ii)}$$

From equation (i) and (ii)

$$I_L\angle\theta \cdot \frac{1}{1+\frac{1}{j\omega CR}} = 5\angle 0°\ (j\omega C)$$

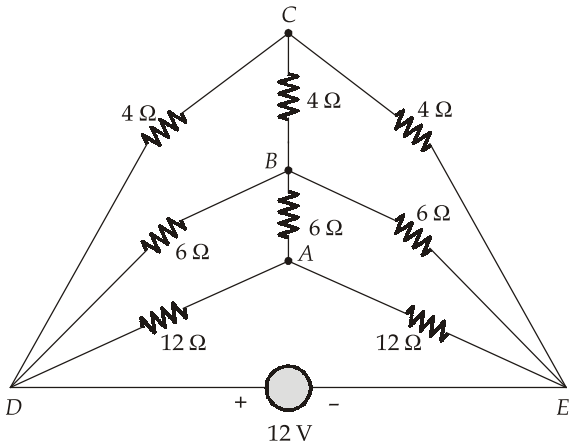
$$\theta - \tan^{-1}\omega CR + 90° = 0° + 90°$$

$$\theta = \tan^{-1}\omega CR = \tan^{-1}(4 \times 0.25 \times 1) = 45°$$



As we know inductor current lags the voltage by 90°. So inductor voltage phase angle = 90° + 45° = 135°. i.e., inductor voltage lead the capacitor voltage by 135°.

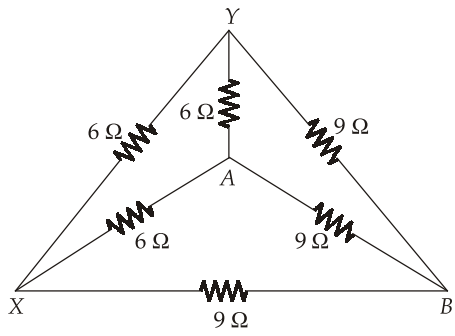
55. (a)



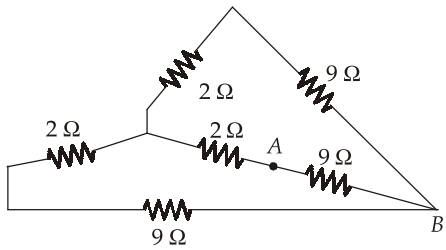
Circuit is symmetrical, so voltage at nodes V_A, V_B and V_C are equal and no current flows between these nodes.

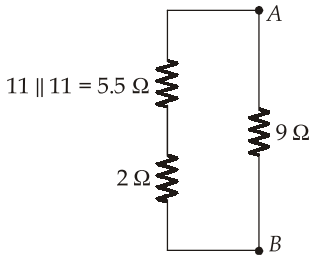
$$I = \frac{12}{24}+\frac{12}{12}+\frac{12}{8} = \frac{1}{2}+1+\frac{3}{2} = \frac{4}{2}+1 = 3\text{A}$$

56. (d)



Apply delta to star transformation in *A*-*X*-*Y*.





$R_{AB} = 7.5 \parallel 9 = 4.09\ \Omega$

57. (c)

- The value of the current remains the same in a series connection. Hence, the series connection of two current sources having different values is an invalid condition. Therefore, Statement (I) is true.
- Superposition theorem can be applied to current sources if a terminal of the source is connected to a common node. Therefore, Statement (II) is false.

Section C : Digital Circuits-1

58. (d)

$$(2A0F)_{16} = 2 \times 16^3 + 10 \times 16^2 + 0 \times 16^1 + 15 \times 16^0$$
$$= (10767)_{10}$$

59. (b)

Grouping bits in pairs of 3 for binary to octal conversion,
$001\ 100\ 101 \cdot 101\ 100 = (145.54)_8$

60. (a)

$$f(A, B, C) = \left[A \oplus (\bar{B}AB + B(\bar{A} + \bar{B})\right]\left[A \oplus (\bar{C}AC + C(\bar{A} + \bar{C})\right]$$
$$= \left[A \oplus (\bar{A}B)\right]\left[A \oplus (\bar{A}C)\right]$$
$$= \left[\bar{A}\bar{A}B + A(A + \bar{B})\right]\left[\bar{A}\bar{A}C + A(A + \bar{C})\right]$$
$$= (\bar{A}B + A + A\bar{B})(\bar{A}C + A + A\bar{C})$$
$$= (A + B)\ (A + C) = A + AC + AB + BC$$
$$= A + BC$$

Hence, it requires one-AND gate and one OR gate to implement the Boolean function $A + BC$.

61. (a)

$$F = \overline{\overline{(\bar{A}+B)} + \overline{(A+\bar{B})}} + (\overline{\bar{A}B})(\overline{A\bar{B}})$$

$$F = A \odot B \qquad \left[\begin{array}{l} \because F = \overline{\overline{\bar{A}+B} + \overline{(A+\bar{B})}} + (\overline{\bar{A}B})(\overline{A\bar{B}}) \\ F = \overline{(A\bar{B}+\bar{A}B)} + (A+\bar{B})(\bar{A}+B) \\ F = A \odot B + A \odot B \\ F = A \odot B \end{array}\right]$$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

For EX-NOR gate

Hence, $F = 0$ for $A \neq B$

62. (d)

$$f = \bar{C}_2\bar{C}_1 \cdot 1 + \bar{C}_2 \cdot C_1(\bar{A}+\bar{B}) + C_2 \cdot \bar{C}_1 \cdot S + C_2C_1 \cdot 0$$

$$f = \bar{C}_2\bar{C}_1 + \bar{C}_2C_1(\overline{AB}) + C_2 \cdot \bar{C}_1 \cdot S$$

63. (c)

Given, $A_1 = x$, $A_0 = y$

For decoder 1:

A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	0	0	0	1

Since, D_2 and D_3 cannot be at logic '1' at the same time, the output of AND gate is always zero i.e. $A_1 = 0$ for 2nd decoder.

We have,

$$f = D_0 + D_1$$

$$f = \bar{A}_0\bar{A}_1 + \bar{A}_0A_1 = \bar{z}.1 + z.0 = \bar{z}$$

64. (c)

$$2\text{ K} = 2 \times 1024 = 2048$$

Each word is having 8-bit (1 byte)

The total number of bits, that can be stored is $2 \times 1024 \times 8 = 16384$ bits.

65. (a)

PROM generates all the minterms using AND array which are then selected by the OR array to implement the desired function in SOP form.

66. (a)

$$\begin{aligned} P(x, y, z) &= \bar{y}\,\bar{z}\,x + \bar{y}\,z \cdot \bar{x} + y\bar{z} \cdot \bar{x} + yz \cdot x \\ &= \Sigma m\ (1, 2, 4, 7) \text{ sum of full adder} \\ Q(x, y, z) &= \bar{y}\,\bar{z}\,0 + \bar{y}\,z \cdot x + y\bar{z} \cdot x + yz \cdot 1 \\ &= \bar{y}\,z\,x + y\,\bar{z}\,x + yz \\ &= z\left[\bar{y}\,x + y\right] + y\bar{z}\,x \\ &= z\left[(\bar{y} + y)(x + y)\right] + y\bar{z}\,x \\ &= z\left[(x + y)\right] + y\bar{z}\,x \\ &= xz + zy + y\bar{z}\,x \\ &= x\left[z + y\bar{z}\right] + zy \\ Q &= x(z + y) + zy = xz + xy + yz \text{ [Carry of full adder]} \end{aligned}$$

67. (c)

$4 \times 16^3 + 9 \times 16^2 + 7 \times 16^1 + 5 \times 16^0 = (4975)_{16}$

Represent each Hex digit in 4-bit binary format

$$(4975)_{16} \leftrightarrow 0100\ 1001\ 0111\ 0101$$

68. (a)

$$(12C9)_{16} = \left(0|001\ \ |001|0\ \ 11|00\ \ 1|001\right)_2$$

$$(11X\ 1Y)_8 = (1131\ 1)_8$$

On comparing, $X = 3$ and $Y = 1$

69. (b)

	I_0	I_1	I_2	I_3
$\bar{A}$	⓪	①	2	3
A	4	⑤	⑥	⑦
	$\bar{A}$	1	A	A

70. (c)

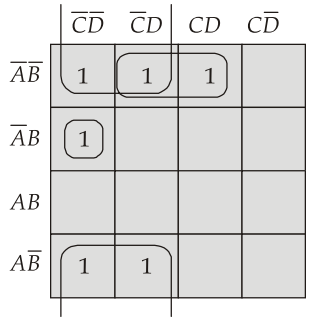
$$\begin{aligned} n &= 4 \\ t_{pd\ \text{sum}} &= 75 \text{ nsec} \\ t_{pd\ \text{carry}} &= 50 \text{ nsec} \\ \text{Delay for 1 addition} &= 3 \times 50 + 75 \\ &= 225 \text{ nsec} \\ \text{Rate of addition} &= \frac{1}{225 \times 10^{-9}} \\ &= \frac{1000 \times 10^6}{225} = 4.4 \times 10^6 \text{ additions/sec} \end{aligned}$$

$\therefore \quad A = 4.4$

71. (d)

From the truth table,

$$f = \bar{A}\bar{B}\bar{C}W + \bar{A}\bar{B}CX + \bar{A}B\bar{C}Y + A\bar{B}\bar{C}Z$$



$$f = \bar{B}\bar{C} + \bar{A}\bar{B}D + \bar{A}B\bar{C}\bar{D}$$

$$f = (A + \bar{A})\bar{B}\bar{C} + \bar{A}\bar{B}D + \bar{A}B\bar{C}\bar{D}$$

$$f = A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}D + \bar{A}B\bar{C}\bar{D}$$

On comparing, $W = 1, X = D, Y = d, Z = 1$

72. (d)

Let the base of the system be P, then

$$9 \times 8 \times 5 = (190)_P$$
$$360 = P^2 + 9P$$
$$P^2 + 9P - 360 = 0$$
$$(P - 15)(P + 24) = 0$$
$$P = 15 \quad \because P > 0$$

Sum of roots $a = 5 + 8 + 9 = (22)_{10} = (17)_{15} = (16)_{16}$

Sum of the product of roots

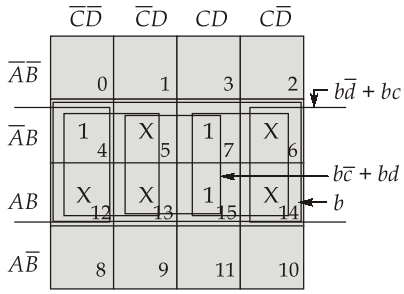
$$b = 5 \times 8 + 5 \times 9 + 8 \times 9 = (157)_{10}$$
$$b = (A7)_{15} = (9D)_{16}$$

In hexadecimal system, the equation is

$$x^3 - 16x^2 + 9Dx - 168 = 0$$

73. (d)

$$f_2 = \Sigma m(4, 7, 15) + \Sigma d(5, 6, 12, 13, 14)$$



From the K-MAP,

$$f = b\bar{d} + bc = b(\bar{d} + c)$$

$$f = b\bar{c} + bd = b(\bar{c} + d)$$

$$f = b(c + \bar{c}) = b(d + \bar{d}) = b$$

74. (d)

The dual of a Boolean expression can easily be obtained by interchanging sums and products and interchanging 0 as well as 1 whereas to obtain the complement of the function, the variable is also complemented. Hence, the Statement (I) is incorrect.

75. (b)

- Large random access memory (RAM) is used for the main memory because it has greater storage densities and is less expensive.
- ROM is used to store system programs, library, subroutines etc. because it stores the information permanently on the chip that cannot be changed by users.

❍❍❍❍