DETAILED SOLUTIONS

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ESE 2024 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 2

Section A : Network Theory

Section B : Digital Circuits

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11.	(c)	26.	(a)	41.	(a)	56.	(d)	71.	(c)
12.	(a)	27.	(b)	42.	(b)	57.	(c)	72.	(b)
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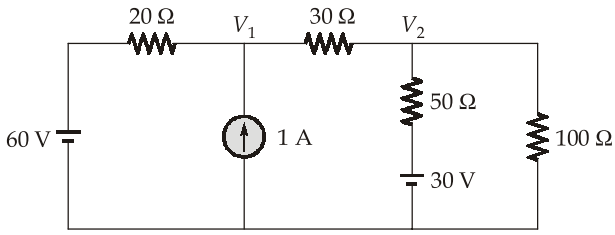
14.	(a)	29.	(b)	44.	(c)	59.	(c)	74.	(b)
15.	(d)	30.	(c)	45.	(a)	60.	(d)	75.	(b)

DETAILED EXPLANATIONS
Section A : Network Theory

1. (c)

Given circuit is



Applying KCL at node 1,

$$\frac{V_1 - 60}{20} + \frac{V_1 - V_2}{30} = 1$$

$$\Rightarrow \quad \frac{3V_1 - 180 + 2V_1 - 2V_2}{60} = 1$$

$$\Rightarrow \quad 5V_1 - 2V_2 = 60 + 180$$

$$\Rightarrow \quad 5V_1 - 2V_2 = 240 \qquad \text{...(i)}$$

$$\frac{V_2 - V_1}{30} + \frac{V_2 - 30}{50} + \frac{V_2}{100} = 0$$

$$\Rightarrow \quad \frac{10V_2 - 10V_1 + 6V_2 - 180 + 3V_2}{300} = 0$$

$$\Rightarrow \quad -10V_1 + 19V_2 = 180 \qquad \text{...(ii)}$$

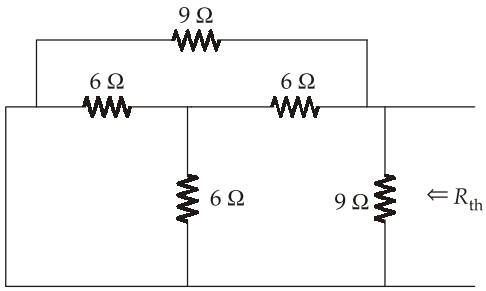
Solving equation (i) and (ii),

$$V_1 = 54.6 \text{ V}$$
$$V_2 = 44 \text{ V}$$

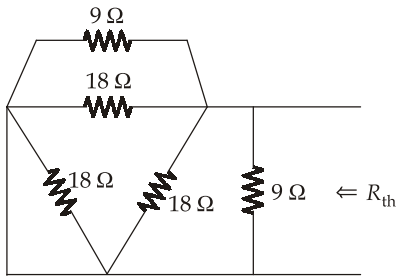
$$I_{100\ \Omega} = \frac{V_2}{100} = \frac{44}{100} = \frac{1.84}{5} = 0.44 \text{ A}$$

2. (b)

To calculate R_{th}, deactivate all independent sources.



Using star to delta transformation,



$$R_{th} = 9 \parallel [(9 \parallel 18) \parallel 18] = 9 \parallel \frac{9}{2} = \frac{9 \times \frac{9}{2}}{9 + \frac{9}{2}} = \frac{9 \times 9}{27} = 3\ \Omega$$

For maximum power transfer, $R_L = R_{th} = 3\ \Omega$

3. (b)

$$V(t) = 10 \sin \omega t\ \text{V}$$
$$\text{B.W} = 400\ \text{rad/s}$$
$$V_{rms} = \frac{10}{\sqrt{2}} = 7.07\ \text{V}$$
$$\text{B.W} = \frac{R}{L}$$
$$400 = \frac{100}{L}$$
$$L = 0.25\ \text{H}$$
$$Q_0 = \frac{V_c}{V} = \frac{500}{7.07} = 70.72$$

We have, $Q_0 = \frac{1}{R}\sqrt{\frac{L}{C}}$

$$70.72 = \frac{1}{100}\sqrt{\frac{0.25}{C}}$$
$$(70.72 \times 100)^2 = \frac{0.25}{C}$$
$$C = \frac{0.25}{(7072)^2} = 4.99 \times 10^{-9}\ \text{F}$$

4. (d)

Given data, Power factor = 0.6 (lag)

$$\cos\theta = 0.6$$
$$\theta = \cos^{-1}(0.6) = 53.13°$$

According to given circuit,

$$Z_{eq} = \frac{R_2(1+2j)}{R_2 + 1 + j2}$$

$$\angle\theta = \tan^{-1}2 - \tan^{-1}\frac{2}{R_2+1}$$

$$\angle 53.13^\circ = \tan^{-1}\frac{2-\dfrac{2}{R_2+1}}{1+\dfrac{4}{R_2+1}}$$

$$\tan(53.13^\circ) = \frac{2R_2+2-2}{R_2+5}$$

$$\frac{4}{3}(R_2+5) = 2R_2$$

$$4R_2 + 20 = 6R_2$$

$$2R_2 = 20$$

$$R_2 = 10\ \Omega$$

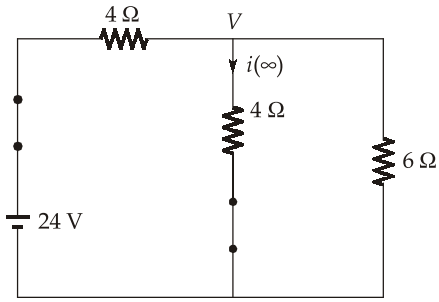
5. (d)

At $t = 0^-$, the source is disconnected

$$i_L(0^-) = i_L(0^+) = 0$$

for $t > 0$, the source is connected to circuit.

In steady state, inductor acts as short circuit. Applying nodal analysis,



$$\frac{V-24}{4}+\frac{V}{4}+\frac{V}{6} = 0$$

$$\frac{3V-72+3V+2V}{12} = 0$$

$$8\ V = 72$$

$$V = 9\ V$$

$$i_L(\infty) = \frac{V}{4} = \frac{9}{4}\text{A}$$

$$i(t) = \left[i(0^+)-i(\infty)\right]e^{-\frac{t}{\tau}} + i(\infty)$$

$$i(t) = \frac{9}{4}+\left(0-\frac{9}{4}\right)e^{-\frac{t}{\tau}} \qquad \ldots(1)$$

$$\tau = \frac{L}{R_{eq}} = \frac{0.8}{6.4} = \frac{1}{8}$$

Where, $R_{eq} = \dfrac{6\times 4}{10}+4 = 6.4\ \Omega$

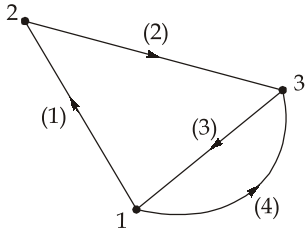
$\therefore$ $i(t) = \dfrac{9}{4}(1-e^{-8t})\text{A};\ t > 0$

6. (b)

To draw the graph,

1. Replace all resistors, inductors and capacitors by line segments.
2. Replace voltage source by short circuit and current source by an open circuit.

3. Assume directions of branch currents arbitrarily.
4. Number all the nodes and branches.



Complete incidence matrix (A_a)

$$A_a = \begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{cccc} 1 & 2 & 3 & 4 \end{array} \\ \begin{bmatrix} 1 & 0 & -1 & 1 \\ -1 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 \end{bmatrix} \end{array}$$

The reduced incidence matrix A is obtained by eliminating the last row from matrix A_a.

$$A = \begin{bmatrix} 1 & 0 & -1 & 1 \\ -1 & 1 & 0 & 0 \end{bmatrix}$$

The number of possible trees = $|AA^T|$

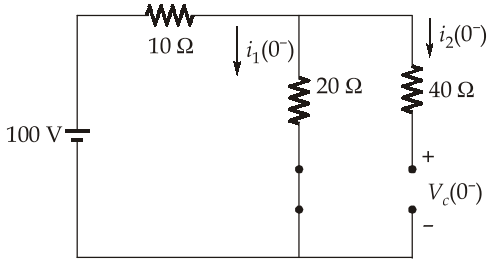
$$AA^T = \begin{bmatrix} 1 & 0 & -1 & 1 \\ -1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} 1 & -1 \\ 0 & 1 \\ -1 & 0 \\ 1 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 3 & -1 \\ -1 & 2 \end{bmatrix}$$

$$|AA^T| = \begin{vmatrix} 3 & -1 \\ -1 & 2 \end{vmatrix} = 6 - 1 = 5$$

7. (a)

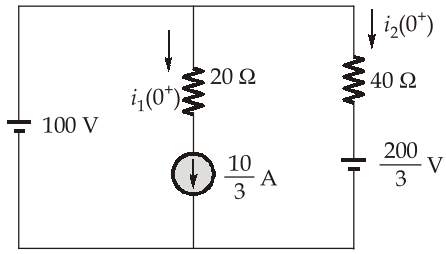
At $t = 0^-$



$$i_1(0^-) = i_1(0^+) = \frac{100}{30} = \frac{10}{3}\text{A}$$

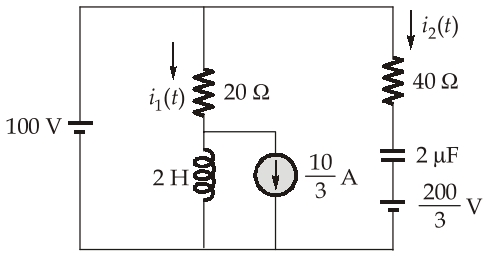
$$V_c(0^-) = V_c(0^+) = \frac{10}{3} \times 20 = \frac{200}{3}\text{V}$$

For $t = 0^+$



$$i_2(0^+) = \frac{100 - \frac{200}{3}}{40} = \frac{100}{3 \times 40} = \frac{25}{30}\text{A}$$

For $t > 0$



Writing KVL equations for $t > 0$

$$40i_2 + \frac{1}{2 \times 10^{-6}}\int_0^t i_2\,dt = 100 - \frac{200}{3} = \frac{100}{3}$$

$$40\frac{di_2}{dt} + \frac{1}{2} \times 10^6 i_2 = 0$$

$$\frac{di_2(0^+)}{dt} = -\frac{1}{2} \times 10^6 \left[i_2(0^+)\right] \times \frac{1}{40}$$

$$= -\frac{1}{2 \times 40} \times 10^6 \times \frac{25}{30} = \frac{-1 \times 10^6}{2 \times 8 \times 6}$$

$$= \frac{-1000 \times 10^3}{2 \times 8 \times 6} = \frac{-125}{12} \times 10^3 = -10.415 \times 10^3\,\text{A/s}^2$$

$$\frac{di_2(0^+)}{dt} = -10.415 \times 10^3\ \text{A/s}^2$$

8. (a)

at $t = 0^-$

$$V_c(0^-) = V_c(0^+) = 0\ \text{V}$$

at $t > 0$

$$V_c(\infty) = 1\ \text{V}$$

$$V_c(t) = 1\left(1 - e^{-\frac{t}{RC}}\right)$$

$$\frac{dV(t)}{dt} = \frac{1}{RC}e^{-\frac{t}{RC}}$$

$$\frac{dV(0^+)}{dt} = \frac{1}{RC}$$

9. (b)

$$i(t) = \frac{-4\times10^{-3}}{8}[V(t)-8]$$

$$i(t) = -\frac{1}{2}\times10^{-3}[V(t)-8] = -\frac{1}{2}\times10^{-3}V(t)+4\times10^{-3}$$

$$V(t) = \frac{2i(t)-8\times10^{-3}}{-10^{-3}} = -2\times10^{3}i(t)+8$$

Hence, $R_{th} = 2\times10^{3}\ \Omega$

$$\text{Time constant} = \tau = \frac{L}{R_{th}} = \frac{8\times10^{-3}}{2\times10^{3}} = 4\ \mu s$$

10. (d)

According to given circuit

$$V_2 = -5I_2$$

Substituting the value of V_2 in the given equation,

$$V_1 = -25I_2 - 6I_2$$

$$V_1 = -31I_2$$

$$I_1 = 8\times(-5I_2) - 3I_2$$

$$I_1 = (-40-3)I_2 = -43I_2$$

Input impedance

$$Z_i = \frac{V_1}{I_1} = \frac{-31}{-43} = \frac{31}{43}\Omega$$

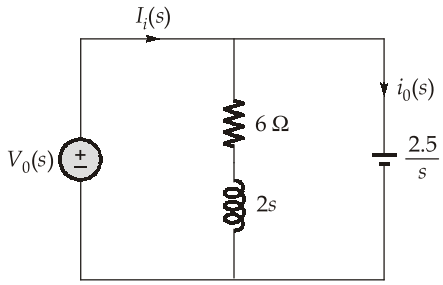
11. (c)

$Y_{12} \neq Y_{21}$, hence network is non reciprocal

$\frac{Y_{12}}{Y_{21}} = \frac{-1/3}{1/3} = -\text{Ve}$, hence network is active.

12. (a)

In s-domain, the circuit can be drawn as below:



The admittance

$$Y(s) = \frac{1}{6+2s} + \frac{s}{2.5} = \frac{1}{2(s+3)} + \frac{2}{5}s = \frac{5+4s(s+3)}{10(s+3)}$$

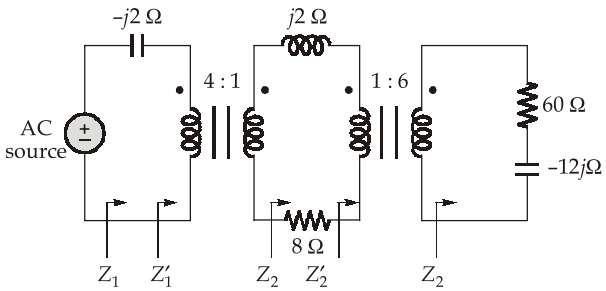
$$Y(s) = \frac{4s^2+12s+5}{10(s+3)}$$

$$Z(s) = \frac{1}{Y(s)} = \frac{10(s+3)}{4s^2+12s+5}$$

Poles, $s = -0.5, -2.5$

Zero $\Rightarrow$ $s = -3$

13. (d)



$$\frac{Z_2'}{Z_3} = \frac{1}{36} \Rightarrow Z_2' = \left[\frac{60-12j}{36}\right]\Omega$$

$$Z_2' = \left(\frac{5}{3} - \frac{j}{3}\right)\Omega = \frac{5-j}{3}\Omega$$

So, $$Z_2 = 8 + 2j + \frac{5-j}{3} = \frac{24+6j+5-j}{3} = \frac{29+5j}{3}$$

$$\frac{Z_1'}{Z_2} = 16 \Rightarrow Z_1' = 16\left(\frac{29}{3} + \frac{5}{3}j\right)$$

So, $$Z_1 = -2j + Z_1' = -2j + 16\left(\frac{29+5j}{3}\right)$$

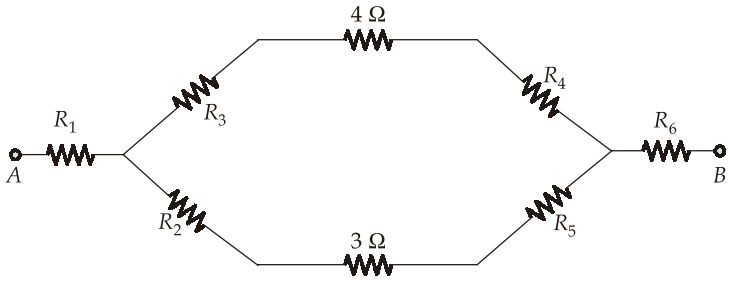
$$= \frac{-6j+464+80j}{3} = \frac{464+74j}{3}$$

$$Z_1 = \left(\frac{464+74j}{3}\right)\Omega$$

Z_1 is the impedance seen by ac source.

14. (a)

Converting the two delta network formed by resistors 4.5 Ω, 3 Ω and 7.5 Ω into equivalent star network, we have,

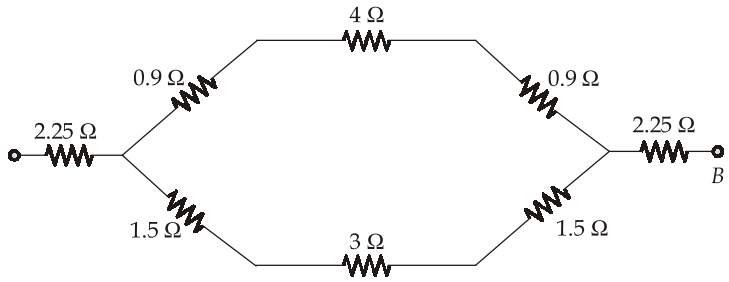


$$R_1 = R_6 = \frac{4.5 \times 7.5}{4.5 + 7.5 + 3} = 2.25\ \Omega$$

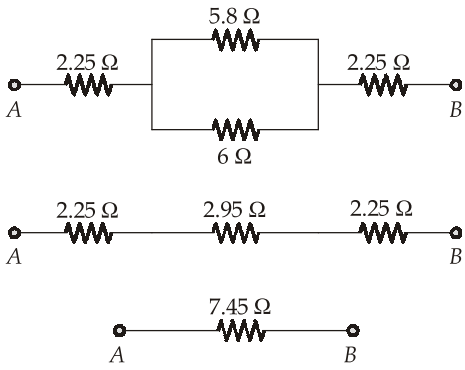
$$R_2 = R_5 = \frac{7.5 \times 3}{4.5 + 7.5 + 3} = 1.5\ \Omega$$

$$R_3 = R_4 = \frac{4.5 \times 3}{4.5 + 7.5 + 3} = 0.9\ \Omega$$

The simplified network is



The network can be simplified as follows:



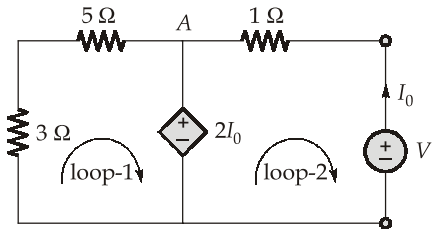
$$R_{AB} = 7.45\ \Omega$$

15. (d)

For the given tree, the possible fundamental cut-sets are {1, 6, 8}, {2, 6, 8, 3}, {8, 7, 5, 3} and {4, 7, 8}.

16. (c)

To calculate R_{th}, the equivalent circuit is



KVL in loop-1

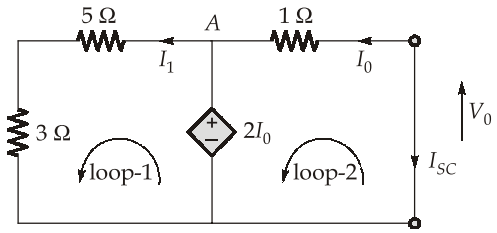
$$8I + 2I_0 = 0 \qquad \text{...(i)}$$

KVL in loop-2

$$V = I_0 + 2I_0$$

$$\frac{V}{I_0} = 3\ \Omega = R_{th}$$

Calculate V_{th}



$$I_{sc} = -I_0$$

KVL in loop-1

$$2I_0 = 8I_1$$

$$I_1 = \frac{1}{4}I_0 \qquad \text{...(ii)}$$

KVL in loop-2

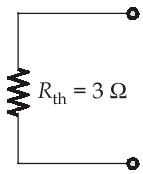
$$3I_0 = 0$$

$$I_0 = 0$$

Hence, $I_{sc} = 0$

$\therefore$ $V_{th} = R_{th}\, I_{sc} = 0$ V

Thevenin equivalent circuit is



17. (d)

According to reciprocity theorem,

$$\frac{V_x}{I_y} = \frac{V_y}{I_x}$$

18. (c)

Whenever an ideal voltage source and ideal current source are connected in series, the current through the combination would be same as the current source. Hence, it will behave like an ideal current source alone and if they are connected in parallel, it will behave like an ideal voltage source alone.

19. (b)

20. (b)

- Forced current is the current due to the external voltage source while the initial condition is zero, which gives zero state response.
- Natural current is the current because of initial conditions with all external voltage sources set to zero, which gives zero input response.

21. (c)

For a series RLC circuit,

$$X_{eq} = |X_L - X_C| = \omega L - \frac{1}{\omega C}$$

At low frequency, $\omega L << 1/\omega C$, hence the circuit impedance is capacitive with

$$X_{eq} = -\frac{1}{\omega C}$$

At high frequency, $\omega L >> 1/\omega C$, hence the circuit impedance is inductive with

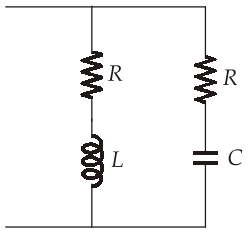
$$X_{eq} = \omega L$$

22. (d)

Tie set matrix gives the relation between the tie set currents and branch currents. Thus, the order of B_f is $(b - n + 1) \times b$ and it's rank is $(b - n + 1)$. Further, the submatrix corresponding to twigs (B_t) is not an identity matrix and the submatrix corresponding to links (B_l) is a identity matrix of order $(b - n + 1)$.

23. (d)

For unity power factor, imaginary term of impedance should be zero.



$$Z(j\omega) = \frac{(R + j\omega L)\left(R - \frac{j}{\omega C}\right)}{R + j\omega L + R - \frac{j}{\omega C}}$$

$$Z(j\omega) = \frac{(R + j\omega L)\left(R - \frac{j}{\omega C}\right)\left(2R - j\omega L + \frac{j}{\omega C}\right)}{\left(2R + j\omega L - \frac{j}{\omega C}\right)\left(2R - j\omega L + \frac{j}{\omega C}\right)}$$

$$\text{Imaginary term} = \left(\omega L R^2 - \frac{R^2}{\omega C}\right) - \left(\frac{\omega L^2}{C} - \frac{L}{\omega C^2}\right)$$

$$= R^2\left(\omega L - \frac{1}{\omega C}\right) - \frac{L}{C}\left(\omega L - \frac{1}{\omega C}\right)$$

For unity power factor, Imaginary term = 0

$$\left(R^2 - \frac{L}{C}\right)\left(\omega L - \frac{1}{\omega C}\right) = 0$$

$$R = \sqrt{\frac{L}{C}}$$

24. (d)

From linearity,

$$V_{out} = K_1 V_{s1} + K_2 i_{s2}$$

For $V_{s1} = 6$ V, $i_{s2} = 0$, $V_{out} = 5$ V, hence

$$V_{out} = 6K_1$$

$$5 = 6K_1 \quad \Rightarrow \quad K_1 = \frac{5}{6}$$

For $V_{s1} = 0$, $i_{s2} = 3$ A, $V_{out} = 8$ V, hence

$$V_{out} = K_1 \times 0 + 3 \times K_2$$

$$8 = 3K_2$$

$$K_2 = \frac{8}{3}$$

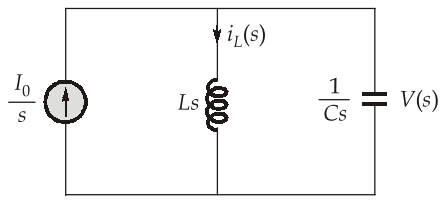
Therefore for $V_{s1} = 12$ V and $i_{s2} = 9$ A

$$V_{out} = \frac{5}{6}V_{s1} + \frac{8}{3}i_{s2} = \frac{5}{6} \times 12 + \frac{8}{3} \times 9$$

$$= 10 + 24 = 34 \text{ V}$$

25. (c)

For $t > 0$



$$V(s) \times Cs + \frac{V(s)}{Ls} = \frac{I_0}{s}$$

$$V(s)[LCs^2+1] = \frac{I_0}{s}\times Ls$$

$$V(s) = I_0 \times \frac{L}{LC\left(s^2+\frac{1}{LC}\right)}$$

$$= \frac{I_0}{C}\times\frac{1}{\left(s^2+\frac{1}{LC}\right)} = \frac{I_0}{C}\times\frac{\frac{1}{\sqrt{LC}}\times\sqrt{LC}}{\left(s^2+\frac{1}{LC}\right)}$$

$$\Rightarrow \quad V(t) = I_0\sqrt{\frac{L}{C}}\sin(\omega_0 t)$$

$$V(t) = \frac{I_0}{\omega_0 C}\sin(\omega_0 t)\ \text{V}$$

26. (a)

When, load $Z_L = 500\ \angle -90° = -j500\ \Omega$

$$Z_{eq} = [Z_L \parallel 500\ \Omega]$$

$$Z_{eq} = \frac{-500j\times 500}{500-500j} = \frac{-500j}{1-j}$$

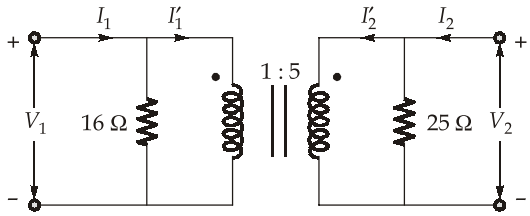
$$= 250\sqrt{2}\angle -90° - 180° + \tan^{-1}1$$

$$= 250\sqrt{2}\angle -225°$$

Power factor, $\cos\phi = \cos(-225°)$

$\cos\phi = 0.707$ (lag)

27. (b)



$$\frac{V_1}{V_2} = \frac{1}{5}$$

$$\frac{I_1'}{I_2'} = -5$$

$$I_1' = -5I_2'$$

$$V_1 = 16I_1 - 16I_1'$$

$$V_1 = 16I_1 + 80I_2'$$

$$I_2' = I_2 - \frac{V_2}{25}$$

$$V_1 = 16I_1 + 80I_2 - \frac{80}{25}V_2$$

$$= 16I_1 + 80I_2 - \frac{16}{5}V_2$$

$$17V_1 = 16I_1 + 80I_2$$

$$V_1 = \frac{16}{17}I_1 + \frac{80}{17}I_2 \quad ..(i)$$

from (i),

$$\frac{V_2}{5} = \frac{16}{17}I_1 + \frac{80}{17}I_2$$

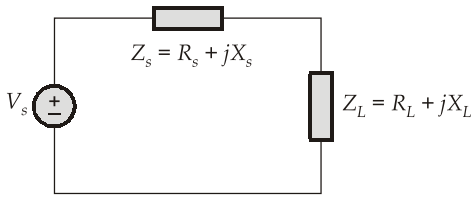
$$V_2 = \frac{80}{17}I_1 + \frac{400}{17}I_2 \quad ...(ii)$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{16}{17} & \frac{80}{17} \\ \frac{80}{17} & \frac{400}{17} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$[z] = \begin{bmatrix} \frac{16}{17} & \frac{80}{17} \\ \frac{80}{17} & \frac{400}{17} \end{bmatrix} \Omega$$

28. (d)

29. (b)



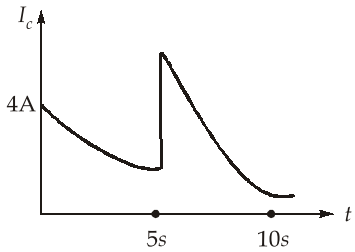
For maximum power transfer

$$Z_L = Z_s^*$$

i.e., $R_L = R_S$ and $X_L = -X_S$

30. (c)

When the switch S_1 is closed at $t = 0$, $I_c(0^+) = 24/6 = 4$A which decays exponentially with time constant $RC = 6 \times 2 = 12$s. At $t = 5$s, $V_c(5) = 24\,(1 - e^{-5/12}) = 8.178$ V. Since, with S_2 closed at $t = 5$s, 4 Ω is shorted, I_c jumps to a new value given by $I_c(t = 5) = V_c(t = 5)/2 = 4.089$ A which then exponentially decreases with reduced time constant.



31. (a)

For $V_0 \propto \frac{dV_i}{dt}$

$V_0(s) = KsV_i(s)$

where K is any constant.

from the circuit, $V_0(s) = \frac{sRC}{1+sRC}V_i(s)$

For the required condition, $RC << T$.

32. (d)

Loop analysis is based on analyzing the network with the help of KVL equations. The loop matrix so obtained from the simultaneous equations cannot be zero and negative and is independent of voltage and current sources and depends on the value of resistances.

33. (d)

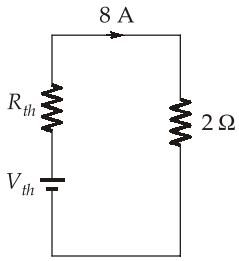
Given circuit,

$$\text{Slope} = \frac{di(t)}{dt} = \frac{5}{4}\text{A/s}$$

For inductor, $V_L = L\frac{di(t)}{dt}$

$$3 = L\frac{5}{4} \Rightarrow L = \frac{12}{5} = 2.4\,\text{H}$$

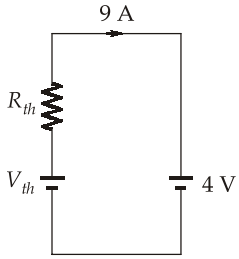
34. (a)



$$I = \frac{V_{th}}{R_{th}+2} \Rightarrow 8 = \frac{V_{th}}{R_{th}+2}$$

$8R_{th} + 16 = V_{th}$

$V_{th} - 8R_{th} = 16$ ...(1)



$$I = \frac{V_{th} - 4}{R_{th}}$$

$$9 = \frac{V_{th} - 4}{R_{th}}$$

$$9R_{th} = V_{th} - 4$$

$$V_{th} - 9R_{th} = 4 \quad \text{...(ii)}$$

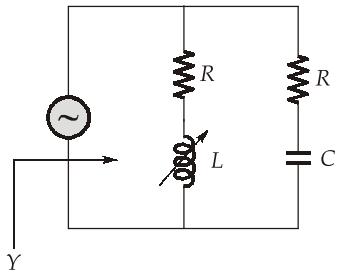
From equation (i) and (ii)

$$R_{th} = 12\ \Omega$$

$$V_{th} = 16 + 8 \times 12$$

$$= 112\ \text{V}$$

35. (a)



$$Y = \frac{1}{R + jX_L} \times \frac{R - jX_L}{R - jX_L} + \frac{1}{R - jX_C} \times \frac{R + jX_C}{R + jX_C}$$

$$= \frac{R - jX_L}{R^2 + X_L^2} + \frac{R + jX_C}{R^2 + X_C^2}$$

For the resonance, imaginary part of admittance is equal to zero.

$$\frac{-X_L}{R^2 + X_L^2} + \frac{X_C}{R^2 + X_C^2} = 0$$

$$\frac{X_L}{R^2 + X_L^2} = \frac{X_C}{R^2 + X_C^2}$$

$$X_L(R^2 + X_C^2) = X_C(R^2 + X_L^2)$$

$$X_L R^2 + X_L X_C^2 = X_C R^2 + X_C X_L^2$$

$$R^2 + X_L^2 = \frac{1}{X_C}(X_L R^2 + X_L X_C^2)$$

$$X_L^2 - \left(\frac{R^2}{X_C} + X_C\right) X_L + R^2 = 0$$

The equation is quadratic giving two values of inductor for which the circuit exhibits resonance.

36. (a)

37. (c)

Other requirements for reciprocity theorem:

(i) Network should have only single-source.

(ii) Network should not have dependent sources.

Section B : Digital Circuits

38. (c)

$(10)_{10} = (1010)_2$ [Switches D_3 and D_1 are closed]

The current flowing in 12.5 kΩ branch,

$$I_3 = \frac{5\text{ V}}{12.5\text{ k}\Omega} = 0.4\text{ mA}$$

The current flowing in 50 kΩ branch,

$$I_1 = \frac{5V}{50\text{ k}\Omega} = 0.1\text{ mA}$$

$$V_{out} = -[(0.4)\text{mA} + 0.1\text{ mA}] \times 20\ (\text{k}\Omega)$$
$$= -10\text{ V}$$

The negative sign is present because the summing amplifier is a polarity-inverting amplifier.

39. (c)

$(15)_{10} = (1\ 1\ 1\ 1)_2$

$(10W1Z)_2 \times (1111)_2$ is calculated as

$$\begin{array}{r} 10W1Z \longrightarrow 1 \\ 10W1Z \\ 10W1Z \\ 10W1Z \\ \hline Y0101\,1001 \end{array}$$

From above, we get $W = Y = Z = 1$

40. (c)

Number of quantization levels for 12-bit DAC

$= 2^{12} = 4096$

$$\text{Resolution} = \frac{1}{2^{12}-1} = 0.244 \times 10^{-3}$$

The smallest reading possible which corresponds to 1 LSB is $0.244 \times 10^{-3} \times 10$

$= 2.44$ mV

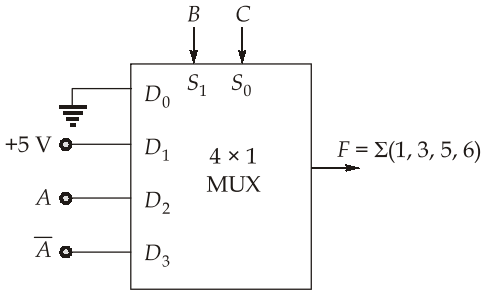
41. (a)

A	B	C	
0	0	0	(Q_1: OFF, Q_2: OFF, Q_3:ON)
0	1	1	(Q_1: OFF, Q_2: ON, Q_3:OFF)
1	0	1	(Q_1: ON, Q_2: OFF, Q_3:OFF)
1	1	1	(Q_1: ON, Q_2: ON, Q_3:OFF)

42. (b)

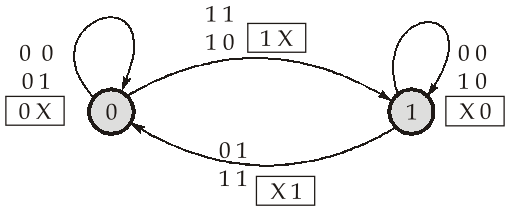
$F(A, B, C) = \Sigma(1, 3, 5, 6)$

	D_0	D_1	D_2	D_3
$\overline{A}$	0	①	2	③
A	4	⑤	⑥	7
	0	1	A	$\overline{A}$



43. (c)

Present State	Inputs		Next State
Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



44. (c)

$(0\ 0\ 1\ 1\ 0\ 0\ 1\ 0) = (50)_{10}$

$1\ V = K \times 50 \Rightarrow K = 20\ mV$

The largest output will occur for an input of $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1)_2 = (255)_{10}$

$V_{out(max)} = 20\ mV \times (255)_{10}$

$= 5.10\ V$

45. (a)

- For ECL logic family, the logic levels are negative, with logic 1 having a level of –0.9 V and logic 0 having a level of –1.7 V which are not compatible with other logic family gates.
- In ECL, the current is continuously being drawn, hence dissipating significantly more power than those of other logic families.

46. (c)

The given circuit is a Binary Ripple Up Counter. The output is cleared when Q_BQ_C =11 corresponding to the state

$$\begin{array}{ccc} Q_C & Q_B & Q_A \\ 1 & 1 & 0 \end{array} \longrightarrow \text{Mod 6 ripple counter}$$

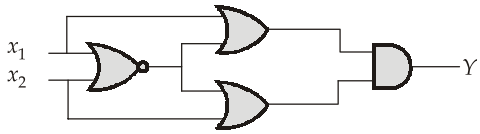
47. (c)

- A synchronous sequential machine M is characterized by a quintuple given by $M = (x, z, y, f, F)$ where x = a set of input functions, z = a set of output functions, y = a set of various states of the machine, $f = f(x_i, y_i)$ = state-transition function and $F = F(x, y)$, an output function.
- Synchronous sequential machines are typically deterministic i.e. if the input sequence is repeated, then the output sequence is repeated.
- As the number of states increases further, more bits are used for encoding.
- In a Mealy circuit, output depends on the present state and current input.
- In a Moore circuit, output depends only on the present state.

48. (d)

OR-AND logic is equivalent to NOR-NOR logic, hence we get

$$Y = (X_1 + \overline{X_1 + X_2}) \cdot (X_2 + \overline{X_1 + X_2})$$



$$Y = (X_1 + \overline{X_1} \cdot \overline{X_2}) \cdot (X_2 + \overline{X_1} \cdot \overline{X_2})$$

$$Y = (X_1 + \overline{X_2})(X_1 + \overline{X_1})(X_2 + \overline{X_1})(X_2 + \overline{X_2})$$

$$Y = (X_1 + \overline{X_2})(X_2 + \overline{X_1})$$

$$Y = X_1X_2 + \overline{X_1} \cdot \overline{X_2} = X_1 \odot X_2 = \overline{X_1 \oplus X_2}$$

49. (d)

For 10 bit ring counter, $f_{out} = \dfrac{f_{clk}}{10} = \dfrac{100\text{ kHz}}{10}$

Clock output at 'P' $f_{out} = 10$ kHz

$\Rightarrow$ For MOD-20 ripple counter

$$f_{out} = \frac{10\text{ kHz}}{20}$$

Clock output at 'Q' $\Rightarrow$ $f_{out} = 0.5$ kHz

$\Rightarrow$ For 4 bit parallel counter,

$$f_{out} = \frac{0.5\,\text{kHz}}{16}$$

Clock output at 'R' $f_{out} = 31.25$ Hz

$\Rightarrow$ For 4 bit Johnson counter

$$f_{out} = \frac{31.25}{2 \times 4} = 3.9\,\text{Hz}$$

Clock output at 'S' $f_{out} = 3.9$ Hz

50. (d)

$$S = A \odot B$$
$$R = B$$
$$Q_{n+1} = S + \bar{R}Q = A \odot B + \bar{B}Q$$
$$Q^{+} = \bar{A}\bar{B} + AB + \bar{B}Q$$

51. (d)

A	B	C	(P) Sum/Difference	(Q) Carry	(R) Borrow
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

$$\text{Sum} = \Sigma m(1, 2, 4, 7)$$
$$\text{Carry} = \Sigma m(3, 5, 6, 7)$$
$$\text{Borrow} = \Sigma m(1, 2, 3, 7)$$

Hence, the ROM can be used as a Full Adder with P as the Sum and Q as the Carry. Also, the ROM can be used as a subtractor with P as the Difference and R as the Borrow.

52. (a)

Size of decoder : $n \times 2^n$

For 32×10 ROM circuit, decoder has $32 = 2^n$ outputs.

$\Rightarrow$ $n = 5$

$\therefore$ Size of decoder $= 5 \times 32$

53. (b)

Initially before the clock, D-FF output is 0 and input of XOR gate is 0 and b_7.

So, after 1 clock pulse, $b_7 \oplus 0 = b_7$

after 2 clock pulse, $b_7 \oplus b_6$

after 3 clock pulse, $b_6 \oplus b_5$

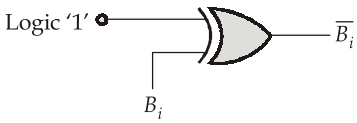
So, it will work as binary to gray code converter.

54. (b)

From the given 4 bit binary parallel adder,

$A_3 = A_0 = 1$; $A_2 = A_1 = 0$; $C_{in} = 1$

For EX-OR gates:



Which is the complement of given input.

Therefore, the output of 4 bit binary parallel adder,

$$S_3\ S_2\ S_1\ S_0 = 1001 + 1\text{'s complement } (B_3\ B_2\ B_1\ B_0) + C_{in}$$
$$= 1001 + 2\text{'s complement } (B_3\ B_2\ B_1\ B_0)$$
$$= 1001 - (B_3\ B_2\ B_1\ B_0)$$

($\because$ negative numbers are represented by corresponding 2's complement.)

$$= 9 - B$$

$S_3\ S_2\ S_1\ S_0$ = 9's complement of B.

55. (d)

Binary	Gray
0000 →	0000 (0)
0001 →	0001 (1)
0010 →	0011 (3)
0011 →	0010 (2)
0100 →	0110 (6)
0101 →	0111 (7)
0110 →	0101 (5)
0111 →	0100 (4)
1000 →	1100 (12)
1001 →	1101 (13)

$\therefore$ Addition of decimal equivalent of all gray code:

1 + 3 + 2 + 6 + 7 + 5 + 4 + 12 + 13 = 53

56. (d)

In a staircase switch, the switch in each floor has independent control over the lamp irrespective of the position of the switch in other floor. It can be implemented by an XOR Gate. For option (d),

$$Y = \overline{AB} + \overline{A\overline{B}} = \overline{A} + \overline{B} + \overline{A} + \overline{\overline{B}}$$

$$Y = \overline{A} + \overline{B} + \overline{A} + B = \overline{A} + 1 = 1$$

Hence, option (d) does not represent XOR gate.

57. (c)

The maximum frequency at which the counter operates reliably is

$$f_{max} = \frac{1}{nt_{ff} + t_{strobe}} = \frac{10^3}{4 \times 50 + 30} \text{MHz}$$
$$= 4.35 \text{ MHz}$$

58. (b)

Eight clock pulses will be required, since the data is entered serially. Since the clock period is 100 ns, this shift register requires 800 ns to load the 8 bits.

59. (c)

The given state diagram detects overlapping sequence: 11011

60. (d)

For PMOS

$$Y = \overline{(A \cdot B)(C + D)}$$
$$Y = (\overline{AB}) + (\overline{C} \cdot \overline{D})$$
$$Y = (\overline{A} + \overline{B}) + (\overline{C} \cdot \overline{D})$$

61. (d)

The decimal equivalent value

$$D = b_7 2^7 + b_6 2^6 + b_5 2^5 + b_4 2^4 + b_3 2^3 + b_2 2^2 + b_1 2^1 + b_0 2^0$$

For input = 10001010

$$D = (1)2^7 + (0)2^6 + (0)2^5 + (0)2^4 + (1)2^3 + (0)2^2 + (1)2^1 + (0)2^0$$
$$D = 2^7 + 2^3 + 2 = 128 + 8 + 2 = 138$$

$\therefore$ $V_0 = 138 \times 10 \times 10^{-3} = 1.38$ V

62. (c)

Convert the expression in binary base,

$$111000$$
$$\downarrow$$
$$(101111)_2 \Rightarrow (47)_{10}$$

$$100011$$
$$\downarrow$$
$$(111101)_2 \Rightarrow (61)_{10}$$

$$111001$$
$$\downarrow$$
$$(101110)_2 \Rightarrow (46)_{10}$$

$\therefore$ $(47 + 61 - 46)_{10} = (62)_{10} = 111110$

63. (c)

$$\frac{(302)}{20} = 12.1$$

Let the base is b.

$$\frac{3\times b^2+0\times b^1+2\times b^0}{2\times b^1+0\times b^0} = 1\times b^1+2\times b^0+b^{-1}$$

$$\frac{3b^2+2}{2b} = b+2+\frac{1}{b}$$

$$\frac{3b^2+2}{2b} = \frac{b^2+2b+1}{b}$$

$$3b^2+2 = 2b^2+4b+2$$

$$b^2 = 4b$$

$$b = 4$$

64. (c)

The given circuit is a binary ripple up counter.

The clock frequency is 200 kHz.

$\therefore$

$$f_{Q_0} = \frac{f_{clk}}{2} = \frac{200}{2} = 100\text{ kHz}$$

$$f_{Q_2} = \frac{f_{clk}}{8} = \frac{200}{8} = 25\text{ kHz}$$

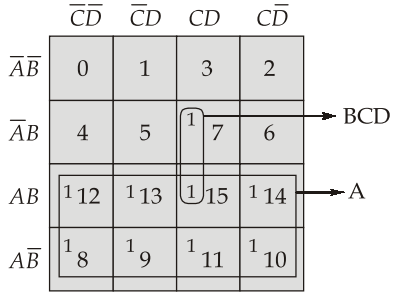
65. (a)

X	Y	A	B	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

$$F = \Sigma m(3, 4, 5, 6, 9, 10, 11, 12)$$

66. (c)

A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

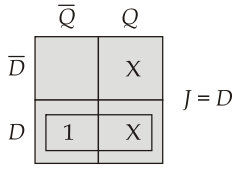


$$Z = A + BCD$$

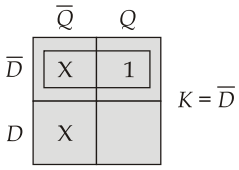
67. (d)

D	Q	Q^+	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

For J



For K



68. (c)

In a ladder-type D/A converter,

$$\text{LSB resistance} = (2^{n-1})\ \text{MSB resistance}$$

$$8\ \text{k}\Omega = (2^{n-1})\ 1\ \text{k}\Omega$$

$$2^{n-1} = 2^3$$

$$n - 1 = 3$$

$$n = 4$$

Let the increased bit length is n' then

$$n' = n + 2 = 4 + 2 = 6$$

So, 2 additional number of resistors are required and their values are 16 kΩ and 32 kΩ.

69. (d)

For NAND Gate, $\overline{A \cdot B} = \overline{B \cdot A}$ [follows commutative law]

$\overline{\overline{A \cdot B} \cdot C} = \overline{A \cdot \overline{B \cdot C}}$ [should be equal to follow associative law]

For easy understanding let $A = 1$, $B = 1$ and $C = 0$

$$\text{LHS} = \overline{\overline{A \cdot B} \cdot C}$$

$$= \overline{\overline{1 \cdot 1} \cdot 0} = \overline{0 \cdot 0} = 1$$

$$\text{RHS} = \overline{1 \cdot \overline{\overline{1 \cdot 0}}}$$

$$= \overline{1.1} = 0$$

$$\text{LHS} \neq \text{RHS}$$

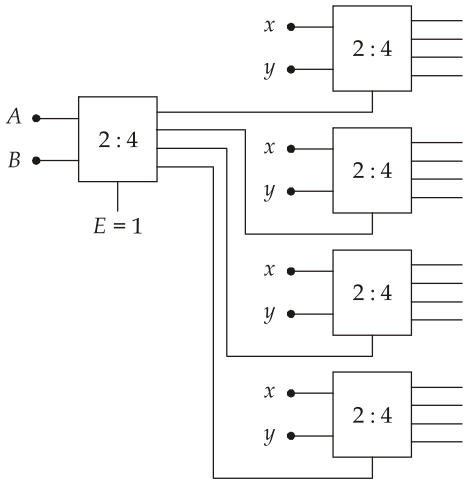
$\therefore$ NAND gate does not follow associative law.

70. (a)

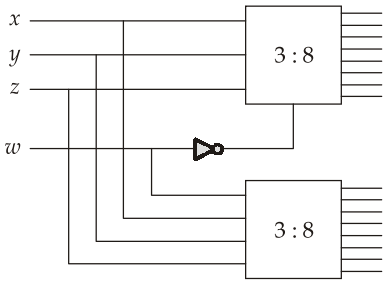
CD \ AB	00	01	11	10
00	X	0	0	X
01		0		X
11	0	X	0	X
10		X		X

$$Y = (C + D)(\overline{C} + \overline{D})(A + \overline{B})$$

71. (c)

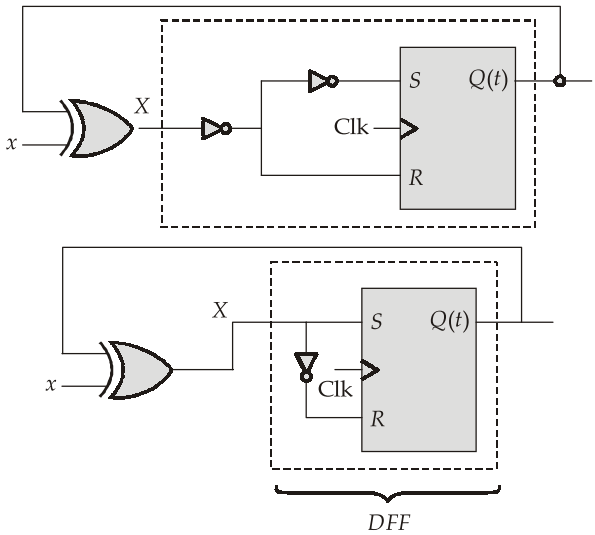


Five 2 : 4 decoders are required.



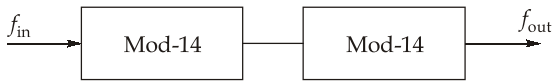
Two 3 : 8 decoders and an inverter are required to implement 4:16 decoder.

72. (b)



$$Q_{t+1} = x \oplus Q(t)$$

73. (c)



$$f_{out} = \frac{19 \times 10^3}{14 \times 14} \approx 96 \text{ Hz}$$

74. (b)

75. (b)

A multiplexer can be used as a logic element due to its ability to select one of several input signals as the output.

❍❍❍❍