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ESE 2024 : Prelims Exam
CLASSROOM TEST SERIES

ELECTRICAL ENGINEERING

Test 2

Section A : Electrical Circuits

Section B : Digital Electronics + Microprocessors

ANSWER KEY

1.	(a)	**16.**	(b)	**31.**	(c)	**46.**	(b)	**61.**	(c)
2.	(b)	**17.**	(c)	**32.**	(c)	**47.**	(d)	**62.**	(d)
3.	(c)	**18.**	(a)	**33.**	(d)	**48.**	(d)	**63.**	(b)
4.	(a)	**19.**	(d)	**34.**	(b)	**49.**	(d)	**64.**	(c)
5.	(a)	**20.**	(b)	**35.**	(c)	**50.**	(a)	**65.**	(b)
6.	(b)	**21.**	(b)	**36.**	(b)	**51.**	(d)	**66.**	(a)
7.	(c)	**22.**	(b)	**37.**	(d)	**52.**	(b)	**67.**	(d)
8.	(b)	**23.**	(b)	**38.**	(d)	**53.**	(c)	**68.**	(c)
9.	(c)	**24.**	(d)	**39.**	(c)	**54.**	(b)	**69.**	(b)
10.	(b)	**25.**	(a)	**40.**	(c)	**55.**	(c)	**70.**	(b)
11.	(c)	**26.**	(b)	**41.**	(b)	**56.**	(d)	**71.**	(b)
12.	(b)	**27.**	(b)	**42.**	(b)	**57.**	(b)	**72.**	(d)
13.	(b)	**28.**	(c)	**43.**	(d)	**58.**	(c)	**73.**	(c)
14.	(c)	**29.**	(c)	**44.**	(c)	**59.**	(b)	**74.**	(c)
15.	(b)	**30.**	(d)	**45.**	(c)	**60.**	(b)	**75.**	(d)

DETAILED EXPLANATIONS
Section A : Electrical Circuits

1. (a)

An ideal current source has the following features.

- It produces a constant current irrespective of the value of the voltage across it.
- It has infinite resistance.
- It is capable of supplying infinite power.

2. (b)

We know that,

Self inductance of a coil is, $L = \dfrac{\mu_0 N^2 A}{l}$

where, N is number of turns

$$\therefore \quad L \propto N^2$$

$$\frac{L_1}{L_2} = \left(\frac{N_1}{N_2}\right)^2$$

$$\frac{1}{0.25} = \left(\frac{N_1}{N_2}\right)^2$$

$$\therefore \quad \frac{N_1}{N_2} = 2$$

3. (c)

Given, nodes, $n = 7$

Independent loops, $b - (n - 1) = 4$

$$b - (7 - 1) = 4$$

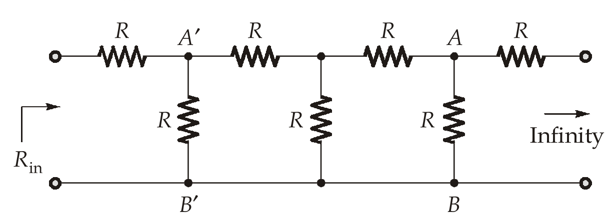
$$b - 6 = 4$$

$$b = 10$$

$\therefore$ number of branches, $b = 10$

4. (a)

Let the equivalent resistance be R_{in}



The network can be terminated at $A'B'$ instead of AB

$$R_{in} = (R_{in} || R) + R$$

$$RR_{in} + R_{in}^2 = RR_{in} + RR_{in} + R^2$$

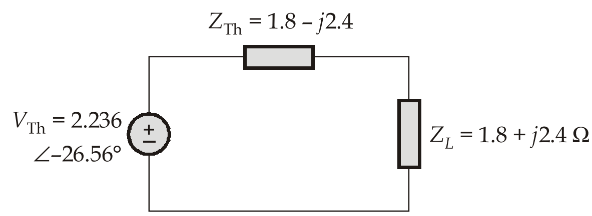
$$R_{in}^2 - R\,R_{in} - R^2 = 0$$

$$R_{in} = \frac{R + \sqrt{R^2 + 4R^2}}{2}$$

Taking positive sign, $R_{in} = R\left(\frac{1+\sqrt{5}}{2}\right)$

5. (a)

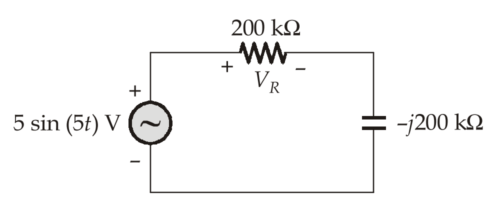
For maximum power, $Z_L = Z_{Th}^*$



$$P_{max} = \frac{V_{Th}^2}{4R_L} = \frac{(2.236)^2}{4 \times 1.8} = 0.694 \text{ W}$$

6. (b)

$$X_C = \frac{1}{\omega C} = \frac{1}{5 \times 10^{-6}} = 200 \text{ k}\Omega$$



$$\therefore \quad V_R = \frac{5\angle 0°}{(200 - j200)} \times 200$$

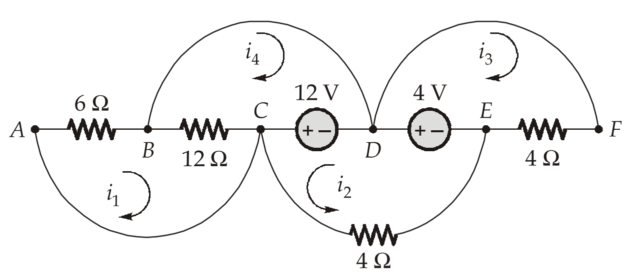
$$= \frac{5\angle 0°}{(1-j)} = \frac{5\angle 0°}{\sqrt{2}\angle -45°}$$

$$= 2.5\sqrt{2}\ \angle 45°$$

$$V_R = 2.5\sqrt{2}\sin(5t + 0.25\pi) \text{ volt}$$

7. (c)

We consider the four meshes and the mesh currents as shown in figure



By KVL for the meshes, we get

$$18i_1 - 12i_4 = 0$$

$$i_4 = \frac{3}{2}i_1$$

$$-12i_1 + 12i_4 = 12$$

$$6i_1 = 12$$

$$i_1 = 2 \text{ A}$$

and $$i_4 = 3 \text{ A}$$

$$4i_2 = 16$$

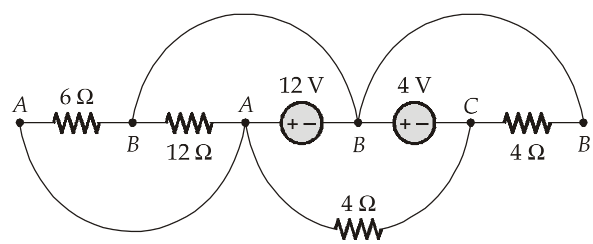
$$i_2 = 4 \text{ A}$$

Power delivered by the 4 V source

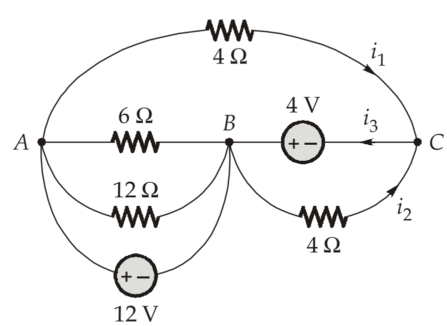
$$= 4 \times (i_2 + i_3)$$

$$= 4 \times 5 = 20 \text{ W}$$

Alternate Solution:



Redrawing the circuit, we get



Let, $$\text{node } C = \text{reference}$$

$$V_B = V_C + 4 \text{ V} = 0 + 4 = 4 \text{ V}$$

$$V_A = V_B + 12 \text{ V} = 4 + 12 = 16 \text{ V}$$

$$i_1 = \frac{V_B}{4} = 4 \text{ A}$$

$$i_2 = \frac{V_B}{4} = 1 \text{ A}$$

$$i_3 = i_1 + i_2 = 4 + 1 = 5 \text{ A}$$

$$P_{4\text{ V}} = 4 \times 5 \text{ A} = 20 \text{ W}$$

8. (b)

Z-parameters for lattice network can be given by,

$$Z_{11} = Z_{22} = \frac{4+2}{2} = 3\,\Omega$$

$$Z_{12} = Z_{21} = \frac{4-2}{2} = 1\,\Omega$$

$$\therefore \qquad [Z] = \begin{bmatrix} 3\,\Omega & 1\,\Omega \\ 1\,\Omega & 3\,\Omega \end{bmatrix} \Rightarrow \begin{matrix} V_1 = 3I_1 + I_2 \\ V_2 = I_1 + 3I_2 \end{matrix}$$

The transmission parameters are

$$V_1 = AV_2 - BI_2$$

$$I_1 = CV_2 - DI_2$$

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} = 3$$

$$B = -\left.\frac{V_1}{I_2}\right|_{V_2=0} = 8\,\Omega$$

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = 1\,\mho$$

$$D = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = 3$$

9. (c)

For a two port network to be symmetrical, in transmission parameter matrix, $\begin{bmatrix} A & B \\ C & D \end{bmatrix}$

$$A = D \qquad \text{...(i)}$$

For a two port network to be reciprocal, in transmission parameter matrix, $\begin{bmatrix} A & B \\ C & D \end{bmatrix}$

$$AD - BC = 1 \qquad \text{...(ii)}$$

$\therefore$ Option (c) will satisfy the above two conditions.

10. (b)

- The determinant of the incidence matrix of a closed loop is zero.
- The rank of the incidence matrix of a connected graph is $(n - 1)$.

11. (c)

$$Y_1 = \frac{1}{R_1 + jX_L} = \frac{R_1}{R_1^2 + X_L^2} - \frac{jX_L}{R_1^2 + X_L^2}$$

$$Y_1 = G_1 - jB_L \quad \text{...(i)}$$

$$Y_2 = \frac{1}{R_2 - jX_C} = \frac{R_2}{R_2^2 + X_C^2} + \frac{jX_C}{R_2^2 + X_C^2}$$

$$Y_2 = G_2 + jB_C \quad \text{...(ii)}$$

At resonance, $B_L = B_C$

$$\frac{X_L}{R_1^2 + X_L^2} = \frac{X_C}{R_2^2 + X_C^2}$$

$$\frac{5}{R_1^2 + 25} = \frac{4}{9+16} = \frac{4}{25}$$

$$125 = 4R_1^2 + 100$$

$$25 = 4R_1^2$$

$$R_1^2 = \frac{25}{4}$$

$$R_1 = \frac{5}{2}$$

$$R_1 = 2.5\ \Omega$$

12. (b)

Considering each options, we get,

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = \frac{Y_{22}}{\Delta Y} = \frac{4}{12-10} = \frac{4}{2} = 2\ \Omega$$

From h-parameters,

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = -\frac{1}{3}$$

From transmission parameters,

$$B = -\left.\frac{V_1}{I_2}\right|_{V_2=0} = -\frac{1}{10}\Omega$$

From Y-parameters,

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = 10\ \mho$$

13. (b)

By KCL at A,

$$\frac{V_{Th} - 12}{10} - 2i_0 + \frac{V_{Th}}{5} = 0 \quad \text{...(i)}$$

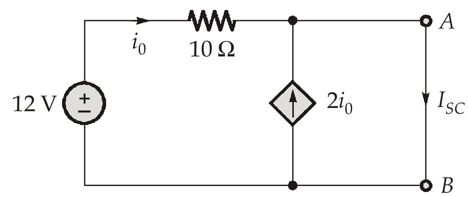
$$i_0 = \frac{12 - V_{Th}}{10} \quad \text{...(ii)}$$

By equation (ii) in (i),

$$\frac{3(V_{Th} - 12)}{10} + \frac{V_{Th}}{5} = 0$$

$$3V_{Th} - 36 + 2V_{Th} = 0$$

$$V_{Th} = \frac{36}{5} = 7.2 \text{ V}$$



When the terminals A and B are shorted, no current flows through the 5 Ω resistance

By KVL for the supermesh

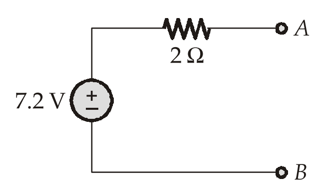
$$10i_0 = 12$$

$$i_0 = 1.2 \text{ A}$$

$$I_{SC} = 3i_0 = 3.6 \text{ A}$$

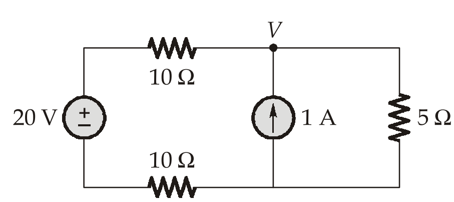
Thevenin impedance is given as

$$Z_{th} = \frac{V_{th}}{I_{SC}} = \frac{7.2}{3.6} = 2\Omega$$



14. (c)

By redrawing the above given circuit,



By writing nodal equation at 'V'

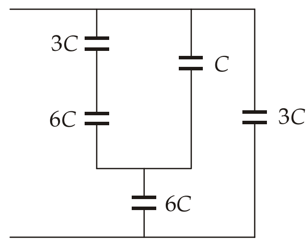
$$\frac{V - 20}{20} + \frac{V}{5} = 1$$

$$V = 8 \text{ V}$$

$$\therefore \quad P_{1D} = 8 \text{ W}$$

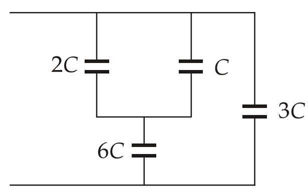
15. (b)

By reducing the given network,



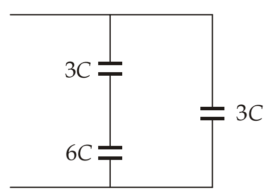
3C and 6C are in series. Hence,

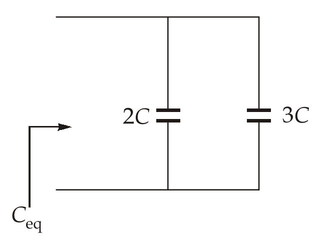
$$C' = \frac{3C \times 6C}{9C} = 2C$$



2C and C are in parallel. Hence, equivalent capacitance is

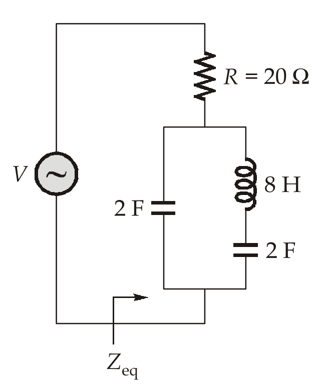
$$2C + C = 3C$$





$$C_{eq} = 2C + 3C = 5C$$

16. (b)



$$Z_{eq} = R + \frac{1}{j\omega C} \| \left(j\omega L + \frac{1}{j\omega C}\right)$$

$$= R + \frac{\frac{1}{j\omega C} \times \left(\frac{1-\omega^2 LC}{j\omega C}\right)}{\frac{1}{j\omega C} + \frac{1-\omega^2 LC}{j\omega C}} = R + \frac{\frac{1-\omega^2 LC}{j\omega C}}{2-\omega^2 LC}$$

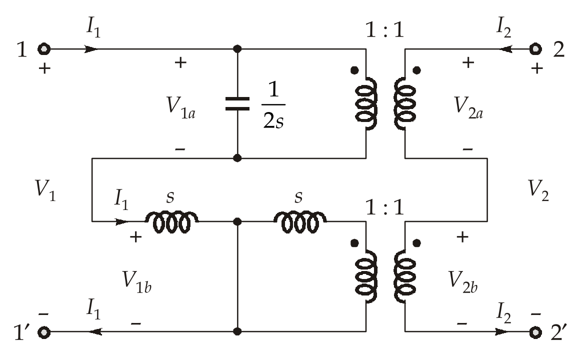
$$Z_{eq} = R - j\left[\frac{1-\omega^2 LC}{(2-\omega^2 LC)\omega C}\right]$$

For the given circuit to resonate, imaginary part of Z_{eq} should be zero,

$\therefore$ $$1 - \omega^2 LC = 0$$

$\therefore$ $$\omega = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{8 \times 2}} = \frac{1}{4} = 0.25 \text{ rad/sec}$$

17. (c)



For top portion of circuit :

Since transformer turns ratio is 1 : 1, the primary and secondary currents and voltages are equal in magnitude

$\therefore$ $$V_{1a} = V_{2a} = \frac{1}{2s}(I_1 + I_2)$$

For bottom portion of circuit,

$$V_{1b} = sI_1 + 0I_2$$

$$V_{2b} = 0I_1 + sI_2$$

Now, $$V_1 = V_{1a} + V_{1b} = \left(s + \frac{1}{2s}\right)I_1 + \frac{1}{2s}I_2$$

$$V_2 = V_{2a} + V_{2b} = \frac{1}{2s}I_1 + \left(s + \frac{1}{2s}\right)I_2$$

Hence, the z-parameters are given by comparing with the following equations

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

and $$V_2 = Z_{21}I_1 + Z_{22}I_2$$

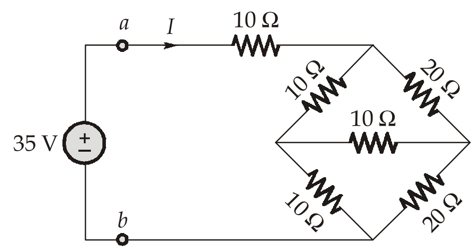
$\therefore$ $$Z_{11} = Z_{22} = s + \frac{1}{2s}$$

and $$Z_{12} = Z_{21} = \frac{1}{2s}$$

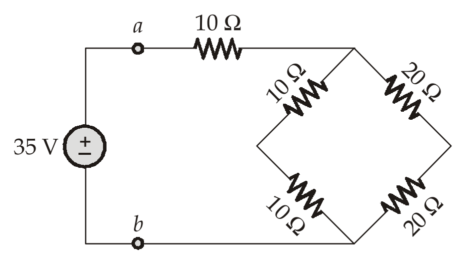
$\therefore$ The network is symmetrical and reciprocal.

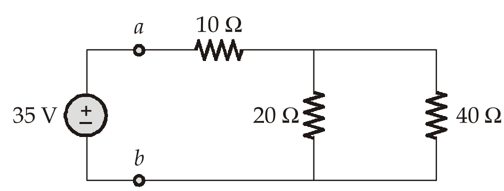
18. (a)

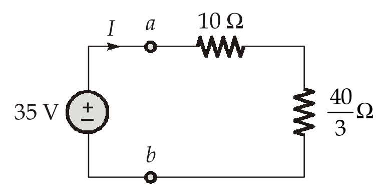
By redrawing the given network as,



Since in the above network, the bridge is balanced hence the circuit can be redrawn as below,







$$I = \frac{35}{10 + \frac{40}{3}} = \frac{35}{\frac{70}{3}} = \frac{3}{2} = 1.5 \text{ A}$$

19. (d)

$$y(t) = \begin{Bmatrix} 4 + 4; & 0 < t < \frac{T}{2} \\ 4 - 4; & \frac{T}{2} < t < T \end{Bmatrix}$$

$$y(t) = \begin{cases} 8; & 0 < t < \frac{T}{2} \\ 0; & \frac{T}{2} < t < T \end{cases}$$

Rms value of any periodic function

$$= \sqrt{\frac{1}{T}\int_0^T f^2(t)dt}$$

$$\therefore \quad y_{\text{rms}} = \sqrt{\frac{1}{T}\left[\int_0^{T/2}(8)^2 dt + \int_{T/2}^{T}(0)^2 dt\right]}$$

$$= \sqrt{\frac{1}{T}\times 64 \times \frac{T}{2}} = \sqrt{32} = 4\sqrt{2}\ \text{V}$$

20. (b)

We know, $$R = \rho\frac{l}{A}$$

as ρ is the property of the material. So it will be constant for same material,

$$\because \quad \text{Volume} = \text{Constant}$$

$$A \propto \frac{1}{l}$$

$$\frac{A_2}{A_1} = \frac{l_1}{l_2} = \frac{1}{2}$$

$$\frac{R_2}{R_1} = \frac{l_2}{l_1}\times\frac{A_1}{A_2} = \frac{2}{1}\times\frac{2}{1} = 4$$

$$R_2 = 4R_1$$

21. (b)

Maximum current for 100 Ω, 4 W

$$I = \sqrt{\frac{4}{100}} = \frac{2}{10} = 0.2\ \text{A}$$

Maximum current for 2 Ω, 2 W

$$I = \sqrt{\frac{2}{2}} = 1\ \text{A}$$

Maximum current for 1 Ω, 2 W

$$I = \sqrt{\frac{2}{1}} = \sqrt{2}\ \text{A}$$

The safe maximum value of current I which can flow through series resistance is 0.2 A.

22. (b)

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

and as R, L and C are halved

$$\therefore \quad Q' = \frac{1}{R/2}\sqrt{\frac{L/2}{C/2}} = \frac{2}{R}\sqrt{\frac{L}{C}}$$

$$Q' = 2Q$$

23. (b)

$$R = 200\ \Omega$$

$$X_L = \omega L = 100\ \Omega$$

$$X_C = \frac{1}{\omega C} = 100\,\Omega$$

$$Z = 200 + j(100 - 100)$$

$$|Z| = 200\ \Omega$$

$$I = \frac{V_{\text{rms}}}{Z} = \frac{\frac{200}{\sqrt{2}}}{200} = \frac{1}{\sqrt{2}}\text{A} = 0.707\text{ A}$$

24. (d)

All statements are correct.

25. (a)

The average power delivered to the reactive component of a load is zero.

26. (b)

A purely resistive load will have a unity power factor. A purely reactive load will have a zero power factor.

27. (b)

The quality factor is proportional to the maximum energy stored in a network divided by the total energy lost per period.

28. (c)

Inductors may be represented in the frequency domain by an impedance sL. If the initial current is non-zero, then the impedance must be placed in series with a voltage source $-Li(0^-)$ or in parallel with a current source $\frac{i(0^-)}{s}$.

29. (c)

Both statements are correct.

30. (d)

When two-two port networks are connected in cascade, the individual $ABCD$ parameters are multiplied,

$$\therefore \quad \begin{bmatrix} A & B \\ C & D \end{bmatrix} \times \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A^2 + BC & AB + BD \\ AC + CD & BC + D^2 \end{bmatrix}$$

31. (c)

For a network to be reciprocal

$$Z_{12} = Z_{21}$$
$$y_{12} = y_{21}$$
$$h_{12} = -h_{21}$$
$$AD - BC = 1$$

32. (c)

From transmission line parameters,

$$V_1 = AV_2 - BI_2 \quad \text{...(i)}$$
$$I_1 = CV_2 - DI_2 \quad \text{...(ii)}$$

From y-parameters

$$I_1 = y_{11}V_1 + y_{12}V_2 \quad \text{...(iii)}$$
$$I_2 = y_{21}V_1 + y_{22}V_2 \quad \text{...(iv)}$$

From above two equations, we have,

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2 = 0}$$

and $$y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1 = 0}$$

From equations (i) and (ii),

Keeping $V_1 = 0$,

$$AV_2 = BI_2$$

and $$I_1 = CV_2 - D\frac{A}{B}V_2$$

$$\therefore \quad y_{12} = -\left(\frac{AD - BC}{B}\right) = -\frac{\Delta T}{B}$$

and by keeping $V_2 = 0$, we have,

$$y_{21} = -\frac{1}{B}$$

33. (d)

As the voltage distribution across C_1, C_2 and C_3 is in the ratio 2 : 3 : 4, and the applied voltage is 135 V,

The voltages are 30 V, 45 V and 60 V respectively across C_1, C_2 and C_3

Capacitance = Charge divided by the potential difference.

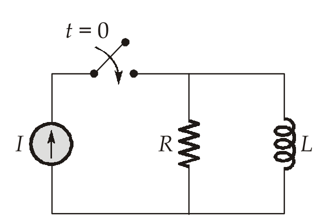
Hence
$$C_1 = \frac{4500}{30} = 150\ \mu F$$
$$C_2 = \frac{4500}{45} = 100\ \mu F$$
$$C_3 = \frac{4500}{60} = 75\ \mu F$$

If C is the resultant capacitance of the series combination,
$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

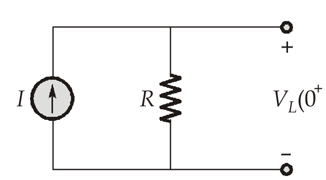
Solving, $C = 33.3\ \mu F$

Alternate Solution:
$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$
$$\frac{1}{C_{eq}} = \frac{V_1}{Q} + \frac{V_2}{Q} + \frac{V_3}{Q} = \frac{V_1 + V_2 + V_3}{Q}$$
$$C_{eq} = \frac{4500\,\mu C}{135} = 33.33\ \mu F$$

34. (b)



$t = 0^-$, the current through inductor is 0 A, i.e.,
$$i_L(0^-) = 0\text{ A}$$
$t = 0^+$, Inductor acts as a O.C.
$$i_L(0^+) = 0\text{ A},$$
$$V_L(0^+) = IR$$



$t \to \infty$, inductor acts as a short circuit and current 'I' flows through it and voltage across it is '0 V'
$$i_L(\infty) = I$$
$$v_L(\infty) = 0\text{ V}$$

Energy stored in a inductor between time interval is $\frac{1}{2}LI^2$

$$\text{Expression for } v_L(t) = v_L(\infty) + (v_L(0^+) - v_L(\infty))e^{-t/\tau}$$

$$v_L(t) = IRe^{-(R/L)t}, t \geq 0$$

The voltage across the supply is $v_L(t)$

The energy supplied by the source is

$$W_s = \int_0^\infty v_L \cdot I\, dt = \int_0^\infty IRe^{(-R/L)t} \cdot I\, dt$$

$$W_s = I^2 L$$

The ratio of energy stored in a inductor to the energy supplied by the source is 0.5.

35. (c)

Let R be the value of one resistor,

$\therefore$ The power dissipated by combined resistor is,

$$P_1 = \frac{V^2}{4R} \qquad (\because R_{eq} = R + R + R + R = 4R)$$

$$\frac{V^2}{R} = 4 \times 25 = 100$$

When resistors are connected in parallel,

$$R_{eq} = \frac{1}{\frac{1}{R}+\frac{1}{R}+\frac{1}{R}+\frac{1}{R}} = \frac{R}{4}\,\Omega$$

$$P_2 = \frac{V^2}{R_{eq}} = \frac{V^2}{R} \times 4 = (100) \times 4 = 400 \text{ W}$$

37. (d)

For parallel RLC circuit,

$$Q = R\sqrt{\frac{C}{L}} = 1$$

$$\because \quad Q = \frac{1}{2\xi}$$

$$\xi = \frac{1}{2Q} = 0.5 \Rightarrow \text{underdamped}$$

38. (d)

For series RLC circuit at resonance.

Imaginary part of input impedance = 0

$$\therefore \quad Z_{min} = R$$

and hence,

$$I = \frac{V}{R} = I_{maximum}$$

39. (c)

The Kirchhoff's current law is based on the law of conservation of charge.

40. (c)

Elements should be also bilateral to satisfy the reciprocity.

Section B : Digital Electronics + Microprocessors

41. (b)

Flash type A/D converter requires comparator but no need of feedback circuit with D/A converter.

42. (b)

We know that,
$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$
$$= (1)\bar{Q}_n + \bar{Q}_n Q_n$$
$$Q_{n+1} = \bar{Q}$$
$\because$ $Q_0 = 0,$

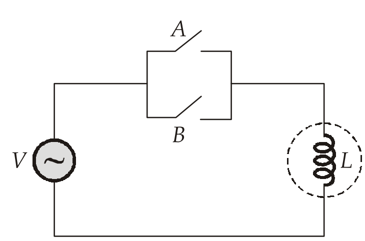
$\therefore$ $Q_1 = 1,$

$Q_2 = 0$

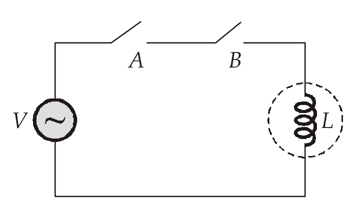
$Q_3 = 1....$

43. (d)

Consider the parallel switches as shown below,



The logic expression for parallel switch is obtained as
$$L = A + B$$
Again, we consider the series connected switches



The logic expression for series connected switches is
$$L = A \cdot B$$
Hence, the logic expression for given circuit is
$$L = A \cdot (B + C + D) \cdot (E + F)$$

44. (c)

For successive approximation converter, the conversion time is independent of V_A.

45. (c)

There are total 5 gates in the oscillator but the delay provided by 3 gates only,

$\therefore$ Hence, $N = 3$

$$\text{Total time period, } T = 2 \times N\, t_{pdg}$$
$$= 2 \times 3 \times 15 \times 10^{-9}$$
$$= 9 \times 10^{-8}$$

Fundamental frequency is, $f = \dfrac{1}{T} = \dfrac{10^8}{9}\text{sec} = 11.11 \text{ MHz}$

46. (b)

- Sequential circuits are dependent on cycles and the state of the circuit is the combined state of all the memory elements.
- Race around condition only occurs in level-triggered flip-flops.

47. (d)

Writing the equation in expanded decimal form, we get

$$(3x + 5) + (x + 6) = 5x$$
$$4x + 11 = 5x$$
$$x = 11$$

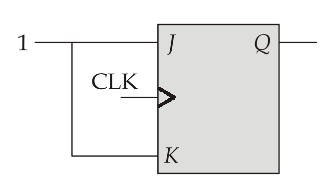
48. (d)

For a digital shaft encoding, the maximum change in the two alternate position is unity, thus grey code is most suitable for digital shaft coding.

49. (d)

Dual slope A/D converter has the highest accuracy among the given converts.

50. (a)



$\because$ $J = K = 1$

The flip-flop will behaves as a T-flip flop

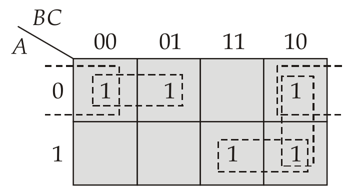
Thus, the output frequency, $Q = \dfrac{f_{clk}}{2} = \dfrac{5 \times 10^6}{2} = 2.5 \text{ MHz}$

51. (d)

- The grey code is used in transmission of digital signal as it reduces occurrence of error.
- The cyclic property of grey code makes it useful for angle measurement.
- It is generally used with position disk as a position indicator.

52. (b)

Using K-map:



Hence, essential prime implicant are $\overline{A}\,\overline{B}$ and AB.

53. (c)

For the given SIPO register,

Clock pulses	Output
Initial	1 1 1 1
1	0 1 1 1
2	0 0 1 1
3	0 0 0 1
4	1 0 0 0
5	1 1 0 0
6	1 1 1 0
7	1 1 1 1

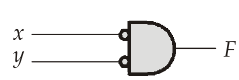
54. (b)

$$F = \overline{\overline{x+\overline{y}}+x}$$

$$= \overline{\overline{x+\overline{y}}}\cdot\overline{x}$$

$$= (x+\overline{y})\cdot(\overline{x})$$

$$F = \overline{x}\,\overline{y}$$



55. (c)

For flash type A/D converter,

$$\text{Number of comparator} = 2^n - 1$$

$$= 2^4 - 1 = 15$$

56. (d)

For weighted resistor type DAC

$$\text{LSB resistor} = 2^{n-1}\ (\text{MSB resistor})$$
$$100\text{ K} = 2^{4-1}\ (\text{MSB resistor})$$
$$\text{MSB resistor} = 12.5\text{ k}\Omega$$

57. (b)

$$\text{Figure of merit (FOM)} = \text{Propogation delay} \times \text{Power dissipation}$$
$$\text{FOM} = 50 \times 10^{-3} \times 15 \times 10^{-9}$$
$$= 750 \times 10^{-12}\text{ J}$$
$$= 750\text{ PJ}$$

58. (c)

From the given diagram,

CLK	J_2	K_2	J_1	K_1	Q_2	Q_1
					0	0 ← Initially
1	1	1	0	1	1	0
2	1	1	1	0	0	1
3	0	0	0	1	0	0

59. (b)

8086 has 20 address lines so it can address

$$= 2^{20}\text{ memory locations}$$
$$= 2^{10} \times 2^{10}$$
$$= 1\text{ K} \times 1\text{ K}$$
$$= 1\text{ M memory location}$$

So, total memory it can address is 1 M byte.

8086 → has 13 → 16 bit registers

8086 has 9 flags as CF , PF, AF, ZF, SF, IF, IF, DF, OF.

60. (b)

LXI SP, 7FFFH

MVI A, 25 H

XRI 02 H

$\Rightarrow$ $$A = 25\text{ H} = 00100101$$

$$A = \left.\begin{matrix} 25\text{ H} = 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 02\text{ H} = 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{matrix}\right\}\text{EXOR}$$
$$\begin{matrix} 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \end{matrix} \quad \Rightarrow A = 27\text{ H}$$

$$\text{PSW} = A\ F$$

F =	S	Z	X	AC	X	P	X	CY	
∴ PSW =	0	0	0	0	0	1	0	0	= 04

∴ PSW = AF = 2704 H

PUSH PSW

7FFDH	04
7FFEH	27
7FFFH	

∴ Content of location 7FFD is 04H,

61. (c)

8086 uses 20 lines for address bus. All other statements are correct.

62. (d)

LXI H, 3500 H	:	Store 3500 H in HL pair
LXI D, 0100 H	:	Store 0100 H in DE pair
DAD D	:	DE + HL → HL
		So, HL pair contain 3600 H
XCHG	:	Exchange content HL pair and DE pair, thus HL pair will contain 0100 H and DE pair will contain 3600 H.

63. (b)

AC ⇒ Auxiliary carry flags status is used only in DAA {DAS}.

All conditional jumps are short jumps. Z = 1 if data is same when compared.

64. (c)

CALL address has 18 T-states. This require maximum T-states for execution among the given instructions.

65. (b)

$$EC = IC - FC$$

$$\therefore \quad IC = EC + FC$$

Instruction cycle is combination of fetch cycle and execution cycle.

66. (a)

Only port C can be used in BSR mode i.e., bit set reset in mode 0, as input or output mode, in mode 1 and mode 2 for control signals.

67. (d)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0		= A800 H
to	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= (AFFF) H

$\underbrace{A_{15} \ldots A_{11}}_{\text{Fix}}$

$\because$ $(\overline{CS})$ = 0 for chip select

68. (c)

S	Z	X	AC	X	P	X	CY

S - Sign flag $\rightarrow$ represent MSB of result

P - Parity flag $\rightarrow$ If no. of 1's in result is even then it is set i.e. result has even parity

P = 1 $\rightarrow$ Even parity

S = 1 $\rightarrow$ So MSB of result is 1

69. (b)

$\because$ Time taken to execute each T-state

$$= \frac{1}{f_{clk}} = \frac{1}{2.5 \times 10^6}$$

$\therefore$ Time taken to execute 6 T-states

$$= \frac{6}{2.5 \times 10^6} = 2.4\ \mu s$$

70. (b)

Data in accumulator 00H

EX-OR 0 0 0 0 0 0 0 0 $\rightarrow$ (0 0) H

0 0 0 0 1 1 1 1 $\rightarrow$ (0 F) H

0 0 0 0 1 1 1 1 $\rightarrow$ Store in accumulator

i.e. only lower nibble of accumulator is complemented.

71. (b)

$$f_{\text{crystal}} = 6 \text{ MHz}$$

$$f_{\text{cross-over}} = \frac{f_{\text{crystal}}}{2} = 3 \text{ MHz}$$

72. (d)

ALU performs only arithmetic and logical operations. So 1 and 2 are correct.

73. (c)

A Master-Slave flip-flop stores only 1-bit of information.

74. **(c)**

- Demultiplexer can be used as decoder by interchanging select lines with input.
- Demultiplexer is implemented using combination of AND gate and NOT gate.

75. **(d)**

In masked ROM process, bit pattern is permanently recorded by the masking and metallization process.

❍❍❍❍