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ESE 2023 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 6

Section A : Electronic Devices & Circuits + Analog Circuits

Section B : Control Systems-1 + Microprocessors and Microcontroller-1

Section C : Network Theory-2 + Digital Circuits-2

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2.	(a)	17.	(b)	32.	(b)	47.	(d)	62.	(d)
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4.	(d)	19.	(b)	34.	(a)	49.	(b)	64.	(d)
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DETAILED EXPLANATIONS
Section A : Electronic Devices & Circuits + Analog Circuits

1. (c)

We know that,

the charge carrier density, $n = \dfrac{1}{R_H \times e}$

Given, $I = 50$ A; $t = 0.33$ mm; $B = 1.3$ T

but $n = \dfrac{BI}{V_H t \times e} \quad \because \quad R_H = \dfrac{V_H \times t}{BI}$

$$= \frac{1.3 \times 50}{(9.6 \times 10^{-6})(0.33 \times 10^{-3})(1.6 \times 10^{-19})}$$

$\therefore$ $n = 1.28 \times 10^{29}/\text{m}^3$

2. (a)

There is significant recombination taking place in the transition region. However, most of the carriers pass through the transition region without recombination.

3. (c)

When the temperature is maintained at a certain constant value, the generation of minority carriers is constant. In reverse bias condition, the drift current due to the flow of minority carriers is called the reverse saturation current and is independent of the value of applied bias voltage.

4. (d)

Once the pinch-off occurs, the current I_D saturates at a particular level and the device acts as a constant current source. Hence, beyond pinch-off, the differential channel resistance becomes very high.

5. (b)

The channel thickness is inversely related to the square root of the doping concentration of the channel. This is because the depletion width,

$$W \propto \frac{1}{\sqrt{\text{Doping}}}$$

6. (d)

We know that,

The fermi factor, $f(E) = \dfrac{1}{\left(1 + e^{\frac{E-E_F}{kT}}\right)} = 0.90$

$$e^{\frac{E-E_f}{kT}} = \frac{1}{0.90} - 1 = 0.11$$

$$\frac{E - E_F}{kT} = \ln(0.11)$$

$$E = E_F + kT \ln(0.11)$$

$$= 7.06 + \frac{T}{11,600} \times \ln(0.11)$$

$$= 7.06 + \frac{1000}{11,600} \ln(0.11)$$

$$= 7.06 + \frac{1000}{11,600}(-2.207)$$

$$= 7.06 - 0.19$$

$$E = 6.87 \text{ eV}$$

7. (b)

Given, $V_{GS} = 1.8$ V

$\frac{W}{L} = 4$

$\mu_n C_{ox} = 70 \times 10^{-6}$ A/V^2

$\lambda = 0.09$ V^{-1}

$V_T = 0.3$ V

For a MOSFET in saturation region, the current is given by

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

the transconductance, $g_d = \frac{\partial I_D}{V_{DS}}$

$$g_d = \frac{\partial}{\partial V_{DS}}\left[\frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 (1 + \lambda V_{DS})\right]$$

$$g_d = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 \lambda$$

$$g_d = \frac{1}{2} \times 70 \times 10^{-6} \times 4 \times (1.8 - 0.3)^2 (0.09)$$

$$g_d = 28.35 \ \mu\text{S}$$

8. (c)

The depletion width, $W = \sqrt{\frac{2 \in}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_j}$

where, $V_j = V_{bi} + V_{RB}$

$\therefore \quad \downarrow W \propto \frac{1}{\sqrt{\text{doping concentration} \uparrow}}$

9. (b)

We know that,

diffusion capacitance, $C_D = \frac{\in A}{W}$

where, $W = \dfrac{1}{\sqrt{\text{Doping}}}$

Therefore, $C_D' = \dfrac{\in \times 2A}{W'} = \dfrac{\in \times 2A}{\frac{W}{\sqrt{4}}}$

$$C_D' = 2 \times \frac{\in A}{W} \times 2$$

$$C_D' = 4\, C_D$$

10. (a)

$$I_C = \beta I_B + (\beta + 1) I_{CBO} = \beta I_B + I_{CEO}$$

now, $\beta + 1 = \dfrac{I_{CEO}}{I_{CBO}} = \dfrac{0.6 \times 10^{-3}}{3 \times 10^{-6}} = 200$

$\therefore$ $\beta = 199$

$\therefore$ $I_C = 199(10\ \mu A) + 0.6\ mA = (1.99 + 0.6)\ mA$

$= 2.59\ mA$

11. (b)

Given, $V_{TN} = 1\ V$

$\mu_n C_{ox} = 0.75\ mA/V^2$

$I_D = 1.5\ mA \quad \text{for} \quad V_{GS} = 5\ V$

In saturation region, $I_D = \dfrac{1}{2}\mu_n C_{ox} \dfrac{W}{L}(V_{GS} - V_T)^2$

$$1.5 \times 10^{-3} = \frac{1}{2} \times 0.75 \times 10^{-3} \frac{W}{L}(4)^2$$

$\therefore$ $\dfrac{W}{L} = \dfrac{1}{4}$

13. (b)

Thermal equilibrium minority concentration,

$$p_0 = \frac{n_i^2}{n} = \frac{n_i^2}{N_D} = \frac{10^{20}}{10^{16}} = 10^4\ \text{cm}^{-3}$$

Excess minority concentration due to light illumination,

$G_L \tau_p = 10^{10} \times 10^{-6} = 10^4\ \text{cm}^{-3}$

Steady state minority concentration $= p_0 + G_L \tau_p = 2 \times 10^4\ \text{cm}^{-3}$

14. (b)

When LED becomes OFF, the current flowing through the photodiode will decrease to reverse saturation current and it works as a normal diode.

15. (c)

Photodiode is always operated in reverse bias and when light is off, current flowing through it is reverse saturation current and it works as a normal diode.

16. (d)

For n-type semiconductor,

$$\tau_n = \frac{n}{p}\tau_p = \frac{n}{\frac{n_i^2}{n}}\tau_p = \left(\frac{n}{n_i}\right)^2 \tau_p \qquad \text{(by mass action law, } np = n_i^2\text{)}$$

$$\therefore \quad \tau_n = \left(\frac{n}{n_i}\right)^2 \tau_p$$

17. (b)

Current density, $J = nqv = \rho v$

where, ρ is charge density and v is velocity of carrier

$$\therefore \quad J = 80\times10^{-3}\ \text{C/m}^3 \times 5\times10^{2}\ \text{m/s} \qquad (\because 1\ \text{cm} = 10^{-2}\ \text{m})$$

$$J = 40\ \text{A/m}^2$$

18. (c)

The concentration of holes in valence band is given as

$$p = N_v \exp\left\{\frac{-(E_F - E_V)}{kT}\right\}$$

For p to be greater than N_V, $E_F < E_V$.

19. (b)

Thermal runaway refers to self destruction or self damage of BJT because of overheating which occurs due to increase in I_C with respect to I_{CO}.

20. (d)

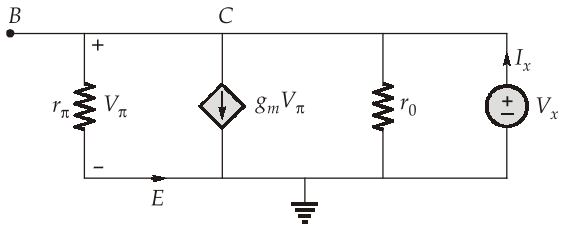
$\Rightarrow$ Basic current mirror can be used as active load in an amplifier.
As $A_V \propto R_L'$
Hence, it can be used to increase voltage gain of amplifier.

$\Rightarrow$ Widlar current mirror is used when smaller current (in μA) is required. It is a slight modification in Basic current mirror with emitter resistance R_E in Q_2 transistor.

$\Rightarrow$ In a BJT current mirror, transistors are in active region whereas in MOSFET current mirror, transistors are in saturation region.

21. (d)

Small signal model



As B and C are connected,

$$\therefore \quad V_x = V_\pi$$

and output resistance between C and E is

$$R_0 = \frac{V_x}{I_x}$$

Applying KCL at collector

$$g_m V_\pi + \frac{V_x}{r_0} + \frac{V_\pi}{r_\pi} = I_x$$

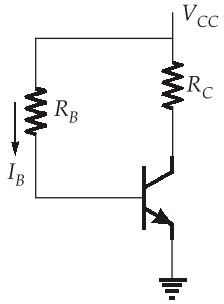
$$V_x\left[g_m + \frac{1}{r_0} + \frac{1}{r_\pi}\right] = I_x$$

$$\frac{V_x}{I_x} = R_0 = \frac{1}{\frac{1}{r_0} + \frac{1}{r_\pi} + g_m}$$

$$R_0 = \frac{1}{g_m} \| r_\pi \| r_0$$

22. (d)

Fixed bias circuit, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$



As V_{CC}, V_{BE}, R_B all are constant values. Hence, I_B is also constant. Therefore, the circuit is named as fixed bias circuit.

For fixed bias circuit, $S = 1 + \beta$

For collector to base bias circuit, $S = \dfrac{1+\beta}{1+\beta R_C/(R_B + R_C)}$

For self bias circuit, $S = \dfrac{1+\beta}{1+\beta R_E/(R_{Th} + R_E)}$

The Self-bias circuit has the least stability factor. It can be used to bias BJT for any configuration.

23. (b)

$$A_V = -126$$

$$\text{Input capacitance } C_{in} = C_\pi + C_\mu(1 - A_V)$$
$$= 100 + 3[1 + 126] = 100 + 127 \times 3$$
$$= 481 \text{ pF}$$

$$\text{Output capacitance } C_{out} = C_\mu$$
$$= 3 \text{ pF}$$

24. (a)

$$V_{DS} = 2.5 \text{ V}$$
$$V_{GS} = 1 \text{ V}$$
$$V_{TN} = 0.25 \text{ V}$$
$$\therefore \quad V_{DS} > V_{GS} - V_T$$

Hence transistor is in saturation.

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2 = \frac{1.2}{2}(1 - 0.25)^2 = \frac{1.2}{2} \times \frac{3}{4} \times \frac{3}{4}$$
$$I_D = 0.3375 \text{ mA}$$

25. (d)

MOSFETs must be operated in saturation region when used as amplifier.

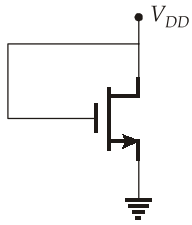
N-channel MOSFET is in saturation when

$$V_{DS} \geq (V_{GS} - V_T)$$
$$V_{DS} \geq V_{GS}$$
$$V_D \geq V_G$$

P-channel enhancement MOSFET is in saturation when

$$V_{DS} \leq (V_{GS} - |V_T|)$$
$$V_{DS} \leq V_{GS}$$
$$V_D < V_G$$

$\Rightarrow$ For a MOSFET with drain shorted to Gate,



$$V_{GS} = V_{DD}, \; V_{DS} = V_{DD}$$
$$V_{DS} > V_{GS} - V_T$$

Hence, transistor is in saturation region.

26. (b)

Type of feedback		R_i	R_0
Series Shunt	Voltage Series	Increases	Decreases
Shunt-Shunt	Voltage Shunt	Decreases	Decreases
Shunt-Series	Current Shunt	Decreases	Increases
Series-Series	Current Series	Increases	Increases

27. (d)

Resistance R and R_E constitute the feedback network. R is directly connected to input node, hence shunt mixing and not directly connected to output node, hence current sampling.

Hence, the feedback is current shunt feedback.

28. (d)

Using the virtual short concept, $V_- = V_+ = 0$ V

Applying KCL at input side

$$\frac{2-0}{1} = \frac{0-V_0}{4} + \frac{0-V_0}{4}$$

$$2 \times 4 = -2\,V_0$$

$$V_0 = -4 \text{ Volt}$$

Applying KCL at output side

$$\frac{V_0}{2} + \frac{V_0-0}{4} + \frac{V_0-0}{4} = I$$

$$\frac{-4}{2} + \frac{(-4)}{4} + \frac{(-4)}{4} = I$$

$$I = -2 - 1 - 1$$

$$I = -4 \text{ mA}$$

29. (a)

If $V_0 = +10$ V, D_1 is ON

$$\therefore \quad V_{UT} = \frac{V_0 \times 3}{1+3} = \frac{10 \times 3}{4} = 7.5 \text{ V}$$

If $V_0 = -10$ V, D_2 is ON

$$V_{LT} = \frac{V_0 \times 3}{3+2} = \frac{-10 \times 3}{5} = -6 \text{ V}$$

Hysteresis width $V_H = V_{UT} - V_{LT}$

$$= 7.5 - (-6)$$

$$V_H = 13.5 \text{ Volt}$$

30. (b)

When switch is at position 1, $R_F = 80$ kΩ, $R_1 = 5$ kΩ

$$A_{V1} = \frac{-R_f}{R_1} = \frac{-80}{5} = -16$$

When switch is at position 3, $R_F = 20$ kΩ, $R_1 = 5$ kΩ

$$A_{V3} = \frac{-R_F}{R_1} = \frac{-20}{5} = -4$$

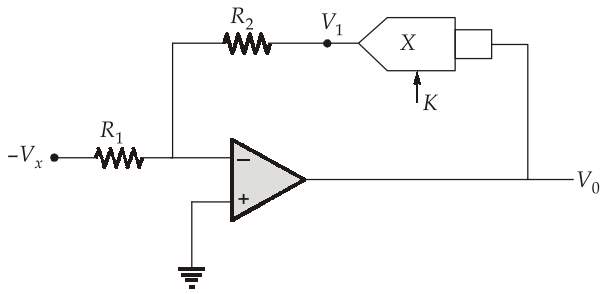
Hence, the difference = 12

31. (a)

For a high slew rate, the output voltage of op-amp can change quickly, thereby reducing the rise time and improving the transient response.

Amplifiers exhibit some non-linear behaviour that causes voltage gain to vary as the input voltage changes. Op-amp in negative feedback will be less sensitive and this will cause the op-amp to behave more linearly. Hence, statement 3 is incorrect.

32. (b)



For the analog multiplier, $V_1 = \dfrac{V_0^2}{K}$

KCL at input side,

$$\frac{-V_x - 0}{R_1} = \frac{0 - V_1}{R_2}$$

$$\frac{V_x}{R_1} = \frac{+V_0^2}{KR_2}$$

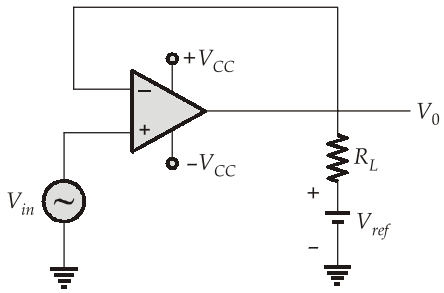
$$V_0^2 = \frac{+KR_2}{R_1} V_x$$

$$V_0 = \sqrt{\frac{KR_2}{R_1} V_x}$$

Hence the circuit is square root extractor.

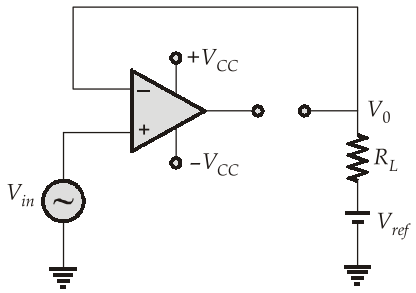
33. (b)

Case 1: For $V_{in} < V_{ref}$, Op amp o/p is –ve. Hence, diode is ON.



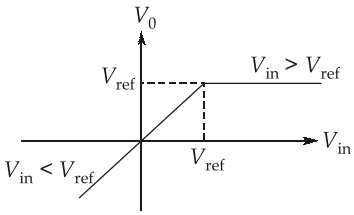
Therefore, $V_0 = V_{in}$

Case 2: For $V_{in} > V_{ref}$, Op amp o/p is +ve. Hence, diode is OFF.



Hence, virtual short can't be applied.

$\therefore \quad V_0 = V_{ref}$



34. (a)

For CLC filter,

$$\text{ripple factor } r = \frac{\sqrt{2}}{R_L}\frac{|X_C|^2}{|X_L|}$$

$$= \frac{\sqrt{2}}{2000} \times \frac{1}{(2\omega_0 C)^2} \times \frac{1}{2\omega_0 L}$$

$$= \frac{\sqrt{2}}{2000} \times \frac{10^{12}}{(2 \times 2\pi \times 50 \times 10)^2} \times \frac{1}{2 \times 2\pi \times 50 \times 0.318}$$

$$= \frac{\sqrt{2} \times 10^9}{2 \times 4 \times 10^7} \times \frac{1}{200}$$

$$r = 88.38 \times 10^{-3}$$

35. (d)

Darlington pair → Connection of common collector amplifiers

The cascode amplifier is a two-stage amplifier that consists of a common-emitter stage feeding into a common-base stage. Since, the current gain of common base amplifier is unity, hence the current gain of cascode amplifier is equivalent to that of single stage common emitter amplifier. Also, the common base amplifier has wide bandwidth, hence the cascode amplifier has high bandwidth.

37. (b)

In a BJT, the collector current,

$$I_C = I_S\left[e^{\frac{V_{BE}}{V_T}} - 1\right] \approx I_S \exp(V_{BE}/V_T),$$

where,

$$I_S = \frac{A_E q D_n n_i^2}{N_B W_B}$$

38. (a)

The drop against Schottky diode forces emitter base junction to never enter into saturation region, thus eliminating the saturation delay and reduces reverse recovery time, thereby increasing the switching speed.

Section B : Control Systems-1 + Microprocessors and Microcontroller-1

39. (b)

We have; $$T(s) = \frac{121}{s^2 + 13.2s + 121}$$

Compare with standard 2nd order system,

$$T(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

$$\omega_n = 11 \text{ rad/s}$$

$$2\xi\omega_n = 13.2$$

$$\xi\omega_n = 6.6$$

$$\text{Settling time } (\pm 5\% \text{ tolerance}) = \frac{3}{\xi\omega_n}$$

$$= \frac{3}{6.6} = 0.45 \text{ sec}$$

40. (d)

For ramp input to a type-1 system, $e_{ss} = \frac{A}{k_V}$; when input = $Ar(t)$

where; $$k_V = \lim_{s\to 0} s \cdot [G(s) \cdot H(s)] \neq 0$$

41. (c)

- Higher bandwidth leads to lower selectivity, and hence, higher noise.
- When the bandwidth is increased, then stability is increased and system becomes fast as it reduces rise time. A closed loop system has lower gain, hence higher bandwidth than open loop system leading to decrease in rise time. Hence, transient response decays more quickly in a closed loop system.
- Since, closed loop system is having a feedback so the control action depends on output.

42. (a)

Given system is type-1

$$k_V = \lim_{s\to 0} s \cdot G(s) = \lim_{s\to 0} s \cdot \frac{2(1 + 0.2s)}{s(0.2 + 5s)(1 + 2s)} = 10$$

Given input is 5 $r(t)$

$$\therefore \quad \text{Steady state error } (e_{ss}) = \frac{A}{k_V} = \frac{5}{10} = 0.5$$

43. (d)

R-H criterion is uses to obtain stability of closed loop system as well as open loop system.

44. (c)

Effect of addition of pole:

1. Operating range of 'K' decreases for system to be stable as with the addition of pole, root locus shift towards the imaginary axis making the system less stable.
2. Since each additional pole contributes an additional exponential term that must die out before the system reaches its final value, hence addition of pole increases the rise time of the system. Since, the bandwidth is inversely proportional to rise time, Bandwidth of system decreases.
3. Settling time increases.

45. (c)

Root locus is defined as a locus of closed loop poles obtained when system gain 'K' is varied from 0 to ∞. Complementary root locus is defined as locus of closed loop poles obtained when system gain 'K' is varied from $-\infty$ to 0.

46. (d)

Given, input, $r(t) = 10u(t)$

$$R(s) = \frac{10}{s} \quad \text{...Laplace domain}$$

Given, Output, $y(t) = \frac{t}{2}e^{-t}u(t)$

$$Y(s) = \frac{1}{2} \times \frac{1}{(s+1)^2} \quad \text{...Laplace domain}$$

Now, Transfer function $H(s) = \frac{Y(s)}{R(s)} = \frac{s}{20(s+1)^2} = \frac{0.05s}{s^2+2s+1}$

47. (d)

R-H table:

s^3	1	9
s^2	4	$-K-4$
s^1	$\frac{K+40}{4}$	
s^0	$-K-4$	

- For stable system, every element in 1st column must be of same sign.
- From s^1 row $\Rightarrow \frac{K+40}{4} > 0 \Rightarrow K > -40$
- From s^0 row $\Rightarrow -K-4 > 0 \Rightarrow K < -4$

For range $-40 < K < -4$, system will be stable.

48. (d)

- 8085 is an 8-bit microprocessor.
- 8085 does not have an instruction queue.

49. (b)

$$(55)_{10} = (37)_H$$

ACI instruction adds the data with the accumulator content with carry.

i.e.,

$$\begin{array}{r} 37\ H \\ 56\ H \\ +\ \ 1 \\ \hline 8E\ H \end{array}$$

50. (d)

- Instruction cycle → to fetch and execute a given instruction.
- Machine cycle → to perform an operation eg. memory or I/O access. 1 machine cycle is equivalent to 1 memory cycle and consists of 3 to 6 clock cycles.
- Clock cycle → 1 clock period or 1 T-state.

51. (c)

- Maskable interrupts are those which can be disabled or ignored by the microprocessor. Maskable interrupts are INTR, RST 7.5, RST 6.5 and RST 5.5.
- TRAP is a non-maskable interrupt.

52. (a)

If the service request bit is set, then the I/O port service routing is called.

53. (b)

RST 6

$$\text{Vector address} = 6 \times 8 = (48)_{10} = 30\ H$$

54. (d)

CMP R/M instruction compares the data byte in the register or memory with the contents of accumulator.

- If A is less than (R/M), the CY flag is set and Zero flag is reset.
- If A is equal to (R/M), the Zero flag is set and CY flag is reset.
- If A is greater than (R/M), the CY and Zero flag are reset.

55. (c)

- With addition of zero, root locus will shift towards left of s-plane. The system becomes more stable i.e. less oscillatory.
- Addition of zero, increases bandwidth and hence, rise time of system decreases.

Section C : Network Theory-2 + Digital Circuits-2

56. (b)

- A closed loop or a closed circuit may NOT contain all the nodes of the graph.
- The branches of the tree are represented as the tree branches or the twigs.
- The branches of the co-tree are represented as link or the chords.

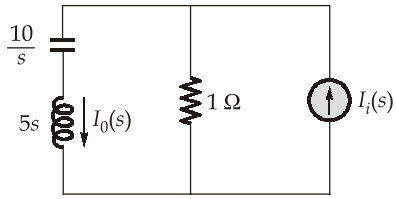
57. (c)

Number of fundamental cut-sets of graph is equal to

- Number of twigs $(n - 1)$.
- Number of KCL equations.
- Number of rows of the reduced incidence matrix.

58. (c)

Convert the given circuit in s-domain,



Apply current division rule;

$$I_0(s) = I_i(s) \times \frac{1}{1 + \frac{10}{s} + 5s}$$

$$\frac{I_0(s)}{I_i(s)} = \frac{s}{5s^2 + 10 + s}, \text{ where } s = j\omega$$

59. (d)

With L-C function, poles will lie on imaginary axis and hence, oscillatory response will be present.

60. (b)

- The order of reduced incidence matrix is $(n - 1) \times b$.
- This matrix can be utilised to find number of trees in a graph whether that graph is fully connected or NOT. The number of trees in a graph, $n = \det(AA^T)$

61. (b)

We have;

$$V_1 = \frac{4}{3}I_2 - \frac{1}{3}I_1$$

$$V_1 = \frac{-1}{3}I_1 + \frac{4}{3}I_2 \quad \text{...(i)}$$

$$V_2 = \frac{-1}{2}I_1 + \frac{1}{2}I_2 \quad \text{...(ii)}$$

From (i) and (ii)

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} -\frac{1}{3} & \frac{4}{3} \\ -\frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$\therefore$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} -\frac{1}{3} & \frac{4}{3} \\ -\frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

Now, Y-parameter from Z-parameter

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \frac{1}{\Delta Z}\begin{bmatrix} Z_{22} & -Z_{12} \\ -Z_{21} & Z_{11} \end{bmatrix}$$

where; $\Delta Z = Z_{11} \cdot Z_{22} - Z_{12} \cdot Z_{21}$

$$= \frac{-1}{3} \times \frac{1}{2} + \frac{4}{3} \cdot \left(\frac{1}{2}\right) = \frac{1}{2}$$

$\therefore$ $$Y_{22} = \frac{Z_{11}}{\Delta Z} = \frac{-1/3}{1/2} = -\frac{2}{3}\text{ʊ}$$

62. (d)

The condition for two-port network to be symmetric are:

1. For Z-parameter $\Rightarrow$ $Z_{11} = Z_{22}$
2. For Y-parameter $\Rightarrow$ $Y_{11} = Y_{22}$
3. For h-parameter $\Rightarrow$ $h_{11}\, h_{22} - h_{12}\, h_{21} = 1$
4. For g-parameter $\Rightarrow$ $g_{11}\, g_{22} - g_{12}\, g_{21} = 1$
5. For $ABCD$-parameter $\Rightarrow$ $A = D$

63. (d)

h-parameters are defined as;

$$V_1 = h_{11}\, I_1 + h_{12}\, V_2$$
$$I_2 = h_{21}\, I_1 + h_{22}\, V_2$$
$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2 = 0}$$
$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0}$$

$\because$ h_{21} is current gain, hence dimensionless.

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0}$$
$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0}$$

$\because$ h_{12} is inverse voltage gain, hence dimensionless.

Note: Two quantity can be added or subtracted only when they have same unit OR both should be unitless.

64. (d)

We have $$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 2 & -2 \\ 0.5 & 9 \end{bmatrix}$$

To get $ABCD$ parameter from Z-parameter:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{1}{Z_{21}}\begin{bmatrix} Z_{11} & \Delta Z \\ 1 & Z_{22} \end{bmatrix} = \begin{bmatrix} 4 & 38 \\ 2 & 18 \end{bmatrix}$$

ABCD-parameters for cascaded connection:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{overall}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_1 \cdot \begin{bmatrix} A & B \\ C & D \end{bmatrix}_2$$

$$= \begin{bmatrix} 1 & 0 \\ 5 & 2 \end{bmatrix}\begin{bmatrix} 4 & 38 \\ 2 & 18 \end{bmatrix} = \begin{bmatrix} 4 & 38 \\ 24 & 226 \end{bmatrix}$$

$\therefore$ $B = 38\ \Omega$

65. (c)

Short circuit parameter is known as *Y*-parameter.

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

When two networks are in parallel connection, then overall *Y*-parameter can be obtained by adding individual *Y*-parameter of the two-port networks.

66. (a)

The output of a flip flop changes 'only once' in one clock cycle, either at positive edge or negative edge of the clock.

67. (c)

In a parallel counter, all flip-flops changes their states simultaneously i.e., they are all synchronised. The maximum frequency of operation of synchronous or parallel counter is,

$$f_{\max} = \frac{1}{t_{pdff} + t_{\text{gate}}}$$

where, t_{pdff} = propagation delay of one flip flop.

t_{gate} = Propagation delay of AND gate.

$$f_{\max} = \frac{1}{2.5+5} \times 1000\ \text{MHz}$$

$$= 133.33\ \text{MHz}$$

68. (b)

Given $R = 0.002$

$$R = \frac{1}{2^n - 1}$$

$$2^n - 1 = \frac{1}{0.002} \Rightarrow 2^n = 501$$

$$n \cong 9$$

69. (d)

Given: $V_{CC} = 6\ \text{V}, I_{CCH} = 2\ \text{mA}, I_{CCL} = 4\ \text{mA}$

Average current, $I_{CC(\text{avg})} = \frac{I_{CCH} + I_{CCL}}{2} = \frac{2+4}{2} = 3\ \text{mA}$

The average power dissipation,

$$P_D = V_{CC} \times I_{CC(avg)}$$
$$= 6 \times 3$$
$$P_D = 18 \text{ mW}$$

70. (a)

The process of converting an analog signal to a digital form requires four processes:

1. Sampling
2. Holding
3. Quantizing
4. Encoding

71. (d)

For n-bit sequence detector, Moore machine requires $(n + 1)$ states.

For n-bit sequence detector, Mealy machine requires 'n' states.

72. (b)

The output of the state diagram depends on the input also. So, it represents Mealy machine.

From state diagram,

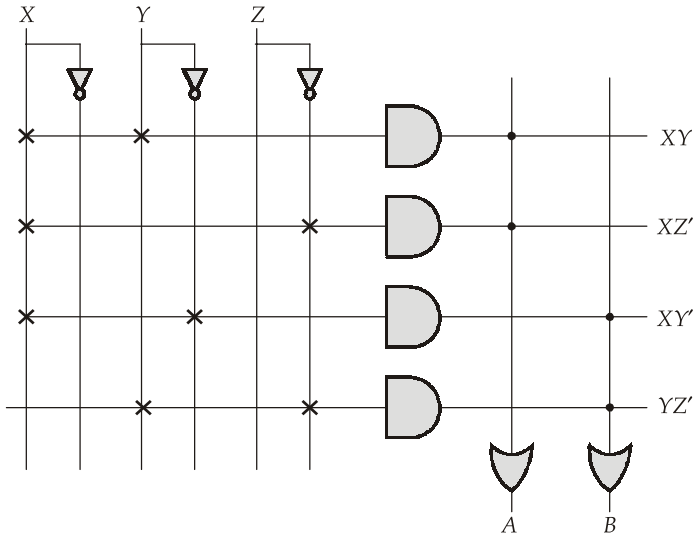
The sequence being detected is 0, 100 or 101.

73. (d)

Given functions $A = XY + XZ'$

$B = XY' + YZ'$

In PAL structure, AND gates are programmable and OR gates are fixed.



Hence, 4 AND gates and 2 OR gates are required.

74. (c)

Excitation table for S-R flip flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

So, $S = X, R = 0$

$Q_{n+1} = 1$

75. (a)

The fan out is sometimes called 'loading factor' because of the fact that the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded.

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