DETAILED SOLUTIONS

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ESE 2023 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 4

Section A : Control Systems + Microprocessors and Microcontroller

Section B : Network Theory-1

Section C : Digital Circuits-1

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DETAILED EXPLANATIONS
Section A : Control Systems + Microprocessors and Microcontroller

1. (a)

Steady state error is defined as the difference between the desired value and the actual value of a system output in the limit as time goes to infinity.

2. (b)

Given, open loop poles, $p = 5$

open loop zeros, $z = 1$

Asymptotes, $p - z = 5 - 1 = 4$

$$\text{Centroid, } \sigma = \frac{\Sigma \text{real part of open loop pole} - \Sigma \text{ real part of open loop zero}}{p - z}$$

$$\sigma = \frac{-4-4-5-6+3}{4} = -4$$

3. (c)

Given, steady state error for unit step input,

$$e_{ss} = \frac{1}{1+K_p} = 0.20$$

$$1 + K_p = 5 \quad \Rightarrow \quad K_p = 4$$

Now, an integrator is cascaded to system and with ramp input,

$$\therefore \quad \text{steady state error, } e_{ss} = \frac{1}{K_a}$$

Here, as unit integrator is used, hence,

$$K_a = K_p$$

$$\therefore \quad e_{ss} = \frac{1}{4} = 0.25$$

4. (b)

Forward path gain : $adbe$ ($\because$ we need $\frac{X_5}{X_1}$)

individual loop gains, $L_1 = bc$

$L_2 = ef$

Two non touching loop gains; $L' = bcef$

$$\therefore \quad \text{Transfer function, } \frac{X_5}{X_1} = \frac{abde}{1-(bc+ef)+bcef}$$

5. (d)

Controllability matrix, $Q_c = \begin{bmatrix} B & AB \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 1 & B \end{bmatrix}$

$$\therefore \quad |Q_c| = 0 \text{ for any value of } B.$$

6. (c)

$$\phi^{-1}(t) = \phi(-t), \text{ as } \phi(t) = e^{At}$$

7. (b)

For a pole at origin, the initial slope is –20 dB/dec

8. (b)

Given, $$G(s)H(s) = \frac{10e^{-Ls}}{s}$$

$$\omega_{pc} = 5 \text{ rad/sec}$$

We know that, at phase crossover frequency, the phase angle is equal to 180°. Hence,

$$-90° - \frac{180°}{\pi} L \cdot \omega_{pc} = -180°$$

$$\frac{-\pi}{2} - L \times 5 = -\pi$$

$$5L = \frac{\pi}{2}$$

$$\therefore \quad L = \frac{\pi}{10}$$

9. (a)

The characteristic equation of the given control system is,

$$q(s) = 1 + G(s)H(s) = 0$$

$$1 + (1 + sK_D)\left(\frac{16}{s(s+1.6)}\right) = 0$$

$$s^2 + 1.6s + 16s + 16sK_D = 0$$

$$s^2 + s(1.6 + 16K_D) + 16 = 0$$

On comparing with the characteristic equation of standard second order system,

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0$$

$$\therefore \quad 2\xi\omega_n = 1.6 + 16K_D$$

$$\omega_n^2 = 16 \quad \Rightarrow \quad \omega_n = 4$$

$$\therefore \quad 2 \times 0.5 \times 4 = 1.6 + 16K_D$$

$$4 - 1.6 = 16\,K_D$$

$$\therefore \quad K_D = \frac{2.4}{16} = 0.15$$

10. (b)

Given, $$h(t) = \frac{1}{6} e^{-0.8t} \sin(0.6t)$$

On comparing with standard notation,

i.e., $$K \frac{e^{-\xi\omega_n t}}{\sqrt{1-\xi^2}} \sin(\omega_d t + \phi)$$

We get, $\xi\omega_n = 0.8$ ...(i)

$$\omega_d = \omega_n\sqrt{1-\xi^2} = 0.6 \text{ rad/sec} \quad \text{...(ii)}$$

$\omega_n = 1$ rad/sec and $\xi = 0.8$

11. (b)

The closed loop transfer function,

$$\text{T.F} = \frac{36}{s^2+6s+36}$$

$2\xi\omega_n = 6;\ \omega_n = 6$ rad/sec

$\therefore \quad 2\xi \times 6 = 6 \Rightarrow \xi = 0.5$

$$t_p = \frac{\pi}{\omega_d} = \frac{\pi}{\omega_n\sqrt{1-\xi^2}} = \frac{\pi}{6\sqrt{1-\left(\frac{1}{2}\right)^2}} = 0.604 \text{ sec}$$

12. (c)

Since it is given that proportional error constant $K_p = 10$, hence it is a type 0 system. It provides infinite steady state error to ramp and parabolic input. Hence, the test signal used is a step input. The system may be stable or unstable.

Stable System: $G(s) = \frac{10}{s+1}$ (Steady state error valid.)

Unstable System: $G(s) = \frac{10}{(s-2)(s-4)}$ (Steady state error is not defined.)

13. (b)

Given, $G(s) = \frac{50K}{s(s+5)}$

For a type-1 system, the steady state error,

$$e_{ss} = \frac{1}{K_V}$$

where, $K_V = \lim_{s\to 0} s\,G(s) = \lim_{s\to 0} s \times \frac{50K}{s(s+5)}$

$K_V = 10K$

$\therefore$ For a unit ramp input, $e_{ss} = \frac{1}{10K} = 0.05$

$\therefore \quad K = \frac{1}{10\times 0.05} = 2$

14. (c)

The introduction of a time delay element decreases both phase margin and gain margin.

15. (d)

The characteristic equation,

$$1 + G(s) = 0$$

$$1 + \frac{4}{(s^2 + 2s + 2)(s + \beta)} = 0$$

$$(s^2 + 2s + 2)(s + \beta) + 4 = 0$$

$$s^3 + \beta s^2 + 2s^2 + 2\beta s + 2s + 2\beta + 4 = 0$$

$$s^3 + (2 + \beta)s^2 + (2\beta + 2)s + (2\beta + 4) = 0$$

For stability,

$$2(2 + \beta) \times (\beta + 1) > 2(\beta + 2)$$

$$(\beta + 1) > 1$$

or, $\beta > 0$

16. (c)

Characteristic equation,

$$1 + G(s)H(s) = 0$$

$$s(s + 2)(s + 4)(s + 32) + K(s + 10) = 0$$

For $s = -6$

$$-6(-4)(-2)(26) + K(4) = 0$$

or $K = 6 \times 2 \times 26 = 312$

17. (d)

The auxiliary equation provides the symmetrically located roots, hence it is always even in order.

18. (a)

The addition of open loop poles in the system pulls the root locus towards right and the system response become slow.

19. (d)

The asymptotes of the root locus intersect the real axis at the centroid (σ),

where, $$\sigma = \frac{\Sigma\text{Real part of the OL poles} - \Sigma\text{Real part of OL zeros}}{\text{Number of OL poles} - \text{Number of OL zeros}}$$

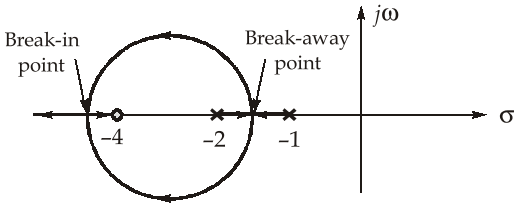
Here, OL zeros $= -1, -4$

and OL poles $= 0, \pm j\sqrt{2}$

$\therefore$ $$\sigma = \frac{0 - (-1 - 4)}{3 - 2} = 5$$

20. (a)

The approximate root locus plot is,



The break-away point is obtained by taking $\frac{dK}{ds} = 0$.

Here, $$K = \frac{-(s+1)(s+2)}{(s+4)} = -\frac{s^2+3s+2}{(s+4)}$$

$\therefore$ $$\frac{dK}{ds} = \frac{(s+4)(2s+3)-s^2-3s-2}{(s+4)^2} = 0$$

$$2s^2 + 8s + 3s + 12 - s^2 - 3s - 2 = 0$$

$$s^2 + 8s + 10 = 0$$

$$s = \frac{-8 \pm \sqrt{64-40}}{2} = \frac{-8 \pm \sqrt{24}}{2} = -4 \pm \sqrt{6}$$

$$s = -4 \pm 2.45 = -1.55, -6.45$$

So, the valid break-away point exists at $s = -1.55$.

21. (b)

Wait state is the name of the time delay in a CPU caused by differences between the speed of the CPU, the system bus, and memory circuits.

22. (c)

BHE stands for Bus High Enable. It is used to interface the odd addressed memory bank. *A*0 is used to select the even addressed memory bank.

23. (d)

MOV AL, 65

$$AL \leftarrow (65)_{10}$$

16	65	
16	4	1 ↑
	0	4

$\therefore$ $(65)_{10} = (41)_H$

$(41)_H = 0100\ 0001$

$\therefore$ The instruction stores 0100 0001 in AL

24. (c)

	LXI *B*,	0040 H	⇒	$C = (40)_H = (64)_{10}$ $B = (00)_H$
LOOP:	DCR	*C*	⇒	Decrement *C* by 1
	MOV	*A*, *B*	⇒	$A \leftarrow B$
	ORA	*C*	⇒	Logical OR of *C* and *A*
	JNZ	LOOP		

The result of ORA *C* will be zero when *C* is decreased to zero as *B* is already zero.

∴ The loop is executed 64 times.

25. (b)

$A \leftarrow 73$ H

$CY \leftarrow 1$

SBI 56 H

⇓

$A \leftarrow A - [56\text{ H}] - [CY]$

$A \leftarrow 73\text{H} - 56\text{H} - 01\text{H}$

A ⇒ 1C H

$$\left\{\begin{array}{r} 0111\ 0011 \\ -0101\ 0110 \\ \hline 0001\ 1101 \\ -1 \\ \hline 0001\ 1100 \\ \hline (1\text{C})\text{H} \end{array}\right\}$$

26. (c)

RAL and RLC operate on the contents of accumulator.

→ XTHL exchange stack top with HL register pair.

→ DAD H ⇒ HL ⇐ [HL] + [HL]

Hence DAD H result in doubling the HL register pair content.

27. (a)

Before the execution of SIM instruction,

A = 6D H

SIM instruction

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SOD	SDE	X	R7.5	MSE	M7.5	M6.5	M5.5
0	1	1	0	1	1	0	1

After the SIM instruction,

RST 5.5 is masked.

RST 7.5 is not reset.

29. (a)

→ 8051 microcontroller has on chip RAM of 128B.

→ 8051 microcontroller has on chip program space (ROM)

→ It has 32 I/O pins and 2 16-bit timers.

30. (a)

→ Directives are also called as pseudo instructions.
Exp: ORG, END

→ Directives give directions to the assembler not CPU. Instructions (such as MOV, ADD) are commands to the CPU.
Exp: ORG tells the assembler to place the opcode at memory location '0' while END indicates to the assembler the end of the source code.

31. (b)

				T-state
	MVI	B, n H	→	7
Back:	LDA	2000 H	→	13
	DCR	B	→	4
	JNZ	Back	→	7/10
	HLT		→	5

Total Execution Time = 200 μsec

f_{clk} = 2 MHz

$$\text{Total Execution Time} = [7 + (n-1)(13+4+10) + (13+4+7) + 5] \times \frac{1}{f_{CLK}}$$

$$200 \times 10^{-6} = \left(7 + (n-1)27 + 24 + 5\right) \times \frac{1}{2 \times 10^{6}}$$

$$400 = 36 + (n-1)27$$

$$364 = 27n - 27$$

$$27n = 391$$

$$n = 14.48 \cong 15 = (15)_{10}$$

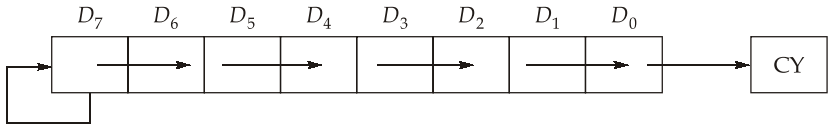
$$(n)_H = (0F)_{Hex}$$

32. (a)

In the 8051, the stack pointer (SP) points to the last used location of the stack. When data is pushed onto the stack, the stack pointer (SP) is incremented by 1.
It is different from 8085 and 8086 microprocessors wherein the stack pointer register is decremented by two on execution of PUSH instruction.

33. (b)

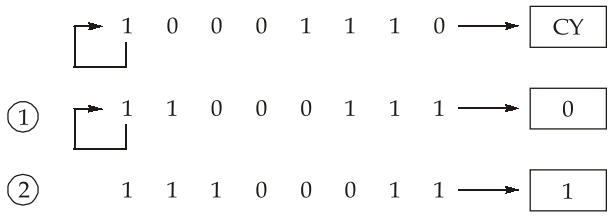
SAR → Shift right Arithmetically



Pictorial representation of SAR

Now
AL ← 8E H
AL ← 1000 1110
CL ← 02 H

It means shift right contents of AL register two times arithmetically.



∴ Contents of AL register = 1110 0011 = E3H
Contents of CY flag = 1

34. (c)
The physical address of the memory location where the address of the ISR is stored can be calculated by multiplying four to the type of interrupt and then converting it in hexadecimal.
The physical address of INT 0D H is

$$0D = 13 \times 4 = (52)_{10} = (34)H$$

Hence, memory address: 00034 H to 00037 H

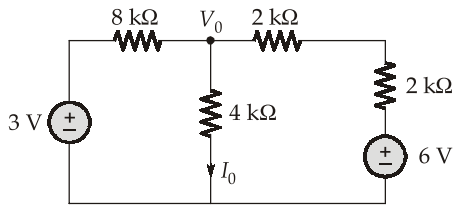
36. (d)
The modern control system theory is based on time domain approach (state-space approach).

37. (b)
Routh-Hurwitz criterion only tells about the number of roots lying in the left and right half of the s-plane but not their exact locations.

38. (d)
In BSR mode, I/O operations of port *A* and *B* are not affected by BSR control word.

Section B : Network Theory-1

39. (d)
Using source transformation



Apply nodal analysis at node V_0

$$\frac{V_0 - 3}{8K} + \frac{V_0}{4K} + \frac{V_0 - 6}{4K} = 0$$

$$V_0 + 2V_0 + 2V_0 = 3 + 2 \times 6$$

$$V_0 = 3 \text{ V}$$

$$I_0 = \frac{V_0}{4} = \frac{3}{4}\text{mA} = 750\ \mu\text{A}$$

40. (d)

At resonance, $Z_{min} = R$

$V_{min} = 49$ V for $I = 14$A

$$R = \frac{V_{min}}{I} = \frac{49}{14} = 3.5\ \Omega$$

The quality factor, $$Q = R\sqrt{\frac{C}{L}} = 3.5\sqrt{\frac{72}{2}}$$

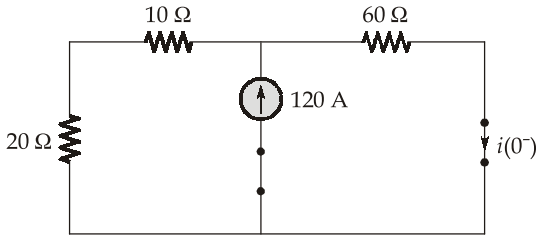
$$Q = 21$$

41. (a)

The power factor angle of the circuit at resonance is 0° and the power factor at resonance is unity.

42. (b)

At $t = 0^-$, the switch was closed and at steady state, inductor acts as short-circuit,



$$i(0^-) = \frac{30}{30+60} \times 120 = 40\ \text{A}$$

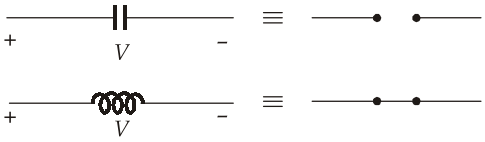
$$R_{eq} = 60 + 10 + 20 = 90\ \Omega$$

$$\tau = \frac{L}{R} = \frac{0.25}{90} = \frac{1}{360}$$

$$i(t) = i(0^-)e^{-t/\tau} = 40\, e^{-360t}\ \text{Amp}$$

43. (b)

In D.C. steady state, capacitor becomes open circuit, which means that there is a break in the circuit while the inductor becomes short circuit, which means they become a wire.



44. (d)

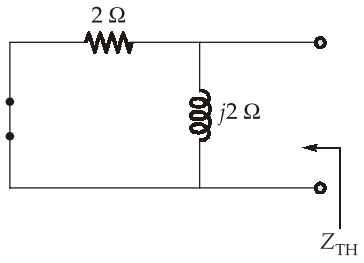
Here, R_L is a resistive load so, for maximum power transfer to R_L.

$$R_L = |Z_{TH}|$$

$$Z_{TH} = 2 \parallel (j2)$$

$$= \frac{2 \times j2}{2 + j2} = \frac{j2}{1 + j}$$

$$= \frac{j2(1-j)}{(1)^2 - (j)^2} = 1 + j\ \Omega$$



$$Z_{TH} = \sqrt{2}\angle 45^\circ\ \Omega$$

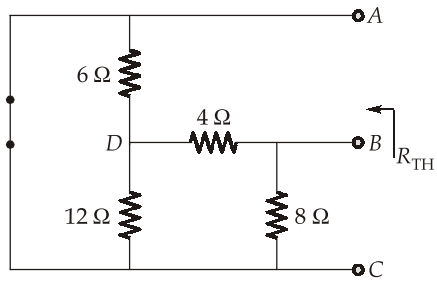
$$R_L = |Z_{TH}| = \sqrt{2}\ \Omega$$

45. (c)

- Reciprocity theorem is based on the symmetry of impedance or admittance matrix.
- Superposition theorem is also applicable for the circuit having initial conditions.

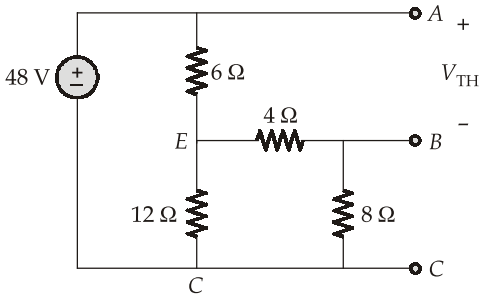
46. (d)

Calculation of thevenin resistance (R_{TH})



$$R_{TH} = 8 \parallel [4 + (12 \parallel 6)]$$
$$= 8 \parallel (4 + 4) = 8 \parallel 8$$
$$R_{TH} = 4\ \Omega$$

Calculation of thevenin voltage (V_{TH})



Equivalent resistance across terminal B-C

$$R_{BC} = 12 \parallel (8 + 4) = 6\ \Omega$$

Voltage across terminal E-C

$$V_{EC} = 24\ \text{V}$$

Voltage across 6 Ω resistance,

$$V_{6\Omega} = 24\ \text{V}$$

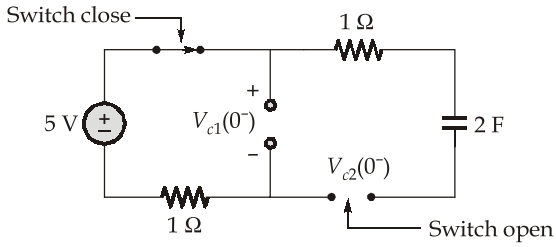
Now, voltage across 4 Ω resistance,

$$V_{4\Omega} = \frac{24 \times 4}{4 + 8} = 8\ \text{V}$$

Thevenin voltage, $V_{Th} = 24 + 8 = 32\ \text{V}$

47. (b)

At $t = 0^-$, at steady state capacitor acts as open circuit



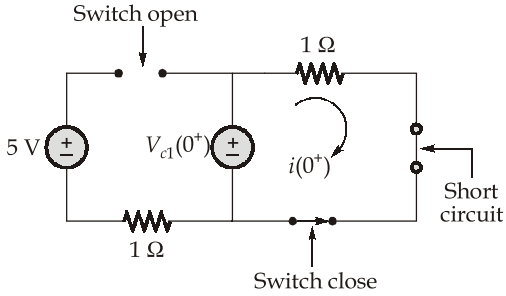
$$V_{c1}(0^-) = 5 \text{ V and } V_{c2}(0^-) = 0$$

$\because$ Voltage across capacitor do not change its magnitude or direction instantly.

$\therefore$ $$V_c(0^-) = V_c(0^+) = 5 \text{ V}$$

at $t = 0^+$

$$V_{c2}(0^-) = V_{c2}(0^+) = 0 \text{ V}$$



$$i(0^+) = \frac{V_{c1}(0^+)}{1} = \frac{5}{1} = 5 \text{ Amp}$$

48. (d)

Linear: "The element which obeys additivity and homogeneity property are linear". For linear element, V-I characteristics is a straight line passing through origin.

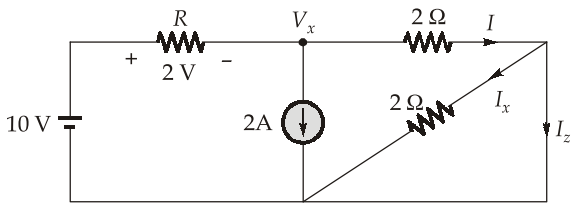
Bilateral: "The element's whose characteristics are same in both direction of current is known as bilateral element".

Passive: "If the ratio of voltage to current is positive over the characteristics, then it is passive element".

49. (d)

With D.C. source, inductor behaves as short circuit and capacitor behaves as open circuit at steady state.

$\therefore$ The simplified circuit can be



$$V_x = 8 \text{ V}$$

$$I = \frac{V_x}{2} = 4 \text{ Amp}$$

$$I = I_x + I_z = I_z \qquad \ldots[\because I_x = 0]$$

50. (c)

At high frequency, KVL and KCL is NOT applicable, there we use field theory.
Eg: Communication system, Transmission line

51. (b)

Current through capacitor:

$$I_C = C \cdot \frac{dV_c}{dt} \qquad \ldots V_c = \text{voltage across capacitor}$$

Voltage across Inductor:

$$V_L = L \cdot \frac{dI_L}{dt} \qquad \ldots I_L = \text{Current through inductor}$$

Now:
$$i_2(t) = i_1(t) - C_1 \cdot \frac{dV_X(t)}{dt}$$

$$V(t) = i_1(t) \cdot R_1 + L_1 \cdot \frac{di_1(t)}{dt} + V_X(t)$$

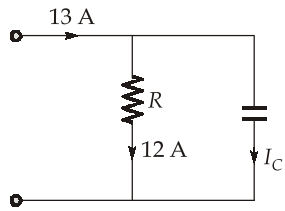
Hence, equations 2 and 3 are incorrect.

52. (b)

First take R-C network
$$13 = \sqrt{12^2 + I_C^2}$$

$$I_C = 5 \text{ Amp}$$

Now take complete R-L-C network,



$$I_R = 12 \text{ A}, I_C = 5 \text{ A}, I_T = 13 \text{ A}$$

$$I_T = \sqrt{I_R^2 + (I_L - I_C)^2}$$

$$(13)^2 = (12)^2 + (I_L - 5)^2$$

$$I_L = 10 \text{ Amp}$$

53. (b)

$$\text{active power } (P) = \frac{1}{2} V_m I_m \cos\phi$$

$$= \frac{1}{2}(50 \times 10 \times \cos 60°) + \frac{1}{2}(50 \times 8 \times \cos 60°)$$

$$= 225 \text{ watt}$$

$$\text{Reactive power } (Q) = \frac{1}{2} V_m I_m \sin\phi$$

$$= \frac{1}{2}(50 \times 10 \times \sin 60°) + \frac{1}{2}(50 \times 8 \times \sin 60°)$$

$$= 225\sqrt{3} \text{ VAR}$$

$$\therefore \quad \frac{P}{Q} = \frac{1}{\sqrt{3}}$$

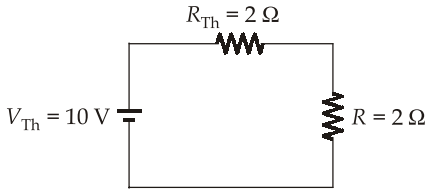
54. (a)

When $R = \infty$, $V = V_{Th} = V_{OC} = 10$ V

When $R = 0$, $I = I_N = I_{SC} = 5$ A

$$R_{Th} = \frac{V_{Th}}{I_N} = \frac{10}{5} = 2\ \Omega$$

Now thevenin's equivalent circuit will



$$I = \frac{V_{Th}}{R_{Th} + R} = \frac{10}{2+2} = \frac{10}{4} = 2.5\ \text{Amp}$$

Power absorbed will be $(P) = I^2 \times R$

$= (2.5)^2 \times 2$

$= 12.5$ watt

55. (d)

Reciprocity theorem is applicable to a network:

1. Containing R, L and C elements.
2. Should be initially relaxed system.
3. With only independent source present.

56. (c)

The equivalent resistance an ideal voltmeter is infinite such that no current passes through it.

Section C : Digital Circuits-1

57. (a)

Consensus theorem:

- Used to eliminate redundant term.
- A Boolean function contains 3 variables only.
- Each variable is used only 2-times.

Eg: $AB + \bar{A}C + BC = AB + \bar{A}C$

$(\bar{A} + B)(B + C)(A + C) = (\bar{A} + B)(A + C)$

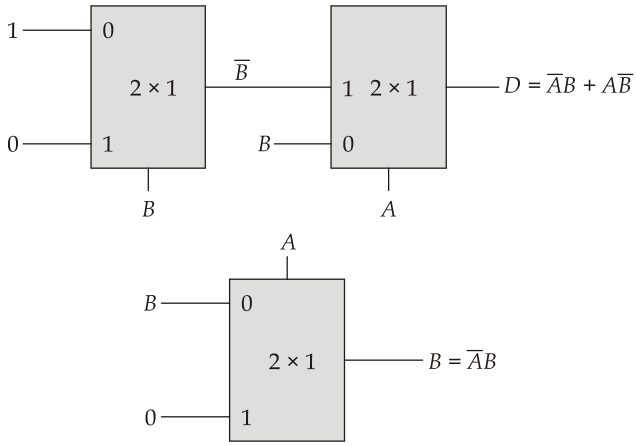
58. (d)

Half subtractor:

A	B	$D = A - B$	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D = Difference, B = Borrow

$$D = A \oplus B \text{ and } B = \overline{A}B$$



Hence, Total number of 2 : 1 MUX required to implement half subtractor is "3".

59. (d)

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	(5)	7	(6)
11	12	13	(15)	14
10	8	(9)	11	(10)

60. (d)

Truth table of a 2-input EX-OR gate

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Hence, the output is complement of second input if one input is logic '1'.

Truth table of 2-input EX-NOR gate

A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

So, the output of 2-input EXNOR gate will be complement of second input if one input is at logic '0'.

61. (b)

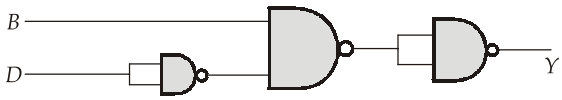
Let $$Y = \overline{\overline{\overline{(A+\bar{C})\cdot B\bar{D}}}\cdot\overline{(A+\bar{C})\cdot B\bar{D}}}$$

$$= \overline{\left(\overline{\overline{(A+\bar{C})}+\overline{B\bar{D}}}\right)\cdot\overline{(A+\bar{C})}+\overline{B\bar{D}}}$$

$$= \overline{(A+\bar{C}+\bar{B}+D)(\bar{A}C+\bar{B}+D)}$$

$$= \overline{(A+\bar{C})\bar{A}C+\bar{B}+D} = \overline{\bar{B}+D} = B\bar{D}$$

$$Y = \overline{\overline{B\bar{D}}}$$



62. (d)

The 2421 code of decimal number 0 is 0000

9's complement of a number is obtained by subracting every digit of a decimal number from 9. 9's complement of 0000 is 1111 = $(9)_{10}$.

63. (d)

A code is said to be reflective when the code for 9 is complement of the code for 0, 8 for 1, 7 for 2, 6 for 3 and 5 for 4.

Excess-3 code is a reflective code as well as sequential code.

64. (b)

Difference between PAL and PLA:

PAL	PLA
1. In PAL, OR array is fixed AND array is programmable.	In PAL, Both OR and AND array are programmable.
2. Speed of PAL is higher than PLA.	Speed is lower than PAL.
3. The complexity of PAL is less than PLA.	The complexity of PLA is high as compared to PAL.
4. It is less available.	It is more available.
5. It is not that expensive.	It is expensive.

65. (c)

$$Y(A, B) = \Sigma m(0, 3)$$

$$Y = \overline{A}\,\overline{B} + AB$$

	I_0	I_1
	A	$\overline{A}$
$\overline{B}$	2	(0)
B	(3)	1
	B	$\overline{B}$

Since the select line is active low, $I_0 = B$ and $I_1 = \overline{B}$

66. (a)

- Serial adder requires less components compared to parallel adder.
- BCD to 7-segment can be constructed by one 4 × 16 decoder circuit as it requires 4 inputs and 7 outputs.

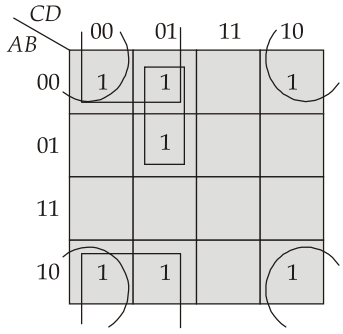
67. (d)

				Integer	Fraction
8	153	R	0.513 × 8	4	0.104
8	19	1	0.104 × 8	0	0.832
8	2	3	0.832 × 8	6	0.656
	0	2	0.656 × 8	5	0.248
			0.248 × 8	1	0.984
			0.984 × 8	7	0.872

$$(153.513)_{10} = (231.406517)_8$$

68. (c)

K-Map for the function F:



$$F = \overline{B}\,\overline{D} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}D$$

69. (b)

The number of self dual functions for n-variable = $(2)^{2^{n-1}} = 2^{(2^n/2)}$

For $n = 3$, No. of self dual functions = $2^{(2^3/2)} = 2^4 = 16$

70. (b)

We have, $$\frac{(19)_b + \left[\sqrt[3]{343}\right]_b}{(4)_b} = (13)_a$$

$$\frac{(b+9)+(7)}{4} = a + 3$$

$$b + 16 = 4a + 12$$

The above equation is valid for $a = 2$ and $b = 4$. Hence, $b = 2a$.

71. (c)

Excess-3 code is a 4-bit code.

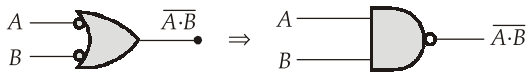
72. (b)

A	B	$A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

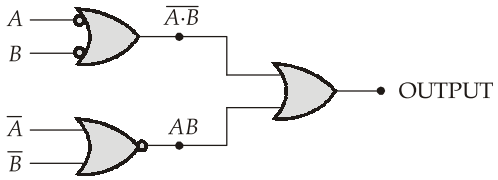
- Output is high, if both inputs are same.
- Output is low, if both inputs are different.

73. (b)

We know;



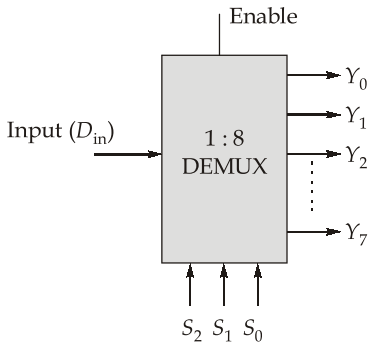
We have;



$\therefore$ Output $= \overline{A \cdot B} + A \cdot B$

$= 1$ ...[$\because X + \overline{X} = 1$]

74. (c)



75. (d)

Multiplexer can be used as a encoder.

❍❍❍❍