DETAILED SOLUTIONS

MADE EASY

India's Best Institute for IES, GATE & PSUs

Test Centres: Delhi, Hyderabad, Bhopal, Jaipur, Lucknow, Bhubaneswar, Pune, Kolkata, Patna

ESE 2023 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 2

Section A : Network Theory

Section B : Digital Circuits

1.	(c)	**16.**	(a)	**31.**	(d)	**46.**	(b)	**61.**	(d)
2.	(a)	**17.**	(c)	**32.**	(a)	**47.**	(b)	**62.**	(d)
3.	(b)	**18.**	(c)	**33.**	(a)	**48.**	(a)	**63.**	(d)
4.	(c)	**19.**	(b)	**34.**	(b)	**49.**	(c)	**64.**	(d)
5.	(b)	**20.**	(d)	**35.**	(c)	**50.**	(b)	**65.**	(d)
6.	(d)	**21.**	(c)	**36.**	(d)	**51.**	(b)	**66.**	(c)
7.	(b)	**22.**	(d)	**37.**	(c)	**52.**	(d)	**67.**	(d)
8.	(a)	**23.**	(a)	**38.**	(c)	**53.**	(c)	**68.**	(b)
9.	(b)	**24.**	(d)	**39.**	(b)	**54.**	(c)	**69.**	(c)
10.	(d)	**25.**	(b)	**40.**	(a)	**55.**	(c)	**70.**	(a)
11.	(c)	**26.**	(a)	**41.**	(b)	**56.**	(b)	**71.**	(a)
12.	(a)	**27.**	(b)	**42.**	(c)	**57.**	(a)	**72.**	(c)
13.	(a)	**28.**	(b)	**43.**	(b)	**58.**	(c)	**73.**	(d)
14.	(c)	**29.**	(b)	**44.**	(a)	**59.**	(d)	**74.**	(c)
15.	(b)	**30.**	(d)	**45.**	(c)	**60.**	(b)	**75.**	(c)

Detailed Explanation

1. (c)

We have, $I = 2$ A, $t = 10$ sec, V = 115 Volt

$$\text{Charge } (q) = I \times t$$
$$= 2 \times 10 = 20 \text{ Coulomb}$$

Since, $$\text{Energy } (E) = qV$$
$$= 20 \times 115 = 2300 \text{ J} = 2.3 \text{ kJ}$$

2. (a)

We have, $$i = 2\cos 60\pi t \text{ Amp}$$

and $$V = 5 + 10\int_0^t i \cdot dt$$

$\therefore$ $$V = 5 + 10\int_0^t 2\cos 60\pi t \cdot dt = 5 + \frac{20}{60\pi}(\sin 60\pi t)_0^t$$

$$V = 5 + \frac{1}{3\pi}\sin 60\pi t \text{ Volt}$$

At $t = 5.55$ ms, $$V = 5 + \frac{1}{3\pi}\sin 60\pi \times 5.55 \times 10^{-3}$$

$$= 5 + \frac{1}{3\pi}\sin\frac{\pi}{3} = 5 + \frac{1}{3\pi} \times \frac{\sqrt{3}}{2}$$

$$V = 5 + \frac{1}{2\sqrt{3}\pi}$$

$$V \approx 5 \text{ Volt}$$

At $t = 5.55 \text{ ms} \cong \frac{1}{180}$, $$i = 2\cos 60\pi t = 2\cos 60\pi \times \frac{1}{180} = 2\cos\frac{\pi}{3} = 1 \text{ Amp}$$

$\therefore$ Power at $t = 5.55$ ms, $$P = v \cdot i = 5 \times 1 \approx 5 \text{ Watt}$$

3. (b)

- Power in kWh $= \frac{600 \times 4}{1000} = 2.4$ kWh
- Electricity rate $= \frac{\text{Amount}}{\text{Power in kWh}}$

$$10 = \frac{\text{Amount}}{2.4}$$
$$\text{Amount} = 24 \text{ cents}$$

$\therefore$ Total 24 cents are wasted.

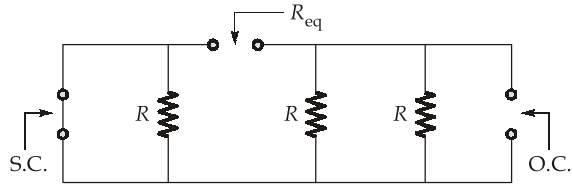
4. (c)

CONCEPT:

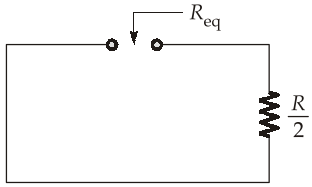
To obtain time constant:

- Replace inductor and capacitor with open circuit across which equivalent resistance is to be calculated.
- Replace independent voltage source with short circuit.
- Replace independent current source with open circuit.

Now after applying above concept,



Since, resistor across short circuit act as redundant element.



$$R_{eq} = \frac{R}{2}$$

$$\therefore \quad \text{Time constant } (\tau) = \frac{L_{eq}}{R_{eq}} = \frac{L}{R/2} = \frac{2L}{R}$$

Note: For '*RC*' network time constant can be obtained as

$$\tau = R_{eq} \cdot C_{eq}$$

where, R_{eq} = Equivalent resistance across capacitor and C_{eq} = Total capacitance.

5. (b)

Conductance: "It is the ability of an element to conduct electric current."

6. (d)

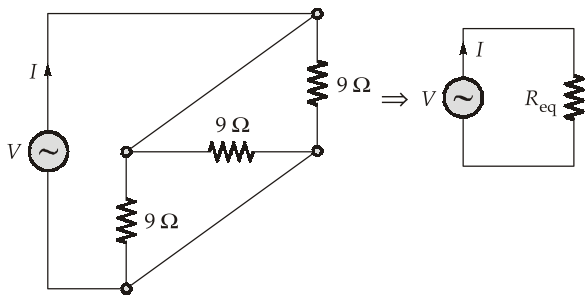
We have, $V = 6\cos 0.5 \times 10^6 t$ and $\omega = 0.5 \times 10^6$ rad/s

$L = 1$ mH $\Rightarrow X_L = \omega L = 0.5 \times 10^6 \times 10^{-3} = 0.5 \times 10^3\ \Omega$

$$C = 4 \text{ nF} \quad \Rightarrow X_C = \frac{1}{\omega C} = \frac{1}{0.5\times10^6 \times 4\times10^{-9}} = 0.5\times10^3\ \Omega$$

$$\therefore \quad X_C = X_L$$

Equivalent circuit will be,



$$R_{eq} = 9\,\Omega \| 9\,\Omega \| 9\,\Omega = 3\,\Omega$$

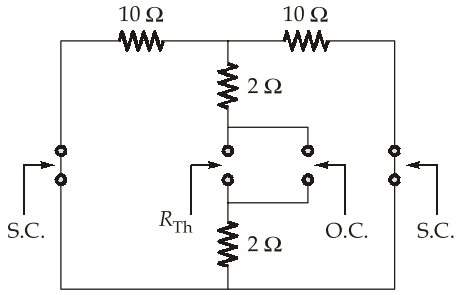
$$\therefore \quad I = \frac{V}{R_{eq}} = \frac{6\cos 0.5\times 10^6 t}{3} = 2\cos 0.5\times 10^6 t\ \text{A}$$

7. (b)

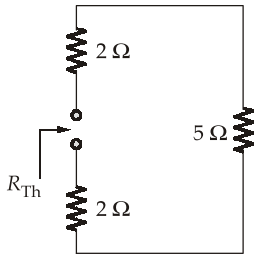
Calculation of Thevenin's Resistance:

- Replace independent voltage source with short circuit.
- Replace independent current source with open circuit.
- Remove load resistor across which Thevenin's resistance is to be calculated.

Now, equivalent circuit



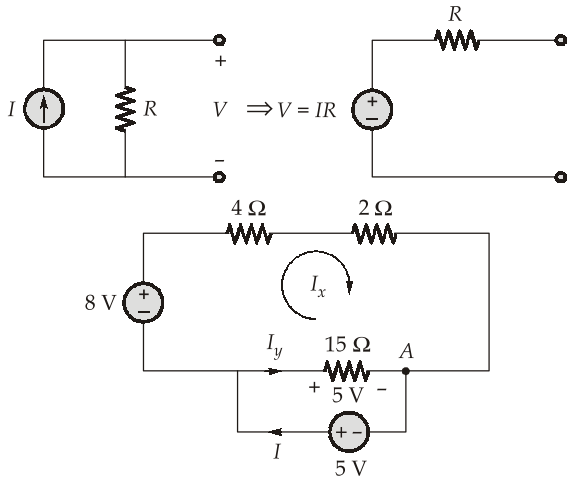
- 10 Ω is in parallel with 10 Ω.



$$\Rightarrow \quad R_{Th} = 5 + 2 + 2 = 9\,\Omega$$

8. (a)

From the source transformation theorem,



$$I_x = \frac{8+5}{6} = \frac{13}{6}\text{ A}$$

$$I_y = \frac{5}{15} = \frac{1}{3}\text{ A}$$

KCL at node A: $I_x + I_y = I$

$$\frac{13}{6} + \frac{1}{3} = I$$

$$I = \frac{13+2}{6} = \frac{15}{6} = \frac{5}{2} = 2.5\text{ Amp}$$

9. (b)

Mathematically, KCL implies that

$$\sum_{n=1}^{N} i_n = 0$$

It is based on law of conservation of charge.

10. (d)

We have, $f = 50$ Hz,

$$V_{\text{rms}} = \frac{V_m}{\sqrt{2}} \Rightarrow V_m = 100\text{ Volt}$$

$$V(t) = V_m \sin(2\pi f t) = 100\sin(314t)\text{ Volt}$$

11. (c)

We have, $V = -2\sin(314t + 10°) = 2\cos(314t + 10° + 90°)$

$V = 2\cos(314t + 100°)$ Volt

$V = 2\angle 100°$ Volt

Now, $I = 5\cos(314t + 160°) = 5\angle 160°$ Amp

Here ; $\theta = \theta_V - \theta_I = 100 - 160° = -60°$

Power factor $\Rightarrow$ $\cos\theta = \cos(-60°) = 0.5$(leading)

Note: Leading because current is leading with voltage.

12. (a)

The total number of possible trees,

$$T = \left| A \cdot A^T \right|$$

$$[A] = \begin{bmatrix} 1 & 1 & 0 & 0 & 1 \\ -1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & -1 & 0 \end{bmatrix}$$

$$[A^T] = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 0 & -1 \\ 1 & 0 & 0 \end{bmatrix}$$

$$[A \cdot A^T] = \begin{bmatrix} 1 & 1 & 0 & 0 & 1 \\ -1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & -1 & 0 \end{bmatrix} \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 0 & -1 \\ 1 & 0 & 0 \end{bmatrix}$$

$$[A \cdot A^T] = \begin{bmatrix} 3 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 3 \end{bmatrix}$$

$$\left|A \cdot A^T\right| = 3(6-1) + 1(-3-1) - 1(1+2) = 15 - 4 - 3$$
$$= 8$$

13. (a)

Transmission parameter is $ABCD$ parameter given as:

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2$$

14. (c)

Symmetric conditions for 2-port parameters:

- $Z_{11} = Z_{22}$
- $Y_{11} = Y_{22}$
- $h_{11}\, h_{22} - h_{12}\, h_{21} = 1$
- $g_{11}\, g_{22} - g_{12}\, g_{21} = 1$
- $A = D$

Reciprocal conditions for 2-port parameters:

- $Z_{12} = Z_{21}$
- $Y_{12} = Y_{21}$
- $h_{12} = -h_{21}$
- $g_{12} = -g_{21}$
- $AD - BC = 1$

15. (b)

In a complete graph, each pair of graph vertices is connected by an edge. Hence, the number of edges in complete graph is ${}^nC_2$.

16. (a)

Current through capacitor:

$$I_C = C \cdot \frac{dV}{dt}$$
$$1 = C \cdot \left(\frac{1}{2}\right)$$
$$C = 2\ \text{F}$$

17. (c)

- For a linear element, *VI* characteristics is a straight line passing through origin. Hence, the element is not linear.
- Since the *VI* characteristics depend on the direction of current flow, hence the element is not bidirectional.
- Since V/I = positive in both the quadrants, hence the element is Passive.

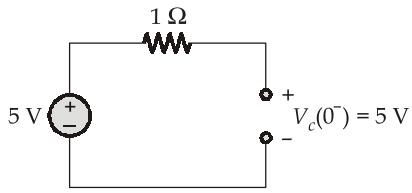
18. (c)

Tellegen's theorem:

- It is applicable to any network (i.e. linear, non-linear, unidirectional, time variant, time invariant).
- It is based on law of conservation of energy.

19. (b)

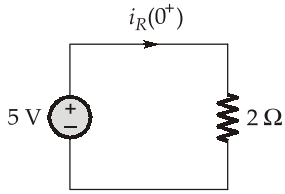
At $t = 0^-$ (switch is present at A) and capacitor acts as open-circuit.



$\because$ $V_c(0^-) = V_c(0^+) = 5$ V

"Capacitor do not allow sudden change in voltage".

At $t = 0^+$;



$$i_R(0^+) = \frac{5}{2} = 2.5 \text{ Amp}$$

20. (d)

In series combination, $P = I^2R \Rightarrow P \propto R$

$V = IR \Rightarrow V \propto R$

$\therefore$ $V \propto P$

Now, $$V_1 = V \cdot \frac{P_1}{P_1 + P_2}$$

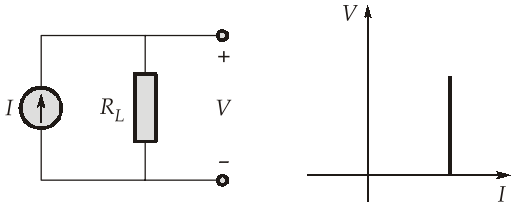
Here, $V = 12$ V, $P_1 = 15$ W and $P_2 = 10$ W.

$\therefore$ $$V_1 = 12 \times \frac{15}{15+10} = 7.2 \text{ V}$$

$$V_2 = 12 \times \frac{10}{15+10} = 4.8 \text{ V}$$

21. (c)

For ideal current source, internal resistance is infinite and the output current is constant irrespective of the load.



22. (d)

$$\text{Crest factor or peak factor} = \frac{V_{peak}}{V_{rms}}$$

$$\text{Form factor} = \frac{V_{rms}}{V_{avg}}$$

23. (a)

We have, $I_1 = 2\cos 10t$ A and $I_2 = 10\sin 10t$ A

Since I_1 and I_2 is in quadrature.

So, time constant of branch will be equal.

i.e. $$\frac{L}{R_1} = R_2 C$$

$$R_1 = \frac{L}{R_2 C} = \frac{12}{5\times 3} = 0.8\,\Omega$$

24. (d)

Series Resonance:

- Impedance is minimum $\Rightarrow Z = R$.
- Bandwidth $= \frac{R}{L}$ (rad/s).
- It perform voltage magnification as the magnitude of voltage across the inductor and the capacitor is equal to Q times the input sinusoidal voltage V.
- It act as bandpass filter.

25. (b)

We know, for parallel L-R-C circuit

$$\text{Bandwidth } (\omega) = \frac{1}{RC}$$

$\because$ $$R_2 = 2R = 2\ \Omega$$

$$C_2 = 2C = 2\ \text{F}$$

$$\text{Bandwidth } (\omega') = \frac{1}{R_2 C_2} = \frac{1}{4}$$

$\Rightarrow$ $$\omega' = \frac{\omega}{4}$$

26. (a)

When all the nodes are connected to each other and there is no repeated path existing between any two node then;

Total number of tress possible = N^{N-2}

N = Number of nodes = 4

Total number of tress possible = $4^{4-2} = 16$

27. (b)

- For parallel *R-L-C* resonance circuit

$$B_L = \frac{1}{X_L} = \frac{1}{\omega \cdot L}$$

$$B_C = \frac{1}{X_C} = \omega C$$

- At low frequency $\Rightarrow B_L > B_C$ (Inductive).
- At high frequency $\Rightarrow B_C > B_L$ (Capacitive).

28. (b)

We know, $\text{Quality factor } (Q) = \dfrac{\text{Resonant frequency } (\omega_o)}{\text{Bandwidth}}$

Here, $\text{Resonance frequency } (\omega_o) = \sqrt{\omega_1 \cdot \omega_2} = 2\omega_1$

$\text{Bandwidth (B.W.)} = \omega_2 - \omega_1 = 3\omega_1$

$\therefore \quad Q = \dfrac{2\omega_1}{3\omega_1} = \dfrac{2}{3}$

29. (b)

For parallel connection;

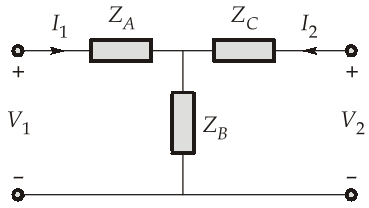
$$\text{Input admittance } (Y) = G + \frac{1}{sL}$$

where, $G = \dfrac{1}{R} = \dfrac{1}{3} S$

$$Y = \frac{1}{3} + \frac{1}{2s} = \frac{2s+3}{6s}$$

30. (d)

We know,



$$\Rightarrow \quad \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_A + Z_B & Z_B \\ Z_B & Z_B + Z_C \end{bmatrix}$$

For network-A:

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 2 & 2 \\ 2 & 3 \end{bmatrix}$$

For network-B:

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 3 & 2 \\ 2 & 3 \end{bmatrix}$$

- If networks are connected in series, then equivalent z-parameter is obtained by addition.

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}_{\text{equivalent}} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}_A + \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}_B$$

$$= \begin{bmatrix} 2 & 2 \\ 2 & 3 \end{bmatrix} + \begin{bmatrix} 3 & 2 \\ 2 & 3 \end{bmatrix} = \begin{bmatrix} 5 & 4 \\ 4 & 6 \end{bmatrix}$$

31. (d)

For R-L-C series circuit:

$$\text{Quality factor } (Q) = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{2}\sqrt{\frac{10^{-4}}{10^{-4}}} = \frac{1}{2}$$

$$\text{Damping ratio } (\xi) = \frac{1}{2Q} = 1$$

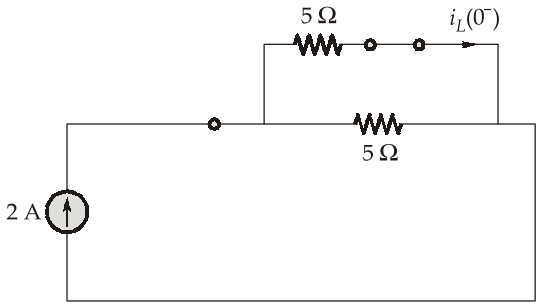
If $\xi = 1$, then system is critically damped.

Note:

- For $0 < \xi < 1 \Rightarrow$ system is underdamped.
- For $\xi > 1 \Rightarrow$ system is overdamped.
- For $\xi = 0 \Rightarrow$ system is undamped.

32. (a)

At $t = 0^-$ (switch is at position A), and at steady state inductor acts as short-circuit.

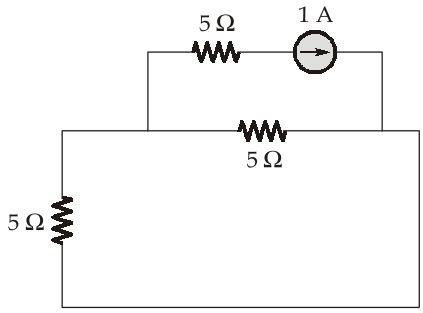


$$i_L(0^-) = 1 \text{ A}$$

$\because$ Inductor do not allow sudden change in current value and direction.

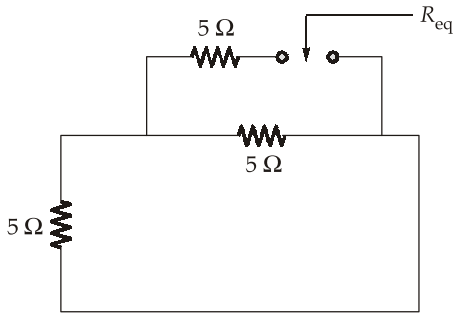
$\therefore$ $$i_L(0^-) = i_L(0^+) = 1 \text{ A}$$

At $t = 0^+$ (switch is at position B), the circuit can be drawn as below:



Obtain time constant:

- Replace inductor with open circuit.
- Operate the switch for $t > 0$.
- Deactivate independent source.



$$R_{eq} = 5 + [5 \| 5] = 7.5\ \Omega$$

$$\text{Time constant } (\tau) = \frac{L}{R_{eq}} = \frac{2.5}{7.5} = \frac{1}{3}$$

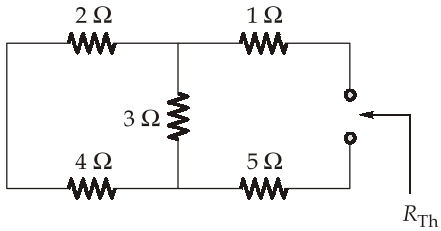
$\therefore$ Current flowing through inductor:

$$i(t) = i_L(0^+) \times e^{-t/\tau} = e^{-3t} \text{ Amp}$$

33. (a)

To get Thevenin's resistance across load:

- Deactivate independent sources.
- Replace load resistance with open circuit.



$$R_{Th} = \left[(2+4) \| 3\right] + [1+5] = 8\ \Omega$$

- For maximum power to transfer at load;

$$R_L = R_{Th}$$

$\therefore$ $$R_L = 8\ \Omega$$

34. (b)

Hybrid parameters are defined as:

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$
$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0} \Rightarrow \text{Reverse voltage gain}$$
$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0} \Rightarrow \text{Forward current gain}$$

35. (c)

In dual concept:

- $R \longleftrightarrow G$
- $L \longleftrightarrow C$
- Series $\longleftrightarrow$ Parallel
- Nodal $\longleftrightarrow$ Mesh

36. (d)

- Mesh analysis works only with planar circuit.
- Mesh analysis works with KVL which is based on law of conservation of energy.

37. (c)

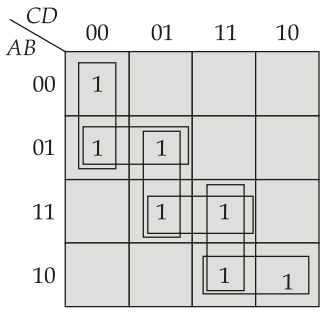
$$\text{Quality factor } (Q) = 2\pi\left[\frac{\text{Maximum energy stored in circuit}}{\text{Power dissipation per cycle}}\right]$$
$$Q \propto \frac{1}{\text{Power loss } (I^2R)}$$

38. (c)

The given logic function can be written as,

$$f(A, B, C, D) = \Sigma m(0, 4, 5, 10, 11, 13, 15)$$

Using *K*-map:



Total prime implicants = 6 ($AC'D'$, $A'BC'$, $BC'D$, ABD, ACD and $AB'C$)

Number of essential prime implicants = 2 ($A'C'D'$ and $AB'C$)

39. (b)

Given, $f_1(A, B, C) = \Sigma m(2, 3, 4)$

$f_2(A, B, C) = \pi M(0, 1, 5, 6, 7) = \Sigma m(2, 3, 4)$

For f_{out} to be zero, the function f_3 should be equal to,

$f_3(A, B, C) = \Sigma m(2, 3, 4)$

$\therefore$ The maximum number of possible minterms = 3.

40. (a)

From the given number, the minimum value of 'x' can be written as, "12 + 1 = 13" ($\because$ $C = 12$)

Therefore, the least decimal equivalent

$= 10 \times 13^2 + 11 \times 13^1 + 12 \times 13^0$

$= 1690 + 143 + 12 = (1845)_{10}$

42. (c)

Since, given that, $V_{out} = 0.2$ V for 00001

$\therefore$ the weight of LSB is 0.2 V.

The the weight of other bits in weighted D/A converter can be obtained as 0.4 V, 0.8 V, 1.6 V and 3.2 V respectively.

For a digital input of 11111, the value of output, $V_{out} = 3.2 + 1.6 + 0.8 + 0.4 + 0.2 = 6.2$ V.

43. (b)

Given, decimal number is $(417)_{10}$

8	417	
8	52	1
	6	4

$\therefore$ $(417)_{10} = (641)_8$.

44. (a)

TTL logic family has leakage current in the HIGH state and has assymmetric output drive; they can sink much more current in the low state than they can source in the high state.

45. (c)

DCTL, I^2L, HTL, TTL are saturating type logic families wherein the transistors are driven into saturation.

Schottky TTL, ECL are non saturated logic families wherein the transistors are not driven into saturation.

46. (b)

Output of 2 × 1 MUX, $Y = \bar{S} I_0 + S I_1$

where, $S = \bar{Q}; I_0 = \bar{X}; I_1 = X$

$\therefore$ $Y = \bar{\bar{Q}} \bar{X} + \bar{Q} X$

$Y = Q\bar{X} + \bar{Q}X$

Since, $Q_{n+1} = D = Y = Q\bar{X} + \bar{Q}X$
which is the characteristic equation of T flip-flop.

47. (b)

Let output of 4 × 1 MUX is P,

$$\therefore \quad P = \bar{S}_1\bar{S}_0 I_o + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

where, $S_1 = A$; $S_0 = B$; $I_0 = 1$; $I_1 = 0$; $I_2 = B$, $I_3 = 1$

$$P = \bar{A}\bar{B}(1) + \bar{A}B(0) + A\bar{B}(B) + AB$$

$$P = \bar{A}\bar{B} + AB$$

Output,

$$Y = \bar{S}I_0 + SI_1$$

$$= \overline{\overline{AB}}(B) + \overline{AB}\cdot P = AB + (\bar{A} + \bar{B})(\bar{A}\bar{B} + AB)$$

$$= AB + \bar{A}\bar{B} + \bar{A}\bar{B} = AB + \bar{A}\bar{B}$$

$$Y = A \odot B$$

48. (a)

In a 4-bit ripple counter, four flip-flops (FF0 to FF3) are used. The input frequency of flip-flop FF0 is 'f' and its output waveform frequency is $f/2$ which is applied as input of FF1. Consequently, the output waveform frequency of FF1 is $f/4$ which is used as input of FF2.

Then output waveform frequency of FF2 is $f/8$ which is used as input of FF3. Therefore, the output waveform frequency of FF3 is f/16 and the time period is

$$T = \frac{1}{\text{Frequency}} = \frac{16}{f}$$

Since, time period of the last flip-flop (FF3) is 128 microseconds.

$$\therefore \quad T = \frac{16}{f} = 128\times10^{-6}$$

$$\therefore \quad f = \frac{16}{128\times10^{-6}} = 125\,\text{kHz}$$

$\therefore$ The clock frequency of a 4-bit ripple counter is,

$$f = 125\ \text{kHz}$$

49. (c)

15's complement is equivalent to

$$\begin{array}{r} \text{F F F} \\ -\,\underline{\text{B B D}} \\ (4\,4\,2)_{16} \end{array}$$

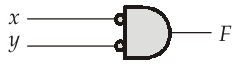
50. (b)

$$F = \overline{\overline{x + \bar{y} + x}}$$

$$= \overline{\overline{x + \bar{y}}\cdot\bar{x}}$$

$$= (x + \bar{y})\cdot(\bar{x})$$

$$F = \overline{x}\,\overline{y}$$



51. (b)

In toggle mode of operation in *J-K* flip-flop, the output frequency is half of the clock frequency.

$$\therefore \quad f = \frac{1}{2} \times 3\,\text{MHz} = 1.5\,\text{MHz}$$

52. (d)

The *K*-map wraps around itself, so the top and bottom cells are adjacent to each other. The cells of the rightmost column are adjacent to those in the leftmost column of the map. The minterms may be grouped horizontally or vertically.

Groupings may occur in the size of 2^r where, r = 1, 2, 3 ... n.

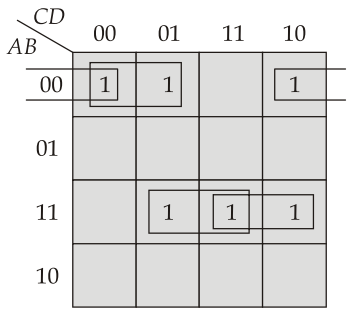
53. (c)

Excess-3 code representation for integers 0 to 9 is

Number	Code (*ABCD*)
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

$\therefore$ The excess-3 code, $f_{ABCD} = \Sigma m(3, 4, 5, 6, 7, 8, 9, 10, 11, 12)$

Invalid code is $f'_{ABCD} = \Sigma m(0, 1, 2, 13, 14, 15)$



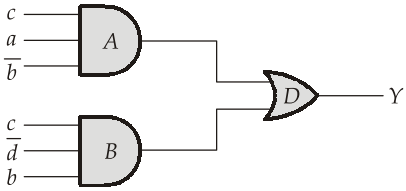
$$f'_{ABCD} = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{D} + ABD + ABC$$

$$f'_{ABCD} = \overline{A}\,\overline{B}(\overline{C} + \overline{D}) + AB(C + D)$$

54. (c)

The output, $Y = a\bar{b}c + \bar{d}bc + \bar{d}ac$

$= c[a\bar{b} + \bar{d}b + \bar{d}a] = c[a\bar{b} + \bar{d}b]$, using consensus theorem



55. (c)

In priority encoder, if an input has 1 then the other inputs with lower priority can be considered with the "don't care" condition.

$I_2 = 1$, $I_3 = 0$; $I_1 = X$ and $I_0 = X$.

Hence, the output will be 10.

56. (b)

Since, RIGHT/$\overline{\text{LEFT}}$ input is HIGH, it's a right shift register.

After 3 clock pulses, entered bits are 011 shifting the bits of register to the right.

Given, 1101 $\longrightarrow$ 1011

1st clock pulse $\Rightarrow$ 1110 $\longleftarrow$ 101

2nd clock pulse $\Rightarrow$ 1111 $\longleftarrow$ 10

3rd clock pulse $\Rightarrow$ 0111 $\longleftarrow$ 1

Therefore, 0111 is the stored valued in the register.

57. (a)

After every full modulus the initial state will repeat, hence after 16-clock pulses the counter holds the same state i.e., decimal 5. The remaining clock pulses are 30 – 16 = 14, so, the final state is 14 + 5 = 19 = 16 + 3.

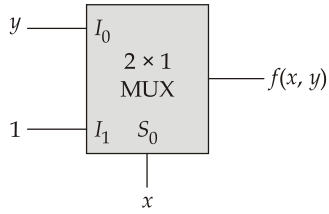
$\therefore$ After 30th clock pulse the counter reads 0011.

58. (c)

From the given circuit,

$$f(x, y) = x \oplus y \oplus xy$$
$$= x \oplus \left[y(\overline{xy}) + \bar{y}(xy)\right]$$
$$= x \oplus \bar{x}y$$
$$= x(\overline{\bar{x}y}) + \bar{x}(\bar{x}y)$$
$$= x(x + \bar{y}) + \bar{x}(\bar{x}y) = x + \bar{x}y$$
$$f(x, y) = x + y$$

Hence, we can design the above $f(x, y)$ function by using 2 × 1 MUX as follows:



60. (b)

Given, $A \oplus C = B$

$$\bar{A}C + A\bar{C} = B \quad \text{...(i)}$$

$$A \odot B = AB + \bar{A}\bar{B}$$

$$= A[\bar{A}C + A\bar{C}] + \bar{A}[\overline{\bar{A}C + A\bar{C}}]$$

$$= A\bar{C} + \bar{A}[\overline{\bar{A}C} \cdot \overline{A\bar{C}}] = A\bar{C} + \bar{A}\left[(A + \bar{C})(\bar{A} + C)\right]$$

$$= A\bar{C} + \bar{A}[\bar{C}\bar{A} + AC] = A\bar{C} + \bar{A}\bar{C} + 0$$

$$= \bar{C}[A + \bar{A}]$$

$$= \bar{C}$$

61. (d)

Given, $\bar{A} + AB = 0$

(i) $(\bar{A} + A)(\bar{A} + B) = 0$

$$\bar{A} + B = 0$$

$\Rightarrow$ $A = 1$ and $B = 0$

(ii) $AB = AC$

(or) $B = C$

(iii) $AB + A\bar{C} + CD = \bar{C}D$

$$1.0 + 1.1 + 0 \cdot D = 1 \cdot D$$

$$D = 1$$

Hence, option (d) is correct.

62. (d)

Given: $\dfrac{(302)_x}{(20)_x} = (12.1)_x$

$$\frac{3x^2 + 2}{2x} = x + 2 + \frac{1}{x}$$

$$3x^2 + 2 = 2x^2 + 4x + 2$$

$$x^2 - 4x = 0$$

$\therefore$ $x = 4$

63. (d)

PSRAM is basically a dynamic RAM. It has a built in refresh logic. Hence, no external refreshing circuit is required and thereby PSRAM can be used as a static RAM device. SRAM is used in hard disk buffers, router buffers and LCD screen. LCD screens employ SRAM to hold the image displayed.

64. (d)

Since, SRAM uses flip-flops, which can be made of upto 6 transistors, SRAM needs more transistors to store 1-bit than DRAM does, which only uses a single transistor and capacitor.

Thus, for the same amount of memory, SRAM requires higher number of transistors which increases the production cost compared to DRAM.

65. (d)

In the ripple counter (asynchronous counter) different flip-flops are applied with different clocks. Only one flip-flop is applied with external clock and for rest of the flip-flops, the output of one flip-flop acts as clock for the next flip-flop. For every input clock pulse, atleast one flip flop get clocked at a time. The triggering edge of the clock pulses of more than one flip-flops may also coincide at some time.

66. (c)

Input voltage required to generate a change of 1 LSB at the output is

$$\Delta V_i = \frac{V_{FS}}{2^n}$$

$$\Delta V_i = \frac{8}{2^8} = \frac{2^3}{2^8} = \frac{1}{2^5} = 31.25\,\text{mV}$$

67. (d)

CMOS devices dissipates almost zero static power.

Dynamic power of CMOS device = $Cf V_{DD}^2$

68. (b)

A	B	T_2	T_3	Y
0	0	ON	ON	1
0	1	ON	OFF	1
1	0	OFF	ON	1
1	1	OFF	OFF	0

Transistor T_1 is always in saturation mode.

$$Y = \overline{A} + \overline{B} = \overline{A \cdot B}$$

$\therefore$ NAND gate.

69. (c)

0	1	1	0	CLK pulse
1	1	0	1	(1)
1	0	1	1	(2)
0	1	1	0	(3)

70. (a)

Full adder, full subtractor and half adder come under the class of combinational logic circuits.

$\Rightarrow$ *J-K* flip flop and counter comes under the class of sequential logic circuit.

71. (a)

MOD-1000 ripple-up counter is constructed using 10-flip flops.

The MSB i.e., Q_9 will have 50% duty cycle if it is MOD-1024 ripple up counter.

But for MOD-1000, Q_9 will be '0' for 512 clock pulses and will be '1' for 488 clock pulses.

Hence, $$\text{Duty cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$\%\,\text{Duty cycle} = \frac{488\,T_{CLK}}{1000\,T_{CLK}} \times 100 = 48.8\%$$

72. (c)

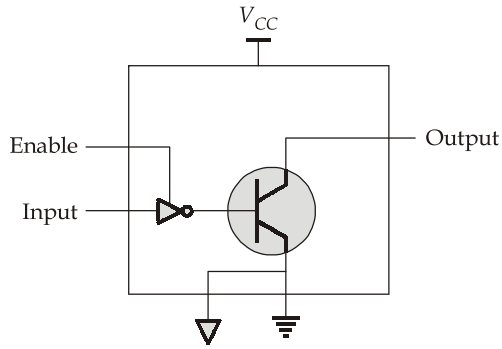
$$\text{Memory capacity} = 16\text{ K} \times 16 = 2^4 \times 2^{10} \times 16 = 2^{14} \times 16$$

$\therefore$ Address lines = 14

Data lines = 16

73. (d)

Since, the tri-state buffer allows input to go to output when desired using enable input, it can be used to design multiplexers, where a selected input is sent to the output.The open-collector tri-state buffer is as shown below:



74. (c)

The input at which flip-flop changes its state when synchronized with the clock is called synchronous control inputs.

75. (c)

By using the combination of NAND and NOR gates, we can realize any Boolean function but not with the minimum number of logic gates. Hence. Statement(II) is incorrect.

❍❍❍❍