DETAILED SOLUTIONS

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ESE 2023 : Prelims Exam
CLASSROOM TEST SERIES

ELECTRICAL ENGINEERING

Test 2

Section A : Electrical Circuits

Section B : Digital Electronics + Microprocessors

ANSWER KEY

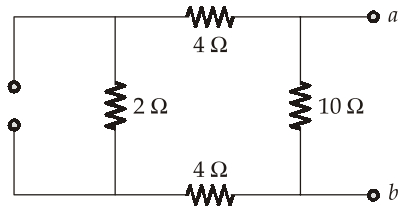
1. (a)	**16.** (c)	**31.** (a)	**46.** (d)	**61.** (d)
2. (b)	**17.** (d)	**32.** (c)	**47.** (a)	**62.** (a)
3. (c)	**18.** (d)	**33.** (c)	**48.** (b)	**63.** (d)
4. (a)	**19.** (a)	**34.** (a)	**49.** (d)	**64.** (c)
5. (d)	**20.** (c)	**35.** (b)	**50.** (a)	**65.** (c)
6. (b)	**21.** (a)	**36.** (c)	**51.** (c)	**66.** (c)
7. (a)	**22.** (b)	**37.** (b)	**52.** (c)	**67.** (d)
8. (a)	**23.** (c)	**38.** (d)	**53.** (b)	**68.** (c)
9. (c)	**24.** (d)	**39.** (c)	**54.** (a)	**69.** (b)
10. (b)	**25.** (b)	**40.** (d)	**55.** (d)	**70.** (a)
11. (a)	**26.** (b)	**41.** (d)	**56.** (a)	**71.** (d)
12. (d)	**27.** (d)	**42.** (d)	**57.** (b)	**72.** (c)
13. (d)	**28.** (c)	**43.** (b)	**58.** (a)	**73.** (c)
14. (c)	**29.** (d)	**44.** (b)	**59.** (a)	**74.** (c)
15. (c)	**30.** (d)	**45.** (a)	**60.** (b)	**75.** (c)

Note: Answer key has been updated of Q.18 & 19.

DETAILED EXPLANATIONS
Section A : Electrical Circuits

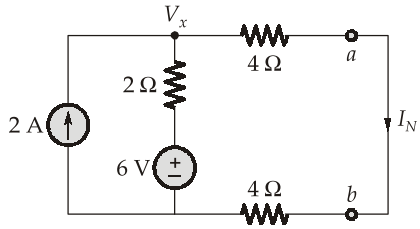
1. (a)

R_{eq} can be drawn as



$$R_N = 10 \,||\, 10 = 5\ \Omega$$

For I_N



$$\frac{V_x}{8} + \frac{V_x - 6}{2} = 2$$

$$\frac{V_x + 4V_x - 24}{8} = 2$$

$$5V_x - 24 = 16$$

$$5V_x = 40$$

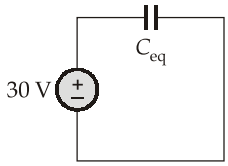
$$V_x = 8\ \text{V}$$

$$I_N = \frac{V_x}{4+4} = \frac{V_x}{8}$$

$$\therefore \quad I_N = \frac{8}{8} = 1\ \text{A}$$

2. (b)

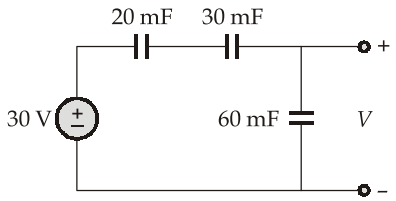
Above circuit can be reduced as



40 mF is in parallel with 20 mF capacitor which are in series with 20 mF and 30 mF capacitor,

$$\therefore \quad C_{eq} = \frac{1}{\frac{1}{20} + \frac{1}{30} + \frac{1}{40+20}} \times 10^{-3} = 10\ \text{mF}$$

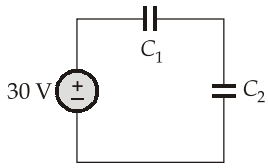
Total charge is, $\quad q = C_{eq} \times V = 10 \times 10^{-3} \times 30 = 0.3\ \text{C}$



Since charge 'q' is constant in series capacitors thus we can calculate

$$\therefore \quad V = \frac{q}{C} = \frac{0.3}{60 \times 10^{-3}} = 5 \text{ V}$$

Alternate Solution:



$$C_1 = 20 \parallel 30 = \frac{20 \times 30}{20 + 30} = 12 \text{ mF}$$

$$C_2 = 40 + 20 = 60 \text{ mF}$$

By voltage division,

$$V_{40} = \frac{30 \times C_1}{C_1 + C_2} = \frac{30 \times 12}{60 + 12}$$

$$V_{40} = 5 \text{ V}$$

3. (c)

$$V_1 = 40I_1 + j20I_2$$

$$V_2 = j30I_1 + 50I_2$$

$$V_1 = 100\angle 0°$$

and $V_2 = -10I_2$

Thus, $-10I_2 = j30I_1 + 50I_2$

$$\therefore \quad \frac{I_2}{I_1} = -j0.5$$

4. (a)

For parallel resonant circuit,

$$Q_0 = R\sqrt{\frac{C}{L}} = 2000\sqrt{\frac{54 \times 10^{-6}}{960 \times 10^{-3}}}$$

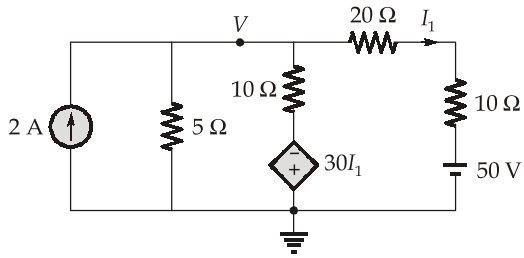
$$= 2000\sqrt{\frac{9}{16} \times 10^{-4}} = 2000 \times \frac{3}{4} \times 10^{-2} = 1500 \times 10^{-2} = 15$$

5. (d)

- Superposition theorem can't be used for the given circuit, because while acting one source alone, the circuit violates KVL.
- Superposition theorem is applicable when there are different source.

6. (b)

Applying nodal analysis we get,



$$\frac{V-50}{30}+\frac{V+30I_1}{10}+\frac{V}{5} = 2$$

$$V\left[\frac{1}{30}+\frac{1}{10}+\frac{1}{5}\right]+3I_1 = 3.66 \quad \text{...(i)}$$

Now, $$I_1 = \frac{V-50}{30} \quad \text{...(ii)}$$

Combining equation (i) and (ii), we get

$$\frac{V}{3}+3\left[\frac{V-50}{30}\right] = 3.66$$

$$\frac{V}{3}+\frac{V-50}{10} = 3.66$$

$$\frac{10V+3V-150}{30} = 3.66$$

$$\frac{13V-150}{30} = 3.66$$

$$V = 20 \text{ V}$$

7. (a)

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

By applying KVL at the output,

$$V_2 = -I_2 \times 1 = -I_2$$

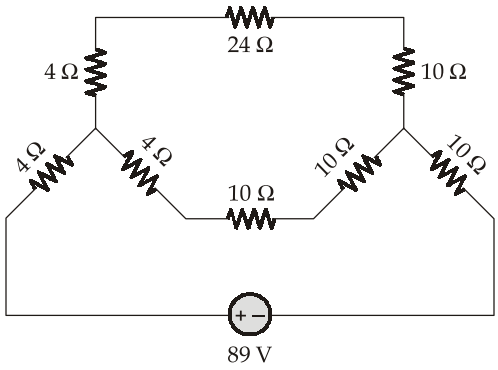
Now,
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$
$$V_2 = Z_{21}I_1 - Z_{22}V_2$$
$$(1 + Z_{22})V_2 = Z_{21}I_1$$
$$\frac{V_2}{I_1} = \frac{Z_{21}}{1+Z_{22}}$$

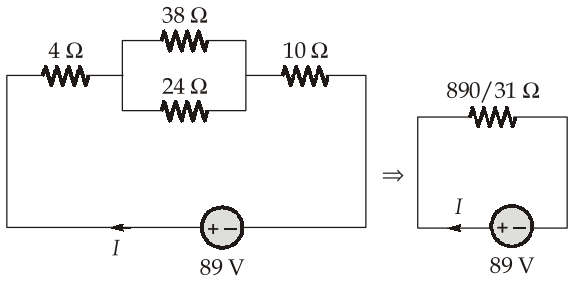
8. (a)

Applying delta to star conversion, we get

$$R = \frac{12\times 12}{12+12+12} = 4\ \Omega$$

$$R' = \frac{30\times 30}{30+30+30} = 10\ \Omega$$

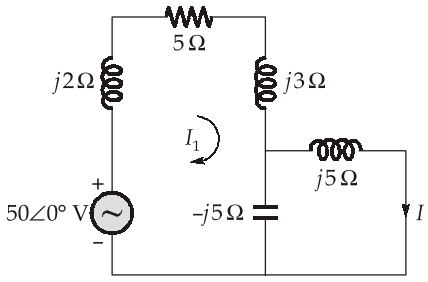




$$\therefore \quad I = \frac{V}{R} = \frac{89}{890}\times 31$$

$$\therefore \quad P = VI = 89\times\frac{89}{890}\times 31 = 275.9\ \text{W}$$

9. (c)



KVL in loop-1,

$$-50\angle 0° + j2I_1 + 5I_1 + j3I_1 - j5(I_1 - I) = 0$$

$$5I_1 + j5I = 0 \qquad \ldots(i)$$

$$-j5(I - I_1) + j5I = 0$$

$$j5I_1 = 0 \quad \ldots(ii)$$

$$\begin{bmatrix} 5 & j5 \\ j5 & 0 \end{bmatrix}\begin{bmatrix} I_1 \\ I \end{bmatrix} = \begin{bmatrix} 50\angle 0° \\ 0 \end{bmatrix}$$

By Cramer's rule,

$$I = \frac{\begin{vmatrix} 5 & 50\angle 0° \\ j5 & 0 \end{vmatrix}}{\begin{vmatrix} 5 & j5 \\ j5 & 0 \end{vmatrix}} = 10\angle -90° = -j10 \text{ A}$$

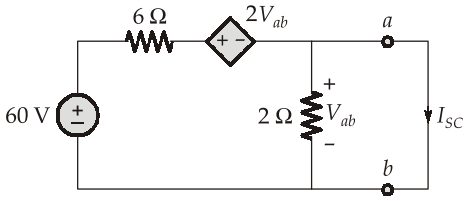
10. (b)

The value of output resistance can be calculated as

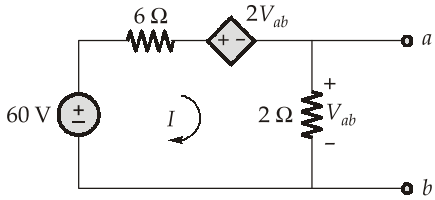
$$R_{th} = \frac{V_{OC}}{I_{SC}}$$

$$V_{OC} = V_{ab}$$

Now, calculating the short circuit current by applying source transformation, we get



$$I_{SC} = \frac{60}{6} = 10 \text{ Amp}$$



$$6I + 2V_{ab} + 2I - 60 = 0$$

$$V_{ab} = 2I$$

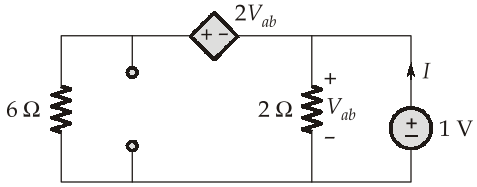
$$I = 5 \text{ A}$$

$$V_{ab} = 2 \times 5 = 10 \text{ V}$$

$$\therefore \quad R_{th} = \frac{10}{10} = 1\Omega$$

Alternate Solution:

To calculate R_{Th}, deactivate all independent sources, and put a test source of 1 V at *ab*



$$I = \frac{1}{2} + \frac{1 + 2V_{ab}}{6}$$

$\because$ $V_{ab} = 1\text{ V}$

$\therefore$ $$I = \frac{1}{2} + \frac{3}{6} = 1\text{ A}$$

$$R_{ab} = R_{Th} = \frac{1}{1} = 1\ \Omega$$

11. (a)

Norton's equivalent circuit is dual of Thevenin's equivalent circuit.

12. (d)

Energy stored in capacitor is $\frac{1}{2}CV^2$.

Whereas the energy stored in inductor is $\frac{1}{2}Li^2$.

13. (d)

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0}$$

$\therefore$ $$I_2 = \frac{-\alpha V_1}{10}$$

$\therefore$ $$y_{21} = \frac{-\alpha}{10} = 0.2$$

$$\alpha = -2$$

14. (c)

$$R_P = R(1 + Q^2)$$

Now, $$Q = \frac{|X_L|}{R_L} = \frac{20}{20} = 1$$

$\therefore$ $$R_P = 20 \times 2 = 40\ \Omega$$

and $$jX_P = j20\left(1 + \frac{1}{Q^2}\right) = j40\Omega$$

Alternate Solution:

$$Y_{eq} = G - jB_L = \frac{1}{20 + j20} = \frac{20 - j20}{20^2 + 20^2}$$

$$G = \frac{20}{800} = \frac{1}{40} \Rightarrow R_P = 40\ \Omega$$

$$B_L = \frac{20}{800} = \frac{1}{40} \Rightarrow X_P = 40\ \Omega$$

15. (c)

Overall circuit impedance,

$$Z = (Z_2 \parallel Z_3) + Z_1$$

$$(Z_2 \parallel Z_3) = \frac{(2 + j4)(6 - j8)}{(8 - j4)} = \frac{(1 + j2)(3 - j4)}{(2 - j1)} \times \frac{(2 + j1)}{(2 + j1)}$$

$$= \frac{(11 + j2)(2 + j1)}{5} = \frac{20 + j15}{5} = (4 + j3)\Omega$$

$$Z = Z_1 + (Z_2 \parallel Z_3)$$

$$= (6 - j8) + (4 + j3)$$

$$= (10 - j5)\ \Omega$$

$$|I| = \frac{|V|}{|Z|} = \frac{100}{5\sqrt{5}} = \frac{20}{\sqrt{5}} \text{A (peak)}$$

Average power delivered by the source,

$$P = \frac{I_m^2}{2} \times R = \frac{(20)^2 \times 10}{5 \times 2} = 400\ \text{W}$$

16. (c)

Series and parallel RLC circuits fall into one of three categories, depending on the relative values of R, L and C :

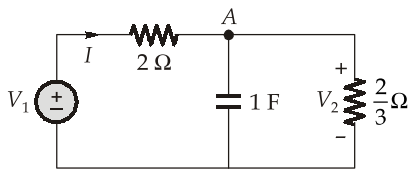
Overdamped	$\alpha > \omega_0$
Critically damped	$\alpha = \omega_0$
Underdamped	$\alpha < \omega_0$

17. (d)

Applying KCL at node A,

$$I = \frac{V_2}{2/3} + C\frac{dV_2}{dt}$$

$$= \frac{1 - e^{-2t}}{2/3} + C\frac{d}{dt}(1 - e^{-2t})$$



$$= \frac{3}{2} - \frac{3}{2}e^{-2t} + 2e^{-2t} = \frac{3}{2} + \frac{1}{2}e^{-2t}$$

Applying KVL we get,

$$V_1 = 2I + V_2$$

$$= 2\left(\frac{3}{2} + \frac{1}{2}e^{-2t}\right) + 1 - e^{-2t}$$

$$V_1 = 3 + e^{-2t} + 1 - e^{-2t} = 4 \text{ V}$$

18. (d)

Number of independent loops = $b - N + 1$

Number of nodes, $N = 8$

Number of branches, $b = 16$

Number of independent loops = $16 - 8 + 1$

$= 9$

19. (a)

The input admittance is

$$Y = j\omega \times 0.1 + \frac{1}{10} + \frac{1}{2 + j2\omega}$$

$$= 0.1 + j\omega \times 0.1 + \frac{1}{2 + j2\omega}\left(\frac{2 - j2\omega}{2 - j2\omega}\right)$$

$$= 0.1 + j\omega \times 0.1 + \frac{2 - j2\omega}{4 + 4\omega^2}$$

At resonance, $I_m(Y) = 0$

$$\omega_0 \times 0.1 - \frac{2\omega_0}{4 + 4\omega_0^2} = 0$$

$$\omega_0 \times 0.1 = \frac{2\omega_0}{4 + 4\omega_0^2}$$

$$4 + 4\omega_0^2 = \frac{2\omega_0}{0.1\omega_0} = 20$$

$$\omega_0^2 = 4$$

$$\omega_0 = 2 \text{ rad/sec}$$

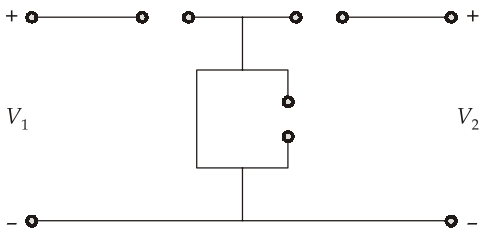
20. (c)

At $\omega = 0$,

i.e., $f = 0$

$$X_L = 0$$

$$X_C = \infty$$



There is no connection between input and output,

So, $V_2 = 0$

At $\omega = \infty$,

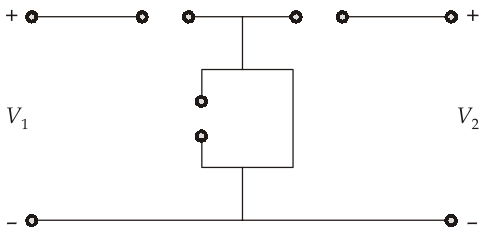
i.e. $f = \infty$,

$$X_L = \infty$$

$$X_C = 0$$

Then also, there is no connection between input and output,

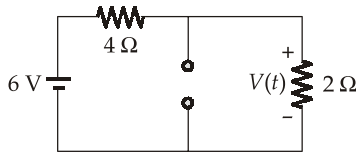
So, $V_2 = 0$



Band pass filter.

21. (a)

At $t = 0^-$, steady-state condition is reached, hence the capacitor acts as an open circuit,

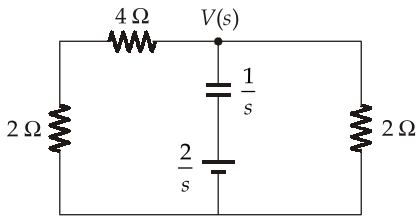


$$V(0^-) = 6 \times \frac{2}{4+2} = 2\ \text{V}$$

Since voltage across the capacitor can not change instantaneously,

$$V(0^+) = 2\ \text{V}$$

For $t > 0$, the transformed network is shown in figure



Applying KCL at node for $t > 0$,

$$\frac{V(s)}{6}+\frac{V(s)-2/s}{1/s}+\frac{V(s)}{2} = 0$$

$$V(s)\left(\frac{2}{3}+s\right) = 2$$

$$V(s) = \frac{2}{s+\frac{2}{3}}$$

Taking the inverse Laplace transform,

$$V(t) = 2e^{-(2/3)t}$$

22. (b)

Since all the branches are connected in parallel to the current source. Thus,

$$\frac{i_1}{i_2} = \frac{\frac{1/50}{R_{eq}}}{\frac{1/100}{R_{eq}}} = \frac{100}{50} = 2$$

Where, $$\frac{1}{R_{eq}} = \frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4} = 16.67\ \Omega$$

23. (c)

$$V_1 = nV_2\ ; \qquad \text{Since } \left(\frac{V_1}{V_2}=\frac{n}{1}\right)$$

and $$I_1 = \frac{1}{n}I_2\ ; \qquad \text{Since } \left(\frac{I_1}{I_2}=\frac{n}{1}\right)$$

$\therefore$ $$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & \frac{1}{n} \end{bmatrix}$$

24. (d)

All statements are correct.

25. (b)

When multiple sources are present, each operating at a different frequency, the individual contribution to average power may be summed. This is not true for sources operating at the same frequency.

26. (b)

The complex frequency, $s = \sigma + j\omega$ is the general case;

dc ($s = 0$), exponential ($\omega = 0$) and sinusoidal ($\sigma = 0$) functions are special cases.

27. (d)

All statement are correct.

28. (c)

Both statement I and statement-II are correct. They both are examples of reciprocity theorem.

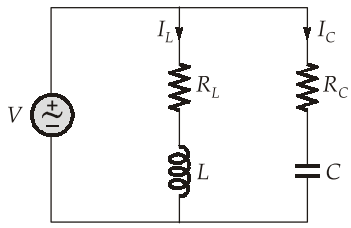
29. (d)

All statement are correct.

30. (d)

All statements are correct.

31. (a)



Phase angle of the inductive branch,

$$\phi_L = \tan^{-1}\left(\frac{\omega L}{R_L}\right)$$

Phase angle of the capacitive branch,

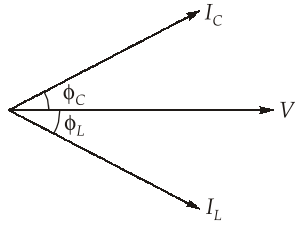
$$\phi_C = \tan^{-1}\left(\frac{1}{\omega R_C C}\right)$$

For I_L and I_C to be in quadrature,

$$\phi_L + \phi_C = 90°$$

$$\tan^{-1}\left(\frac{\omega L}{R_L}\right) + \tan^{-1}\left(\frac{1}{\omega R_C C}\right) = 90°$$

$$\left(\frac{\frac{\omega L}{R_L} + \frac{1}{\omega R_C C}}{1 - \frac{\omega L}{\omega R_C R_L C}}\right) = \tan 90° = \frac{1}{0}$$



$$1 - \frac{\omega L}{\omega R_C R_L C} = 0$$

$$\Rightarrow \quad R_C R_L = \frac{L}{C}$$

32. (c)

Let, V_L line voltage, I_L line current, V_p phase Voltage, I_p phase current

For a balanced star-connected system

$$\therefore \quad V_p = \frac{V_L}{\sqrt{3}} \text{ and } I_P = I_L$$

$$\therefore \text{ Impedance per phase, } \quad Z_{star} = \frac{V_P}{I_P}$$

$$= \frac{V_L / \sqrt{3}}{I_P} = \frac{1}{\sqrt{3}} \frac{V_L}{I_L} \qquad \text{...(i)}$$

For a balanced delta-connected system,

For the same line voltages and currents,

$$\therefore \quad V_P = V_L$$

and

$$I_P = \frac{I_L}{\sqrt{3}}$$

$$\therefore \text{ Impedance per phase, } \quad Z_{delta} = \frac{V_P}{I_P} = \frac{V_L}{\frac{I_L}{\sqrt{3}}} = \sqrt{3} \frac{V_L}{I_L} \qquad \text{...(ii)}$$

From equation (i) and (ii),

$$\frac{Z_{Star}}{Z_{Delta}} = \frac{1}{3}$$

$$\therefore \quad Z_{star} = \frac{1}{3} Z_{Delta}$$

33. (c)

Equivalent inductive reactance,

$$X_L = (j5 + j6 + j7) - 2(j2 + j3 - j5)$$
$$= j18 \ \Omega$$

34. (a)

For parallel-opposing connection,

$$\text{Total inductance} = \frac{L_1 L_2 - M^2}{L_1 + L_2 + 2M}$$

35. (b)

Applying KVL to mesh-1,

$$V_1 = 3I_1 + I_2 \quad \text{...(i)}$$

Applying KVL to mesh-2,

$$V_2 = I_1 + 3I_2 \quad \text{...(ii)}$$

Comparing equation (i) and (ii) with z-parameter equations, we get

$$\begin{bmatrix} z''_{11} & z''_{12} \\ z''_{21} & z''_{22} \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix}$$

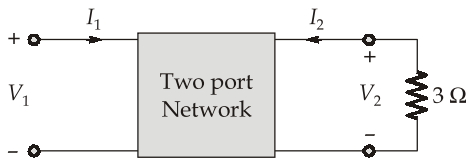
Hence, z-parameters of the overall connection are

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix} + \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix} = \begin{bmatrix} 6 & 2 \\ 2 & 6 \end{bmatrix}$$

36. (c)

$$V_1 = 5I_1 + 2I_2 \quad \text{...(i)}$$

$$V_2 = 2I_1 + I_2 \quad \text{...(ii)}$$



$$V_2 = -3I_2 \quad \text{...(iii)}$$

Substituting the equation (iii) in the given equation (ii),

$$-3I_2 = 2I_1 + I_2$$

$$I_2 = \frac{-I_1}{2} \quad \text{...(iv)}$$

Substituting the equation (iv) in the equation (i),

$$V_1 = 5I_1 - I_1 = 4I_1$$

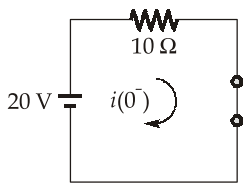
Input impedance, $$Z_i = \frac{V_1}{I_1} = 4\ \Omega$$

37. (b)

At $t = 0^-$, the network attains steady-state condition,

Hence, the inductor acts as a short circuit,

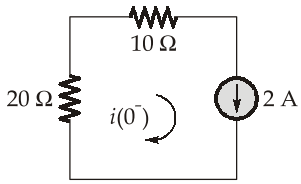
$$i(0^-) = \frac{20}{10} = 2\ \text{A}$$



At $t = 0^+$, the inductor acts as a current source of 2 A,

$$i(0^+) = 2 \text{ A}$$

Writing KVL equation for $t > 0$,



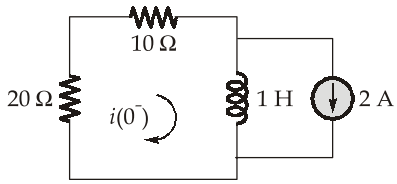
$$-30i - \frac{di}{dt} = 0$$

At $t = 0^+$

$$-30i(0^+) - \frac{di(0^+)}{dt} = 0$$

$$\frac{di(0^+)}{dt} = -30 \times 2 = -60 \text{ A/sec}$$

Differentiating the equation, (i) we get



$$-30i\frac{di}{dt} - \frac{d^2i}{dt^2} = 0$$

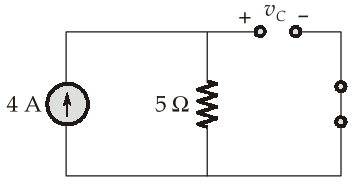
at $t = 0^+$

$$-30\frac{di}{dt}(0^+) = \frac{d^2i}{dt^2}(0^+)$$

$$\frac{d^2i}{dt^2}(0^+) = -30 \times -60 = 1800$$

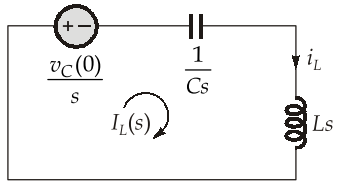
38. (d)

For $t < 0$,



$$v_C(0^-) = v_C(0^+) = 20 \text{ V}$$
$$i_L(0^-) = i_L(0^+) = 0 \text{ A}$$

Redrawing the circuit for $t > 0$,



Applying KVL, we get

$$I_L(s) = \frac{-\frac{20}{s}}{\frac{1}{Cs} + Ls} = \frac{-80}{s^2 + 64}$$

$$I_L(s) = \frac{-10(8)}{s^2 + (8)^2}$$

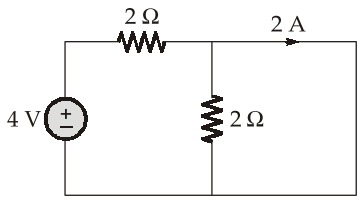
Taking Laplace inverse, we get

$$i_L(t) = -10 \sin 8t$$

39. (c)

$$V_R = 300 \text{ V}$$
$$V_L = 100 \text{ V}$$
$$V_C = 500 \text{ V}$$
$$V_S = \sqrt{V_R^2 + (V_C - V_L)^2}$$

40. (d)



In case of short circuit current is non zero.

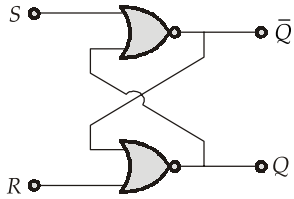
Section B : Digital Electronics + Microprocessors

41. (d)

For a counter type ADC of n bits, maximum conversion time is

$$= (2^n - 1)T_{clk}$$
$$= (2^6 - 1) \times \frac{1}{400\text{k}}$$
$$= 157.5 \text{ µsec}$$

42. (d)



S	R	Q_{n+1}
0	0	Q_n (HOLD state)
0	1	0 (Reset)
1	0	1 (Set)
1	1	$Q = \bar{Q} = 0$ (Invalid state)

43. (b)

To construct 8 × 256 line decoder by 3 × 8 line decoder

$$= \frac{256}{8} = 32$$

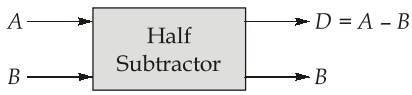
$$\frac{32}{8} = 4$$

$$\frac{4}{8} = 1$$

Total 3 × 8 line decoder required is

$$= 32 + 4 + 1 = 37$$

44. (b)



A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

45. (a)

For n variables function, minimum $(n - 1)$ select inputs are required. So $(2^{n-1} \times 1)$ is the minimum size of the multiplexer which is needed with an inverter to implement a boolean function of n variables.

46. (d)

$$y_1 = x \oplus y$$

and $$y_2 = x \oplus y$$

Truth table of XOR gate,

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR gate acts as buffer when one input is fixed at 0 and acts as inverter when one input is fixed at 1.

So,

$$y_3 = \overline{y}_1 = \overline{x \oplus y}$$

$$y_4 = y_2 = x \oplus y$$

$$f = y_3 + y_4 = 1$$

47. (a)

Truth table for -

OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

X-NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

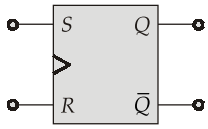
So, when both the inputs are at logic-1 then the output will be '1' in OR and X-NOR gate.

48. (b)

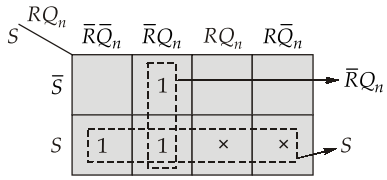
$$f = 1 \cdot \overline{S}_2\overline{S}_1 + \overline{A \cdot B} \cdot \overline{S}_2 S_1 + 0 \cdot S_2 \cdot \overline{S}_1 + 0 \cdot S_2 S_1$$

$$f = \overline{S}_2\left[\overline{S}_1 + \overline{AB}S_1\right]$$

49. (d)



S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×



$$Q_{n+1} = S + \bar{R}Q_n$$

50. (a)

For SR flip-flop, $Q_{n+1} = S + \bar{R}Q_n$

If we use inverter or NOT gate between S and R then,

$\Rightarrow$ $Q_{n+1} = S + \bar{\bar{S}}Q_n = S + SQ_n = S(1 + Q_n)$

$Q_{n+1} = S$

and this is the characteristics equation at a D flip-flop. Hence option (a) is correct.

51. (c)

Synchronous counter is the fastest counter with least delay.

52. (c)

For a universal-shift registers,

S_0	S_1	Mode of operation
0	0	No change (LOCKED STATE)
0	1	Shift-left
1	0	Shift-Right
1	1	Parallel-Loading

53. (b)

Race around condition occurs when $t_p < \Delta t < T$.

Hence option (b) is correct.

54. (a)

ECL is the fastest among all the logic families and PMOS is the slowest. TTL is faster than CMOS.

Hence the correct sequence of propagation delay is ECL < TTL < CMOS < NMOS.

55. (d)

The truth table of the above circuit is

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

So, $\text{Output} = \overline{A \cdot B}$

56. (a)

$$\text{Figure of merit (FoM)} = \text{Propagation delay (nsec)} \times \text{Power dissipation (mW)}$$

Hence option (a) is correct.

57. (b)

$$\begin{aligned} f &= (\overline{\overline{A \cdot B}}) \cdot (\overline{\overline{B + C}}) \\ &= (A \,.\, B) \cdot (B + C) \\ &= AB + ABC \\ f &= AB\,(1 + C) \\ f &= AB \end{aligned}$$

58. (a)

$$\begin{aligned} f &= A(A+B) + AB\bar{C} + AB\bar{C}D \\ &= A + AB + AB\bar{C}(1+D) \\ &= A + AB + AB\bar{C} \\ &= A + AB(1+\bar{C}) \\ &= A(1 + B) \\ &= A \end{aligned}$$

59. (a)

$$\text{Value of LSB} = \frac{10}{2^n - 1} = \frac{10}{2^4 - 1} = 0.66$$

60. (b)

Q_2^{+1}	Q_1^{+1}	Q_0^{+1}
0	0	0
0	0	1
0	1	1
1	1	0
1	0	1
0	1	0
⋮	⋮	⋮

Here, $Q_2^{+1} = Q_1$

$Q_1^{+1} = Q_0$

$Q_0^{+1} = Q_2 \odot Q_1$

So, the sequence of Q_0 is 011010 ....

61. (d)

n-bit ring counter is mod n-counter and n-bit Johnson counter is mod $2n$ counter,

So, $f_a = \dfrac{200\text{ kHz}}{10} = 20\text{ kHz}$

$f_b = \dfrac{20\text{ kHz}}{4} = 5\text{ kHz}$

$f_c = \dfrac{5\text{ kHz}}{2\times 8} = 312.5\text{ Hz}$

62. (a)

$f = a + \bar{a}b + \bar{a}\bar{b}c + \bar{a}\bar{b}\bar{c}d + ...$

Let, $f_1 = a + \bar{a}b$

$= (a+\bar{a})(a+b) = a + b$

$f_2 = a + \bar{a}b + \bar{a}\bar{b}c$

$= a + \bar{a}\left[b + \bar{b}c\right]$

$= a + \bar{a}(b+c)(b+\bar{b})$

$= a + \bar{a}(b+c)$

$= (a+\bar{a})(a+b+c)$

$= a + b + c$

Similarly, $f = a + \bar{a}b + \bar{a}\bar{b}c + \bar{a}\bar{b}\bar{c}d + ...$

$= a + b + c + d + ...$

63. (d)

SHLD 2015 H requires 5 machine cycle

F → 4 T
MERD → 3 T
MERD → 3 T
MEWR → 3 T
MEWR → 3 T

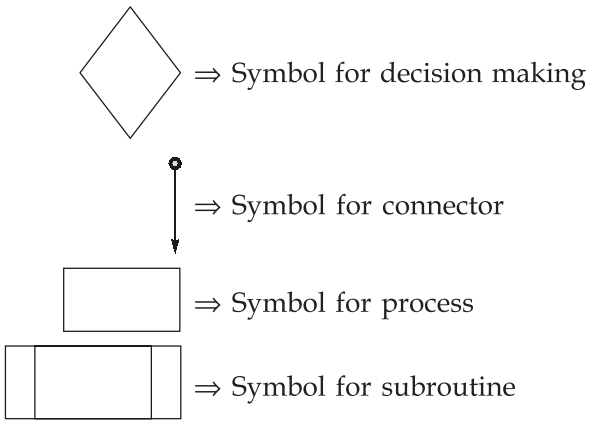
Total T-state of I_1 = 16 T

INX BC requires 1 machine cycle

F → 6 T

T-state of I_2 = 6 T

64. (c)



65. (c)

In 8085 there are 5 hardware and 8 software interrupt

5 hardware – TRAP, RST 7.5, RST 6.5, RST 5.5

8 software – RST 0, RST 1 ..... RST 7.

66. (c)

Only statement-3 is incorrect because encoder is a combinational circuit that performs the reverse operation of decoder. It has maximum of 2^n input lines and 'n' output lines, hence it encodes the information from 2^n input an n-bit code.

67. (d)

Option (a) and (b) are properties of Von-neumann architecture. Speed of harvard architecture is more than Von-Neumann. This type of architecture can result in space wastage because instruction memory cannot utilize the left over space in the data memory.

68. (c)

RST 4.5/TRAP is a non-maskable interrupt. RST 7.5 is edge triggering interrupt.

So, only 1 and 2 are correct.

69. (b)

INR M → All flags are affected except 'Cy'
ACI → affects all flag
RAL → affects only carry flag
POP PSW → affects no flag.

70. (a)

MVI A, A8H → A = 1010 1000
ORI C5 H → = 1100 0101
1110 1101

RRC → 1110 1101

1111 0110
A → F 6 H

So, contents of A → F6 H

71. (d)

2^n → Memory size (Where n → no. of address lines)

$2^n = 100$ TB

$= 100 \times (2^{40})$

$= 2^7 \times 2^{40} = 2^{47}$

So, 47 address line is required.

72. (c)

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1				F				F				F			

$(1FFF)_H = 1 \times 16^3 + 15 \times 16^2 + 15 \times 16 + 15$

$= (8191)_{DEC}$

73. (c)

READY pin is an active high signal and provides input to 8085 as an external request from slow peripheral to indicate that peripheral is not ready yet, for the data transfer between processor and peripheral device.

74. (c)

ECL family has the highest speed and least propagation delay. Hence statement (I) is correct.

In ECL family, the transistors never operate in saturation region. Hence statement (II) is not correct.

75. (c)

To reducing the number of pins in microprocessor data-bus is 'Time-Division Multiplexed' with address bus. It does not increase the speed of microprocessor.

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