DETAILED SOLUTIONS

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ESE 2022 : Prelims Exam
CLASSROOM TEST SERIES

ELECTRICAL ENGINEERING

Test 2

Section A : Electrical Circuits

Section B : Digital Electronics + Microprocessors

ANSWER KEY

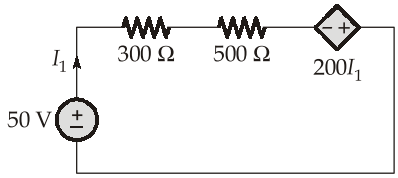
1. (*)	**16.** (d)	**31.** (c)	**46.** (b)	**61.** (d)
2. (d)	**17.** (d)	**32.** (d)	**47.** (a)	**62.** (b)
3. (b)	**18.** (d)	**33.** (b)	**48.** (a)	**63.** (c)
4. (a)	**19.** (a)	**34.** (a)	**49.** (c)	**64.** (d)
5. (c)	**20.** (d)	**35.** (d)	**50.** (b)	**65.** (d)
6. (b)	**21.** (b)	**36.** (c)	**51.** (a)	**66.** (a)
7. (a)	**22.** (d)	**37.** (a)	**52.** (d)	**67.** (c)
8. (c)	**23.** (a)	**38.** (a)	**53.** (d)	**68.** (c)
9. (d)	**24.** (a)	**39.** (a)	**54.** (d)	**69.** (b)
10. (b)	**25.** (b)	**40.** (c)	**55.** (b)	**70.** (d)
11. (c)	**26.** (c)	**41.** (a)	**56.** (d)	**71.** (c)
12. (d)	**27.** (a)	**42.** (d)	**57.** (b)	**72.** (a)
13. (d)	**28.** (c)	**43.** (d)	**58.** (a)	**73.** (b)
14. (b)	**29.** (b)	**44.** (d)	**59.** (a)	**74.** (c)
15. (a)	**30.** (d)	**45.** (a)	**60.** (d)	**75.** (d)

Note: In Q. no. 1 ('*' indicates) mark to all.

DETAILED EXPLANATIONS

1. (*)

Converting the dependent current source into dependent voltage source,



By KVL,

$$800I_1 - 200I_1 = 50$$

$$I_1 = \frac{50}{600} = 0.083 \text{ A}$$

Current throught 500 Ω = $I_1 - 0.4I_1 = 0.6\ I_1$

$$= 0.6 \times \frac{50}{600} = \frac{1}{20}$$

Power absorbed by the 500 Ω resistor

$$= I_1^2 R = \left(\frac{1}{20}\right)^2 \times 500 = 1.25 \text{ W}$$

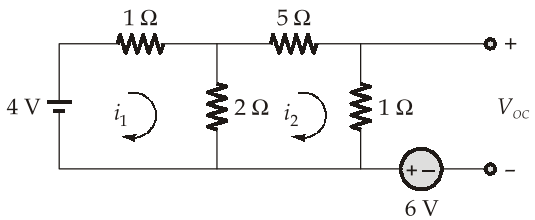
2. (d)

Properties of complete incidence matrix:

- The sum of the entries in any column is zero.
- The determinant of the incidence matrix of a closed loop is zero.
- The rank of the incidence matrix of a connected graph is $(n - 1)$, where n is number of nodes of the graph.

3. (b)

Removing the resistance R,



$$\therefore \quad 3i_1 - 2i_2 = 4 \qquad \text{...(i)}$$

and $\quad 8i_2 - 2i_1 = 0$

or $\quad i_1 = 4i_2 \qquad \text{...(ii)}$

Solving (i) and (ii), we get

$$i_2 = 0.4 \text{ A}$$

Applying KVL in outer loop,

$$1 \times i_2 + 6 = V_{OC}$$

$$V_{OC} = 6 + \frac{2}{5} = \frac{32}{5}\text{V} = 6.4\text{ V}$$

$\therefore$ For maximum power transfer,

$$R = R_{th} = \frac{17}{20} = 0.85\ \Omega$$

$\therefore$ Maximum power, $P_{max} = \dfrac{V_{OC}^2}{4R} = 12\text{ W}$

4. (a)

Total impedance of the circuit,

$$Z_T = 20 + (j200) - j200 = 20\ \Omega$$

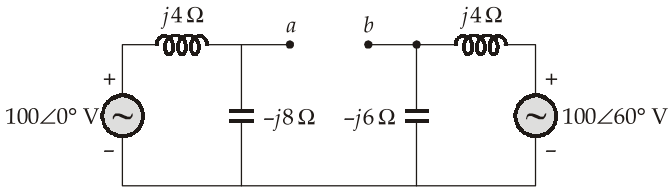
$$\text{Current, } I = \frac{20}{20} = 1\text{ A}$$

Hence voltage across capacitor,

$$V_C = 1 \times (-j200) = -j200\text{ V}$$

5. (c)

With a-b open circuited,



$$V_a = \frac{100\angle 0^\circ}{j4 - j8}(-j8) = 200\angle 0^\circ\text{ V}$$

$$V_b = \frac{100\angle 60^\circ}{j4 - j6}(-j6) = 300\angle 60^\circ\text{ V}$$

$\therefore$ $V_{th} = (V_a - V_b) = 200\angle 0^\circ - 300\angle 60^\circ$

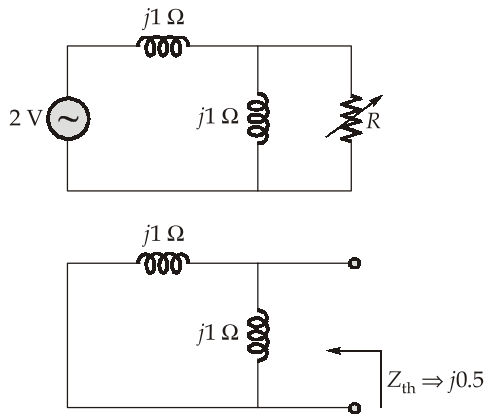
$= 200\cos 0^\circ + j200\sin 0^\circ - 300\cos 60^\circ - j300\sin 60^\circ$

$= (200 - 150) - j259.81$

$= 50 - j259.81\text{ V}$

$$Z_{th} = \frac{(j4)(-j8)}{j4 - j8} + \frac{(j4)(-j6)}{j4 - j6} = j20\ \Omega$$

6. (b)



$$R = |Z_{th}| = 0.5\ \Omega$$

Alternate Solution :

Here, Impedance across ac source,

$$Z = \frac{R \times j1}{R + j1} + j1 = \frac{-1 + j2R}{R + j1}$$

$$\therefore \qquad \text{Current, } I = \frac{2\angle 0°}{Z} = \frac{2\angle 0° \times (R + j1)}{-1 + j2R}$$

$\therefore$ Current through the resistance,

$$I_R = I \times \frac{j1}{R + j1} = \frac{j2}{-1 + j2R}$$

For maximum power,

$$\frac{dP}{dR} = 0$$

$$\frac{(1 + 4R^2) \times 4 - 4R \times 8R}{(1 + 4R^2)^2} = 0$$

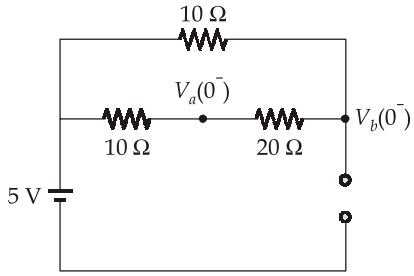
$$R = 0.5\ \Omega$$

7. (a)

The superposition principle states that the voltage across (or currents through) an element in a linear circuit is the algebraic sum of the voltage across (or current through) that element due to each independent source acting alone.

8. (c)

At $t = 0^-$, the network attains steady-state condition. Hence, the capacitor acts as an open circuit

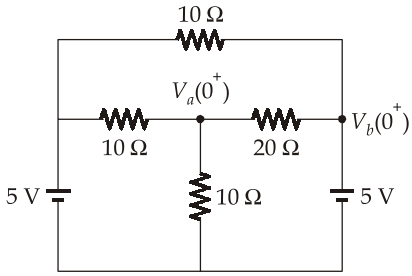


$$V_a(0^-) = 5 \text{ V}$$
$$V_b(0^-) = 5 \text{ V}$$

At $t = 0^+$, the capacitor acts as a voltage source of 5 V.

$$V_b(0^+) = 5 \text{ V}$$

writing KCL equation at $t = 0^+$



$$\frac{V_a(0^+)-5}{10}+\frac{V_a(0^+)}{10}+\frac{V_a(0^+)-5}{20} = 0$$

$$\frac{2V_a(0^+)-10+2V_a(0^+)+V_a(0^+)-5}{20} = 0$$

$$\frac{5V_a(0^+)-15}{20} = 0$$

$$V_a(0^+) = 3 \text{ V}$$

9. (d)

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = \frac{25}{1} = 25\ \Omega$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = \frac{2}{1} = 2$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = \frac{10}{50} = 0.2$$

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \frac{2}{50} = 0.04\,\text{℧}$$

Hence, the h-parameters are:

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} 25 & 0.2 \\ 2 & 0.04 \end{bmatrix}$$

10. (b)

Applying KVL to mesh-1,

$$V_1 = 3I_1 + I_2 \quad \text{...(i)}$$

Applying KVL to mesh-2,

$$V_2 = I_1 + 3I_2 \quad \text{...(ii)}$$

Comparing equation (i) and (ii) with z-paramter equations, we get

$$\begin{bmatrix} Z_{11}'' & Z_{12}'' \\ Z_{21}'' & Z_{22}'' \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix}$$

Hence, Z-parameter of the overall connections are

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix} + \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix}$$

$$= \begin{bmatrix} 6 & 2 \\ 2 & 6 \end{bmatrix}$$

11. (c)

Phase angle of the inductive branch,

$$\phi_L = \tan^{-1}\left(\frac{\omega L}{R_L}\right)$$

Phase angle of the capacitive branch,

$$\phi_C = \tan^{-1}\left(\frac{1}{\omega R_C C}\right)$$

For the two currents to be in quadrature, the condition is

$$\phi_L + \phi_C = 90°$$

$$\tan^{-1}\left(\frac{\omega L}{R_L}\right) + \tan^{-1}\left(\frac{1}{\omega R_C C}\right) = 90°$$

$$\tan^{-1}\left[\frac{\frac{\omega L}{R_L} + \frac{1}{\omega R_C C}}{1 - \frac{\omega L}{R_L} \times \frac{1}{\omega R_C C}}\right] = 90°$$

$$\frac{\frac{\omega L}{R_L} + \frac{1}{\omega R_C C}}{1 - \frac{L}{R_L R_C C}} = \tan 90° = \infty$$

$$1-\frac{L}{R_L R_C C}=0$$

$$R_L R_C=\frac{L}{C}$$

12. (d)

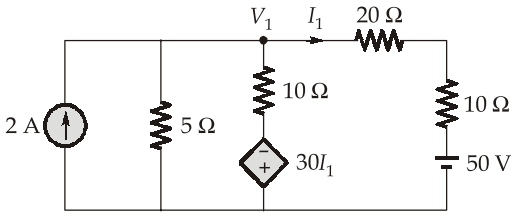
Quality factor, $Q=\frac{|V_C|}{V_m}=\frac{|V_L|}{V_m}$

Resonance frequency, $\omega_0=\sqrt{\omega_1\omega_2}$

$$Q=\frac{\omega L}{R}$$

13. (d)

Assume that the currents are moving away from the node



$$I_1=\frac{V_1-50}{20+10}=\frac{V_1-50}{30}$$

$$2=\frac{V_1}{5}+\frac{V_1+30I_1}{10}+\frac{V_1-50}{30}$$

$$2=\frac{V_1}{5}+\frac{V_1+30\left(\frac{V_1-50}{30}\right)}{10}+\frac{V_1-50}{30}$$

$$2=\frac{V_1}{5}+\frac{2V_1-50}{10}+\frac{V_1-50}{30}$$

$$2=\frac{6V_1+6V_1-150+V_1-50}{30}$$

$$V_1=20\text{ V}$$

$\therefore$ Voltage across the 5 Ω resistor = 20 V

14. (b)

$$V=4\times\left(i-\frac{i}{11}\right)=4\times\frac{10i}{11}$$

$$\frac{V}{i}=\frac{40}{11}\Omega$$

15. (a)

Suspectance of the series branch,

$$B = \frac{X_L}{R^2 + X_L^2} = \frac{10}{15^2 + 10^2} = \frac{10}{325}$$

The power factor of the system will be unity if the susceptance of the capacitor to be connected in parallel is equal to the susceptance of the series branch.

$$\omega C = B$$

$$C = \frac{B}{2\pi f} = \frac{10}{2\pi \times 50 \times 325} = 98\ \mu F$$

16. (d)

Equivalent resistance, between A and B,

$$R_{eq} = \{15 \| 10\} + \{6 \| 4\} = 6 + 2.4 = 8.4\ \Omega$$

17. (d)

- In parallel the effective area of the combined capacitor increases, increasing the overall capacitance while in series, the distance between the plates effectively increases, reducing the over all capacitance.
- A capacitor is an electrical device that can store energy in the electrostatic field between a pair of closely placed conductors.

18. (d)

All statements are correct.

19. (a)

Here, the current through R-C branch

$$I_2 = 1\angle 0° \times \frac{1 + j1}{1 + j1 + 1 - j1} = 0.707\angle 45°\ A$$

The voltage through resistor

$$V = 0.707\angle 45° \times 1$$
$$= 0.707\angle 45°\ V$$

Voltmeter reading = 0.707 V

20. (d)

$$L_1 + L_2 + 2M = 0.6 \quad ...(i)$$
$$L_1 + L_2 - 2M = 0.1 \quad ...(ii)$$

Given, $L_1 = 0.2$ H

$\therefore$ $L_2 + 2M = 0.4$ ...(iii)

$L_2 - 2M = -0.1$

On solving (iii) and (iv),

$L_2 = 0.15$ H and $M = 0.125$ H

21. (b)

Here,

initial current in the circuit,

$$i(0^-) = \frac{V_1}{R}$$

After changing the voltage, the KVL equation is

$$R_i(t) + L\frac{di(t)}{dt} = V_2\, u(t)$$

Taking Laplace transform,

$$RI(s) + L[sI(s) - i(0^-)] = \frac{V_2}{s}$$

$$I(s)[R + sL] = \frac{V_2}{s} + \frac{V_1 L}{R}$$

$$I(s) = \frac{V_2}{s(R+sL)} + \frac{V_1 L}{R}\left(\frac{1}{R+sL}\right)$$

$$= \frac{\frac{V_2}{L}}{s\left(s+\frac{R}{L}\right)} + \left(\frac{\frac{V_1}{R}}{s+\frac{R}{L}}\right)$$

Taking inverse Laplace transform,

$$i(t) = \frac{V_2}{R}\left[1 - e^{-(R/L)t}\right] + \frac{V_1}{R}e^{-(R/L)t}$$

$$= \frac{V_2}{R} + \left(\frac{V_1}{R} - \frac{V_2}{R}\right)e^{-(R/L)t}$$

If $R = 10\ \Omega$, $L = 1$ H, $V_1 = 200$ V

and $V_2 = 100$ V

We get, the current at $t = 0.5$ sec as

$$i(t) = \frac{100}{10} + \left(\frac{200}{10} - \frac{100}{10}\right)e^{-(10/1)\times 0.5}$$

$$= 10.07 \text{ A}$$

Alternate Solution:

Let the switching instant is $t = 0$

$$i(0^-) = \frac{V_1}{R} = \frac{200}{10} = 20 \text{ A}$$

$$\tau = \frac{L}{R} = \frac{1}{10}\text{sec}$$

$$i(\infty) = \frac{V_2}{R} = \frac{100}{10} = 10\text{ A}$$

$$i(t) = \left[i(0^-) - i(\infty)\right]e^{-t/\tau} + i(\infty) = (20 - 10)e^{-10t} + 10$$

at $t = 0.5$ sec,

$$i(0.5) = 10(1 + e^{-0.5 \times 10})$$
$$= 10(1 + e^{-5})$$
$$i(0.5) = 10.07\text{ A}$$

22. (d)

Condition for reciprocity

- $Z_{12} = Z_{21}$
- $AD - BC = 1$
- $g_{12} = -g_{21}$
- $h_{12} = -h_{21}$

23. (a)

- The resultant admittance parameter matrix for the parallel connection is the addition of the two individual admittance matrices.
- The resultant *ABCD* parameter matrix for the cascade connection is the multiplication of the two individual *ABCD* matrices.

24. (a)

Here, Load current, $I_L = \frac{4 \times 10^3}{200 \times 0.8} = 25\text{ A}$

Power factor $= \cos\phi = 0.8$

and $\sin\phi = 0.6$

$\therefore$ $I_L = 25\cos\phi - j25\sin\phi$

$= (20 - j15)\text{ A}$

When *C* is connected in parallel, the current should be in phase with the voltage,

Total current, $I = I_L + I_C = 20 - j15 + I_C$

For unity power factor, $I_C = j15$

$\therefore$ $j\omega CV = j15$

$$C = \frac{15}{2\pi \times 50 \times 200} = 238.73\ \mu\text{F}$$

25. (b)

- $\text{Peak factor} = \dfrac{\text{Maximum value or crest value}}{\text{rms value}}$
- The value of an alternating quantity at any instant of time is known as the instantaneous value.

26. (c)

Here, the turns ratio, $n = 10$

Load impedance, $Z_L = 10\ \text{k}\Omega$

$\therefore$ Input impedance, $Z_{in} = \dfrac{Z_L}{n^2} = \dfrac{10 \times 10^3}{10^2} = 100\ \Omega$

Primary current, $I_1 = \dfrac{100}{100 + 100} = 0.5\,\text{A}$

Secondary current, $I_2 = \dfrac{I_1}{n} = 0.05\ \text{A}$

$\therefore$ Average power dissipated in the 10 kW resistor is

$= (0.05)^2 \times 10 \times 10^3 = 25\ \text{W}$

27. (a)

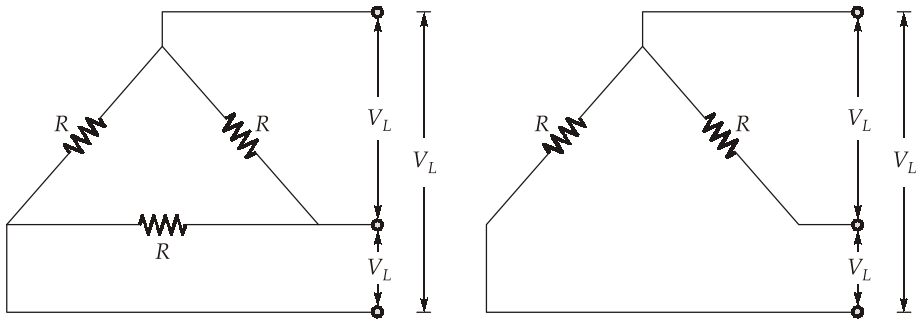
Let, V_L = The line voltage of the 3-phase supply

R = Resistance of each phase

Total power consumed in the load,

$$P = 3 \times \frac{V_p^2}{R} = 3 \times \frac{V_L^2}{R} = \frac{3V_L^2}{R}$$

When one resistor is removed, each of the remaining two resistor is connected across a supply of V_L as shown in



Total power consumed,

$$P' = 2 \times \frac{V_L^2}{R} = \frac{2V_L^2}{R}$$

$\therefore$ Reduced in load $= \dfrac{P - P'}{P} = \dfrac{\left(\dfrac{3V_L^2}{R}\right) - \left(\dfrac{2V_L^2}{R}\right)}{\dfrac{3V_L^2}{R}} = 33.33\%$

28. (c)

When x and y are open-circuited

The current in the second coil, $I_2 = 0$

The energy stored is

$$W = \frac{1}{2}L_1 I_1^2 = \frac{1}{2}\times 0.4 \times 2^2 = 0.8 \text{ J}$$

29. (b)

Let the resistance and reactances of the two circuits be R_1 , R_2 and X_1 and X_2 .

For the circuit 1st

Power factor = 0.8

$\therefore \quad R_1 = Z\cos\phi = 0.8Z$

and $\quad X_1 = Z\sin\phi = 0.6Z$

For the 2nd circuit,

Power factor = 0.6

$\therefore \quad R_1 = Z\cos\phi = 0.6Z$

and $\quad X_1 = Z\sin\phi = 0.8Z$

Impedance of the circuit

$$Z_T = (R_1 + jX_1) \,\|\, (R_2 + jX_2)$$

$$= \frac{(0.8Z + j0.6Z)\times(0.6Z + j0.8Z)}{(0.8Z + j0.6Z) + (0.6Z + j0.8Z)} = \frac{j1Z}{1.4 + j1.4} = 0.505Z\angle 45°$$

$\therefore$ Power factor of the circuit is cos 45° = 0.707

30. (d)

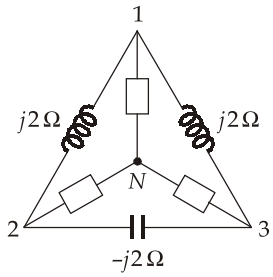
At frequencies below f_r , $\quad X_C > X_L$: the circuit is capacitive

At frequencies below f_r , $\quad X_C = X_L$: the circuit is purely resistance

At frequencies above f_r , $\quad X_C < X_L$: the circuit is inductive

31. (c)

Applying Δ to Y transformation



$$Z_{1N} = \frac{Z_{12}\times Z_{13}}{Z_{12} + Z_{13} + Z_{23}} = \frac{j2\times j2}{j2 + j2 - j2} = j2\ \Omega$$

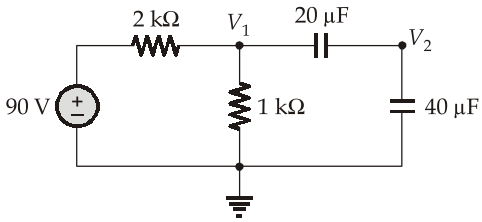
Similarly, $$Z_{2N} = \frac{j2 \times (-j2)}{j2 + j2 - j2} = -j2\,\Omega$$

$$Z_{3N} = \frac{j2 \times (-j2)}{j2 + j2 - j2} = -j2\,\Omega$$

32. (d)

- Kirchhoff's current law is derived from conservation of charge.
- Kirchhoff's voltage law is based on conservation of energy.

33. (b)



By applying voltage divider rule,

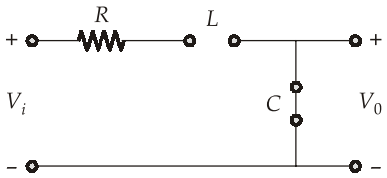
The voltage, $$V_1 = \frac{1}{1+2} \times 90 = 30\ \text{V}$$

$$V_2 = \frac{C_1}{C_1 + C_2} \times V_1$$

$$= 10\ \text{V}$$

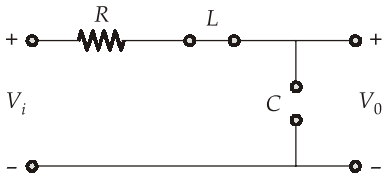
34. (a)

At $\omega \to \infty$, capacitor will be short circuited and inductor will be open circuited, circuit looks like



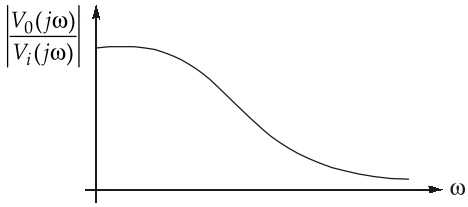
$$\left|\frac{V_0(j\omega)}{V_i(j\omega)}\right| = 0$$

At $\omega \to 0$, capacitor will be open circuited and inductor will be short circuited, circuit looks like



$$\left|\frac{V_0(j\omega)}{V_i(j\omega)}\right| = 1$$

So frequency response of the circuit will be



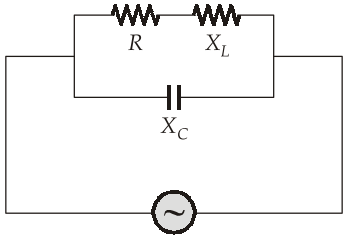
So the circuit is low pass filter.

35. (d)

$$V_{rms} = \sqrt{\frac{0^2 + (10)^2 + (20)^2}{3}} = \sqrt{\frac{100 + 400}{3}} = 12.9 \text{ V}$$

36. (c)

Consider the circuit,



$$Y_1 = \frac{1}{R + jX_L} = \frac{R - jX_L}{R^2 + X_L^2}$$

$$Y_2 = \frac{j}{X_C}$$

Admittance of the circuit,

$$Y = Y_1 + Y_2 = \frac{R}{R^2 + X_L^2} - j\left(\frac{X_L}{R^2 + X_L^2} - \frac{1}{X_C}\right)$$

At resonance the circuit is purely resistive,

$$Z = \frac{R^2 + X_L^2}{R}$$

and $$\frac{X_L}{R^2 + X_L^2} = \frac{1}{X_C}$$

$$X_L \cdot X_C = R^2 + X_L^2 = \frac{L}{C}$$

At resonance, $$Z = \frac{L}{CR} = \frac{0.2}{20 \times 100 \times 10^{-6}} = 100\ \Omega$$

37. (a)

Applying KVL to mesh-2,

$$-j10(I_2 - I_1) + j10I_2 = 0$$
$$j10I_1 = 0$$
$$I_1 = 0 \text{ A}$$

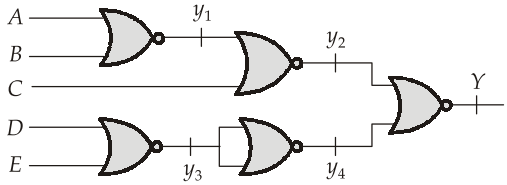
38. (a)

$$V_L = L\frac{di}{dt}$$

Under steady-state condition, current through inductor does not change with time

$\therefore V_L = 0$ and inductor acts as short circuit.

39. (a)



$$y_1 = \overline{A+B}, \quad y_2 = \overline{y_1 + C}$$
$$y_3 = \overline{D+E}, \quad y_4 = \overline{y}_3$$
$$y_2 = \overline{\overline{A+B}+C} = (A+B)\cdot\overline{C}$$
$$y_4 = \overline{\overline{D+E}} = D+E$$
$$y = \overline{y_2 + y_4} = \overline{(A+B)\cdot\overline{C}+D+E}$$
$$= \overline{(A+B)\cdot\overline{C}} + \overline{(D+E)}$$
$$= (\overline{A+B})\cdot C\cdot\overline{D}\cdot\overline{E}$$
$$= \overline{A}\,\overline{B}C\overline{D}\overline{E}$$

40. (c)

When two numbers are added in excess-3 code and the sum is less than 9, then in order to get the correct answer, we need to subtract 0110 i.e. $(6)_{10}$ from the sum.

41. (a)

$$\frac{2^{10}}{2} = 512 \text{ MUX}$$
$$\frac{512}{2} = 256 \text{ MUX}$$

$$\frac{256}{2} = 128 \text{ MUX}$$

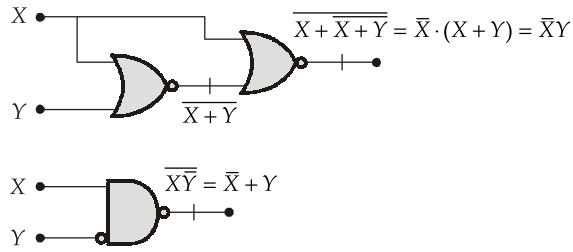
$$\vdots$$

$$\frac{2}{2} = 1 \text{ MUX}$$

Total number of MUX = 512 + 256 + 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1

= 1023

42. (d)



So both circuits are dual of each other.

43. (d)

Since toggle flip-flops are used, so at every clock pulse, Q_1Q_0 toggles (as $T = 1$)

	T	Q_1	Q_0	Q_1^+	Q_0^+
Clk-1 →	1	0	0	1	1
Clk-2 →	1	1	1	0	0
Clk-3 →	1	0	0	1	1
Clk-4 →	1	1	1	0	0

44. (d)

Here, every switch can be used as 1 bit. So, we are having 12 bits.

Now, each BCD number requires 4 bits. So in 12 bits, we can have 3 BCD number.

BCD No. 1	BCD No. 2	BCD No. 3	⇒	0 to 9	0 to 9	0 to 9

∴ Total BCD numbers = 10 × 10 × 10 = 1000 (000 to 999)

45. (a)

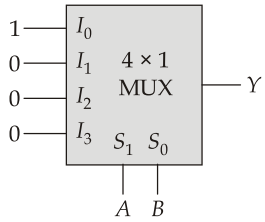
The range of integers that can be represented by n-bit 2's complement number system is -2^{n-1} to $2^{n-1} - 1$.

46. (b)

In a ring counter, to generate 'n' states, 'n' flip flops are required. Since it is a modulus 12 rings counter. Hence 12 flip-flops are required.

47. (a)

$$f = \bar{A}\bar{B}C + \bar{A}B\bar{C}$$
$$= \bar{A}\bar{B}(C + \bar{C})$$
$$= \bar{A}\bar{B}$$



Hence, one 2 × 1 multiplexer is required to realize the given function.

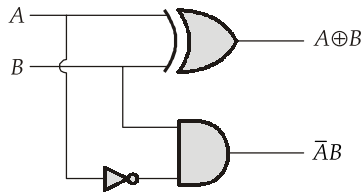
48. (a)

$$f = A + A\bar{B} + A\bar{B}C$$
$$= A(1 + \bar{B} + \bar{B}C) = A$$

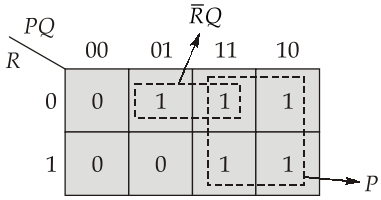
So, there is no need of NAND gate implement the given boolean function,
Since minimum number of NAND gates are asked.

49. (c)

For binary half-subtracter



50. (b)



$$f = P + \bar{R}Q$$

51. (a)

- SAR ADCs have a fixed conversion time of n-clock cycles, where 'n' is the number of bits.
- Counter type ADCs have the conversion time, proportional to input voltage magnitude.

52. (d)

For the given ADC, $n = 10$ bits and $V_{FS} = 5$ V

The maximum peak to peak ripple is equal to resolution,

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{5}{2^{10} - 1} = \frac{5}{10^{23}} \approx 5.0 \text{ mV}$$

53. (d)

$$\text{Step size} = R_F \times \left(\frac{5\text{V}}{8\text{k}\Omega}\right)$$

$$R_F = \frac{0.5 \times 8 \times 10^3}{5} = 800\ \Omega$$

55. (b)

Counter truth table:

b_3	b_2	b_1	b_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	**1**	0	0
0	**1**	0	1
0	**1**	1	0
0	**1**	1	1
1	0	0	0
1	0	0	1

$$\text{Duty cycle of } b_2 = \frac{4}{10} \times 100 = 40\%$$

56. (d)

$$N \le \frac{1}{f_{\max} \times t_{pd}} = \frac{1}{10 \times 10^6 \times 12 \times 10^{-9}} = \frac{100}{12}$$

$$N \le 8.33 \Rightarrow N = 8$$

So, MOD of counter $= 2^N = 2^8 = 256$.

57. (b)

$$f = \overline{\Sigma m(1,3,6)}$$

$$= \Sigma m(0, 2, 4, 5, 7)$$

58. (a)

When HOLD pin is activated by external signal, the microprocessor relinquishes control of buses and allows the external peripheral to use them.

59. (a)

The memory stores the binary information i.e. instruction and data.

61. (d)

IN belongs to peripheral I/O instruction categories.

62. (b)

$$\text{One T state time} = \frac{1}{f} = \frac{1}{4\,\text{MHz}} = 0.25\ \mu\text{sec}$$

Instruction cycle takes 12 T states

$\therefore$ Net instruction time,

$$12 \times 0.25 = 3\ \mu\text{sec}$$

63. (c)

Stack is a set of memory locations in R/W memory reserved for storing information temporarily during the execution of a program.

64. (d)

When RET instruction is executed the stack pointer is incremented by two.

65. (d)

All above mentioned addressing modes belong to 8085 microprocessor.

66. (a)

Instruction	T-state needed
LHLD (address-16)	- 16 T
STA (address-16)	- 13 T
PUSH rp	- 12 T
POP PSW	- 10 T

67. (c)

Among all five flags of 8085 microprocessor auxillary carry flag (AC) is used internally for BCD arithmetic and other four flags can be used by the programmer to check the conditions of the result of an operation.

68. (c)

There are no change in status of flag for MOV and MVI instructions.

ADD C and CMP instruction can change status of flag register.

69. (b)

It is one byte call to the memory address 0038 H.

70. (d)

TRAP is non maskable interrupt with highest priority.

71. (c)

It moves the content of accumulator to the memory address given by the register pair (*rp*).

72. (a)

SHLD is a mnemonic, which stands for store HL pair using direct addressing in memory location whose 16-bit address is denoted as *a*16. It is a 3-byte instruction.

73. (b)

ANI : AND Immediate
XRI : X-OR Immediate
} Logical operation

INR : Increment
ADI : Add Immediate
} Arithmetic operation

74. (c)

A Master-Slave flip-flop stores only 1-bit of information.

75. (d)

In masked ROM process, bit pattern is permanently recorded by the masking and metallization process.

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