



ISRO (Scientist/Engineer) Examination
Computer Science : Paper Analysis
Exam held on 12.01.2020

SI.	Subjects	No. of Qs.	Level of Difficulty
1	Programming and Data Structures	16	Moderate to high
2	Digital Logic	8	Moderate to high
3	Algorithms	5	Moderate
4	Operating System	9	Easy to moderate
5	Computer Networks	5	Easy
6	Databases	4	Moderate
7	Computer organization and	13	High
	Architecture		
8	Software Engineering and others	9	Easy to moderate
9	Discrete Mathematics	4	Easy
10	Theory of Computation	7	Easy

Page 2



# **ESE 2020** Streams : CE, ME, EE, E&T

Batches commencing from

Admission open

# Mains Classroom Course

**Conventional Questions Practice Programme** 

with ESE Mains Test Series

#### Features :

- 350 Hrs of comprehensive course.
- Classes by senior faculty.
- Classes in synchronization with Mains Test Series.
- Well design workbook for every subject.

Corporate office : 44-A/1, Kalu Sarai, New Delhi 🕓 011-45124612, 9958995830 / 🌐 WWW.Madeeasy.in



	INFORMATION IN THE AND A STREE AND A STREET
Q.4	<ul> <li>What is the availability of the software with following reliability figures.</li> <li>Mean Time Between Failures (MTBF) is 20 days</li> <li>Mean Time To Repair (MTTR) is 20 hours.</li> <li>(a) 90%</li> <li>(b) 96%</li> <li>(c) 24%</li> <li>(d) 50%</li> </ul>
Ans.	(d) Software availability = $\frac{\text{MTBF}}{(\text{MTBF} + \text{MTTR})} = \left(\frac{20}{20 + 20}\right) = 50\%$
Q.5	<ul> <li>What is the defect rate for Six sigma?</li> <li>(a) 1.0 defect per million lines of code</li> <li>(b) 1.4 defects per million lines of code</li> <li>(c) 3.0 defects per million lines of code</li> <li>(d) 3.4 defects per million lines of code</li> </ul>
Ans.	(d) End of Solution
Q.6	Consider a 5-segment pipeline with a clock cycle time 20 ns in each sub operation. Find out the approximate speed-up ratio between pipelined and non-pipelined system to execute 100 instructions. (If an average, every five cycles, a bubble due to data hazard has to be introduced in the pipeline) (a) 5 (b) 4.03 (c) 4.81 (d) 4.17
Ans.	(b) $ \begin{aligned} & \mathcal{K} = 5 \\ & \text{Clock time} = 20 \text{ ns} \\ & \text{Number of instructions} = 100 \\ & \text{Number of cycles taken by non-pipelined processor} = 100 \times 5 = 500 \\ & \text{Total inputs in the pipeline} = 100 + \frac{100}{5} = 120 \left[\frac{100}{5} = 20 \text{ stalls}\right] \\ & \text{Speed up} = \frac{(5 \times 100) \times 20 \text{ ns}}{(5 + 120 - 1) \times 20 \text{ ns}} = 4.03 \end{aligned} $
Q.7	Consider a 32-bit processor which supports 70 instructions. Each instruction is 32 bit long and has 4 fields namely opcode, two register identifiers and an immediate operand of unsigned integer type. Maximum value of the immediate operand that can be supported by the processor is 8191. How many registers the processor has? (a) 32 (b) 64 (c) 128 (d) 16
Corpora	te Office: 44-A/1, Kalu Sarai, New Delhi-110016   🖂 info@madeeasy.in   🕢 www.madeeasy.in Page 4





# **ESE** 2021 **GATE** 2021

# 1 Year/2Years **Classroom Courses**

Regular

Weekend

Early Start... • Extra Edge...

## BATCH COMMENCEMENT DATES

Delhi and	Noida	Rest of India
REGULAR BATCHES DELHI Evening : 16 <sup>th</sup> & 20 <sup>th</sup> Jan'20 Morning : 12 <sup>th</sup> & 18 <sup>th</sup> Feb'20	WEEKEND BATCHES DELHI 11 <sup>th</sup> Jan, 2020 NOIDA 12 <sup>th</sup> Jan, 2020	Patna : 24-02-2020 Lucknow : 20-02-2020 Bhopal : 16-01-2020 Indore : 20-02-2020 Pune : 20-01-2020 Hyderabad : 16-03-2020 Bhubaneswar : 23-01-2020 Kolkata : 25-01-2020 Jaipur : 16-02-2020

**(** 011-45124612, 9958995830

🌐 www.madeeasy.in

MADE EASY	India's Best Institute for IES, GATE & PSUs ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020
Ans.	<b>(b)</b> 32-bit processor. Number of instructions supported = 70
	Opcode Reg1 Reg2 Immediate operand
	Maximum value of immediate operand supported = 8191 which can be generated using 13 bits. For opcode = 7 bits are needed. Number of bits left to represents register bits = 12 i.e., 6 bits for 1 register. Hence, at max. 64 registers can be there. So, option (b) is correct.
Q.8	In a 8-bit ripple carry adder using identical full adders, each full adder takes 34 ns for computing sum. If the time taken for 8-bit addition is 90 ns, find time taken by each full adder to find carry. (a) 6 ns (b) 7 ns (c) 10 ns (d) 8 ns
Ans.	(d) n = 8 Ripple Carry Adder SUM delay from each Full Adder $S_{delay} = 34$ ns CARRY delay from each Full Adder $C_{delay} = ?$ Overall delay = $T = 90$ ns $T = S_{delay} + (n - 1)C_{delay}$ $90 = 34 + 7 \times C_{delay}$ $C_{delay} = 8$ ns
Q.9	Following Multiplexer circuit is equivalent to $\begin{array}{c} MUX \ data \\ input \ lines \\ \hline 0 \\ 1 \\ 2 \\ MUX \\ \hline 3 \\ 5 \\ 0 \\ \hline 3 \\ 5 \\ \hline 0 \\ \hline 1 \\ 2 \\ \hline 1 \\ \hline \\ 1$
Corpora	te Office: 44-A/1, Kalu Sarai, New Delhi-110016   🖂 info@madeeasy.in   🕄 www.madeeasy.in Page 5



	India's Best Institute for IES, GATE & PSUs	ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020
Ans.	(d) $\forall x[F(x) \rightarrow \forall y(E(y, x) \rightarrow b(y))]$ whenever x is a fish and if it is eater This translates to option (d), "only be	n by something, then that something is a bear. ears eat fish". End of Solution
Q.12	Following declaration of an array of s are 1, 2, 3 and 4 respectively. Alignment at an address divisible by $n$ . The fields to ensure alignment. All elements of Struct complx Short $s$ Byte $b$ Long $l$ Int $i$ End complx Complx C[10] Assuming $C$ is located at an address of (a) 150	Atruct, assumes size of byte, short, int and long of trule stipulates that <i>n</i> -byte field must be located is in a struct are not rearranged, padding is used array should be of same size. divisible by 8, what is the total size of <i>C</i> , in Bytes? (b) 160
Ans.	<ul> <li>(b)</li> <li>Size of complex data type will be 2</li> <li>But due to padding to align with rules s</li> <li>Hence, Total size = 16 × 10 =</li> </ul>	(d) 2+0 + 1 + 4 + 3 = 10 Bytes size becomes 16 Bytes (after 6 Bytes of padding) = 160 Bytes
Q.13	The immediate addressing mode can <b>1.</b> Loading internal registers with init <b>2.</b> Perform arithmetic or logical oper Which of the following is true? (a) Only 1 (c) Both 1 and 2	be used for ial values ation on data contained in instructions (b) Only 2 (d) Immediate mode refers to data in cache
Ans.	(c) The immediate addressing mode can be arithmetic operations. For example LOAD R1, #100. So, both the statements are correct.	e used for loading value in register and performed
Corpora	te Office: 44-A/1, Kalu Sarai, New Delhi-110016 \mid 📐	info@madeeasy.in   🜏 www.madeeasy.in Page 7



# **UPPSC** Assistant Engineer Examination, 2019 Total Posts : 692

# We are launching Comprehensive Classroom Course

at **DELHI & LUCKNOW** Centres

## Batches from **20<sup>th</sup> Jan, 2020 & 10<sup>th</sup> Feb, 2020** Streams Offered : CE, ME, EE

• 650 Hrs of comprehensive course. • General Studies and Hindi covered.

• Exclusive study materials as per requirement of UPPSC.

# Other courses available:



Useful for candidates who are not able to join Classroom Courses.

Technical books covering well illustrated theory with solved examples and previous solved papers. GS and Hindi also included.

Online test series on standard and pattern of UPPSC examination. Quality Questions with detailed solutions.

MADE EASY	India's Best Institute for IES, GATE & PSUs	ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020	D
Q.14	<ul> <li>Statements associated with registers of</li> <li>(a) The program counter holds the me</li> <li>(b) Only opcode is transferred to the o</li> <li>(c) An instruction in the instruction reg</li> <li>(d) The value of the program counter is to the memory address register.</li> </ul>	a CPU are given. Identify the false statement. mory address of the instruction in execution. control unit. ister consists of the opcode and the operand incremented by 1 once its value has been read	
Ans.	(c)	End of Solution	
Q.15	<ul> <li>Which of the following affects the proces other.</li> <li>1. Data bus capability</li> <li>2. Addressing scheme</li> <li>3. Clock speed</li> <li>(a) 3 only</li> <li>(c) 2 and 3 only</li> </ul>	<ul> <li>(b) 1 and 3 only</li> <li>(d) 1, 2 and 3</li> </ul>	
Ans.	(b)	End of Colution	
Q.16	Convert the pre-fix expression to in-fix $-^* + ABC^* - DE + FG$ (a) $(A - B)^*C + (D^*E) - (F + G)$ (c) $(A + B - C)^*(D - E))^*(F + G)$	(b) $(A + B)*C - (D - E)*(F - G)$ (d) $(A + B)*C - (D*E) - (F + G)$	
Ans.	<ul> <li>(*)</li> <li>Given Prefix operation:</li> <li>-* + ABC* - DE + FG</li> <li>Infix:</li> <li>(A + B)*C - (D - E)*(F + G)</li> <li>None of the option matches.</li> </ul>	End of Solution	
Corpora	te Office: 44-A/1, Kalu Sarai, New Delhi-110016   🔀	info@madeeasy.in   🔬 www.madeeasy.in Page 8	







National Through Scholarship

**BST** For ESE & GATE 202

## Scholarship applicable on Long Term Classroom Courses for ESE & GATE

Date of Test : 1<sup>st</sup> Mar, 2020

Valid on batches commencing from Apr-June, 2020

#### Students may opt any one of the following paper:

• Technical Paper : CE, ME, EE, EC, CS, IN

Avail upto

- 50 Questions; • 100 Marks; 1 Hour duration
- Aptitude Based Paper : Maths + Reasoning + English

🕓 09599946203, 09599946204 🛛 🖂 nst@madeeasy.in For registration, visit: www.madeeasy.in







# Rank Improvement Batches

## for **GATE 2021 & ESE 2021**

**Syllabus Covered** Complete GATE syllabus & Technical syllabus of ESE **Course Duration** Approximately 5 months 450-475 teaching hours

#### **Class Timing**

5-6 days a week 4 hours a day

## **Features :**

- Comprehensive problem solving sessions.
- Techniques to improve accuracy & speed.
- Doubt clearing sessions.
- Weekly class tests for performance improvement.
- Specially designed workbooks for technical subjects.
- Smart techniques to solve problems.
- Systematic & cyclic revision of all subjects.
- Inclusive of interview guidance for PSUs.

Batches commencing from Mid May, 2020 Admission Open

Corporate office : 44-A/1, Kalu Sarai, New Delhi 🕓 011-45124612, 9958995830

🕽 www.madeeasy.in









# **General Studies & Engineering Aptitude** for ESE 2021 Prelims

## BATCHES COMMENCEMENT DATES

Regular Batches Delhi 18<sup>th</sup> Feb, 2020 Weekend Batches Delhi & Noida 22<sup>nd</sup> Feb, 2020

🕓 011-45124612, 9958995830 🛛 🌐 www.madeeasy.in



	India's Best Institute for IES, GATE & PSUS ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020
Ans.	(c) Delete is DML command and can be rolled back (undo) TRUNCATE is DDL command and can not be rolled back.
Q.33	<ul> <li>Remote Procedure Calls are used for</li> <li>(a) communication between two processes remotely different from each other on the same system.</li> <li>(b) communication between two processes on the same system.</li> <li>(c) communication between two processes on separate system.</li> <li>(d) None of the above</li> </ul>
Ans.	(c) Remote procedure calls are used to communicate between process which are not in same address space mainly on different systems.
Q.34	Consider the following recursive C function that takes two arguments unsigned int rer (unsigned int <i>n</i> , unsigned int <i>r</i> ) { if $(n > 0)$ return $(n\% r + rer(n/r, r))$ ; else return 0; } What is the return value of the function rer when it is called as rer (513, 2)? (a) 9  (b) 8 (c) 5  (d) 2
Ans.	(d) 513% 2 + 256% 2 + 128% 2 + 64% 2 + 32% 2 + 16% 2 + 8%2 + 4%2 + 2%2 + 1%2 Hence, output will be $1 + 0 + 0 + 0 + 0 + 0 + 0 + 0 + 1 = 2$ , i.e., sum of bits when 513 represented in binary.
Q.35	A given grammar is called ambiguous if (a) two or more productions have the same non-terminal on the left hand side (b) a derivation tree has more than one associated sentence (c) there is a sentence with more than one derivation tree corresponding to it (d) brackets are not present in the grammar
Ans.	(c) A grammar to ambiguous if there is a sentence with more than one derivation tree corresponding to it.
Corport	to Office: 44.0/1 Kalu Sarai New Delbi 110016 - ↓ \\ Tipfe@madeeacu in ↓ Course madeeacu in Page 17
Corpora	te onice. 447, Vi in Sarai, New Denni-Froorio T Mino@madeeasy.in T S www.madeeasy.in



An initiative of **MADE EASY** Group



🔀 cst@nextia<u>s.com 🕓 8800338066</u>

www.nextias.com

<b>Q.36</b> W #ir int	hat is the output of the code given below?
{	<pre>nclude <stdio.h> t main()  char name[]="satellites"; int len; int size; len = strlen(name); size = sizeof(name); printf("%d", len * size); return 0;</stdio.h></pre>
(a) (c)	) 100 (b) 110 ) 40 (d) 44
Ans. (b	))
str ⇒ He	$\begin{bmatrix} s & a & t & e & 1 & 1 & t & e & s & t \\ len = strlen (name) \\ rlen returns length of string without null character. \\ len = 10 \\ Size = Size of (name) \\ = 11 \\ ence, 110 gets printed. \\ End of Solution$
Q.37 Cr (a) (b (c) (d	necksum field in TCP header is ) ones complement of sum of header and data in bytes ) ones complement of sum of header, data and pseudo header in 16 bit words ) dropped from IPv6 header format ) better than md5 or sh1 methods
Ans. (b Cł he	b) hecksum calculation in TCP header involves header, payload (data) and pseudo eader. All these values gets added and stored in one's complemented form.

г







# **GATE 2020** Online Test Series Stream : CE, ME, EE, EC, CS, IN, PI



- Newly designed quality questions as per standard of GATE.
- Video solutions by senior faculties.
- **B** Fully explained and well illustrated solutions.
- Comprehensive and detailed analysis report of test performance.

## PACKAGES

### **Complete Package**

- Part Syllabus Topicwise Tests : 24
- Single Subject Tests : 12
- Multi Subject Tests : 6
- Full Syllabus Tests : 12

## **Only Full Syllabus Tests**

12 TESTS

Full syllabus tests on standard & pattern on actual GATE exam.

### Test Series available on



Helpline no.: 98180 98817

TESTS

Register online at www.madeeasy.in

MADE EASY	ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020		
Q.43	An aid to determine the deadlock occurrence is(a) resource allocation graph(b) starvation graph(c) inversion graph(d) none of the above		
Ans.	(a)		
Q.44	Consider the following page reference string. 1 2 3 4 2 1 5 6 2 1 2 3 7 6 3 2 1 2 3 6		
	What are the minimum number of frames required to get a single page fault for the above sequence assuming LRU replacement strategy? (a) 7 (b) 4		
Ans.	(c) 6 (d) 5 (c)		
	Above question ambiguous but most probability option (c) should be the answer.		
Q.45	Three CPU-bound tasks, with execution times of 15, 12 and 5 time units respectively arrive at times 0, <i>t</i> and 8, respectively. If the operating system implements a shortest remaining time first scheduling algorithm, what should be the value of <i>t</i> to have 4 context switches? Ignore the context switches at time 0 and at the end. (a) $0 < t < 3$ (b) $t = 0$ (c) $t < = 3$ (d) $3 < t < 8$		
Ans.	(a)		
	ProcessATBT $P_1$ 015 $P_2$ t12 $P_3$ 85		
	Using SRTF, if $t = 2$		
	$\begin{array}{ c c c c c c }\hline P_1 & P_2 & P_3 & P_2 & P_1 \\ \hline 0 & 2 & 8 & 13 & 19 & 32 \\ \hline & & & & & & \\ \hline & & & & & & \\ \hline & & & &$		
	Hence, to have 4 context switches $t$ should be between $0 < t < 3$ .		
Q.46	End of Solution         The post-order traversal of a binary tree is ACEDBHIGF. The pre-order traversal is         (a) ABCDEFGHI       (b) FBADCEGIH         (c) FABCDEGHI       (d) ABDCEFGIH		
Ans.	(*)		
Ans.	(*) End of Solution		

MADE EASY	INTERESTINATION OF IES, GATE & PSUS ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020
Q.47	In linear hasing, if blocking factor bfr, loading factor $i$ and file buckets N are known, the number of records will be (a) $cr = i + bfr + N$ (b) $r = i - bfr - N$ (c) $r = i - bfr - N$ (d) $r = i * bfr * N$
Ans.	(d) End of Solution
Q.48	<ul> <li>What is compaction refers to</li> <li>(a) a technique for overcoming internal fragmentation</li> <li>(b) a paging technique</li> <li>(c) a technique for overcoming external fragmentation</li> <li>(d) a technique for compressing the data</li> </ul>
Ans.	<ul> <li>(c)</li> <li>Compaction is a process in which the free space is collected in a large memory chunk to make some space available for processes.</li> <li>In memory management, swapping creates multiple fragments in the memory because of the processes moving in and out.</li> <li>Compaction refers to combining all the empty spaces together and processes.</li> </ul>
Q.49	<ul> <li>The operating system and the other processes are protected from being modified by an already running process because</li> <li>(a) they run at different time instants and not in parallel</li> <li>(b) they are in different logical addresses</li> <li>(c) they use a protection algorithm in the scheduler</li> <li>(d) every address generated by the CPU is being checked against the relocation and limit parameters</li> </ul>
Ans.	(d)
Q.50	A grammar is defined as $A \rightarrow BC$ $B \rightarrow x   Bx$ $C \rightarrow B   D$ $D \rightarrow y   Ey$ $E \rightarrow z$ The non-terminal alphabet of the grammar is (a) {A, B, C, D, E} (b) {B, C D, E} (c) {A, B, C, D, E, x, y, z} (d) {x, y, z}
Corp <u>ora</u>	te Office: 44-A/1, Kalu Sarai, New Delhi-110016   🖂 info@madeeasy.in   🔊 www.madeeasy.in Page 22





MADE EASY	India's Best Institute for IES, GATE & PSUs ISRO : Computer Science Detailed Solutions : Exam held on 12.01.20
	$= (\overline{E}(1+AB+\overline{F})+AB\overline{F})(C+D+\overline{F})$ $= (\overline{E}+AB\overline{F})(C+D+\overline{F})$ End of Solution
Q.53	What is the in-order successor of 15 in the given binary search tree? $(15)$
	9 (a) 18
	(a) 18 (b) 8 (c) 17 (d) 20
Ans.	(c) Inorder successor of a node is the next node in inorder traversal of the binary search tree.
	OR It can be defined as the node with the smallest key greater than the key of input node Inorder traversal of given tree,
	17 is the inorder successor of 15.
Q.54	The minimum height of an AVL tree with <i>n</i> nodes is (a) Ceil $(\log_2 (n + 1))$ (b) 1.44 $\log_2 n$ (c) Floor $(\log_2 (n + 1))$ (d) 1.64 $\log_2 n$
Ans.	(c) If there are <i>n</i> nodes in AVL tree, minimum height is Floor $(\log_2 (n + 1))$ .
Q.55	The Master theorem (a) assumes the subproblems are unequal sizes (b) can be used if the subproblems are of equal size (c) cannot be used for divide and conquer algorithms (d) cannot be used for asymptotic complexity analysis
Ans.	(b) Master theorem is used for subproblems which are equal in size.
	End of Solution
Corporat	te Office: 44-A/1, Kalu Sarai, New Delbi-110016   🔀 info@madeeasy in   🕥 www.madeeasy in Page 24

WADE EASY	ISRO : Computer Science ISRO : Computer Science Detailed Solutions : Exam held on 12.01.202		
Q.56	Raymonds tree based algorithm ensures (a) no starvation, but deadlock may occur in rare cases (b) no deadlock, but starvation may occur (c) neither deadlock nor starvation can occur (d) deadlock may occur in cases where the process is already starved		
Ans.	(b) Raymonds algorithm ensures no deadlock will occur but can cause starvation.		
Q.57	Consider the following pseudo-code: I = 0; J = 0; K = 8; while (I < K - 1) //while-1 { J = J + 1; while (J < K) //while-2 { if (x[I] < x[J]) { temp = x[I]; x[I] = x[J]; x[J] = temp; } // end of while-2 I = I + 1; // end of while-1 The cyclomatic complexity of the above is		
	(a) 5 (c) 4 (d) 1		
Ans.	(c)		
Q.58	In a class definition with 10 methods, to make the class maximally cohesive, number of direct and indirect connections required among the methods are (a) 90, 0 (b) 45, 0 (c) 10, 10 (d) 45, 45		





MADE EASY	India's Best Institute for IES, GATE & PSUs	ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020	
Q.64	One instruction tries to write an operan may lead to a dependency called (a) True dependency (c) Output dependency	d before it is written by previous instruction. This (b) Anti-dependency (d) Control hazard	
Ans.	(c)	End of Solution	
Q.65	If every non-key attribute functionally dependant on the primary key, then the relation will be in		
	<ul><li>(a) First normal form</li><li>(c) Third normal form</li></ul>	<ul><li>(b) Second normal form</li><li>(d) Fourth normal form</li></ul>	
Ans.	<ul><li>(c)</li><li>Every non key attribute functional</li><li>According to 3NF inference rule e</li></ul>	ity dependent on primary key 3NF. every non key must determine by key. End of Solution	
Q.66	The SQL query SELECT columns FROM TableA RIGHT OUTER JOIN TableB ON A.columnName = B.columnName WHERE A.columnName IS NULL returns the following: (a) All rows in Table B, which meets equality condition above and, none from Table A, which meets the condition (b) All rows in Table A, which meets equality condition above and none from Table B, which meets the condition (c) All rows in Table B, which meets equality condition (d) All rows in Table A, which meets equality condition		
Ans.	(*) SELECT columns FROM TableA RIGHT OUTER JOIN TableB ON A.columnName = B.columnName WHERE A.columnName IS NULL Query returns records of table B which No option matching.	ch are failed equality condition of join. <i>End of Solution</i>	
Corpora	ate Office: 44-A/1, Kalu Sarai, New Delhi-110016 🏾   🔀	info@madeeasy.in   🜏 www.madeeasy.in Page 28	



www.madeeasy.in

	India's Best Institute for IES, GATE & PSUs	ISRO : Computer Science tailed Solutions : Exam held on 12.01.2020
Q.67 Ans.	To send same bit sequence, NRZ encodir (a) Same clock frequency as Manchester (b) Half the clock frequency as Manchest (c) Twice the clock frequency as Manche (d) A clock frequency which depend on m (b)	ng require encoding er encoding ster encoding umber of zeros and ones in the bit sequence
Q.68	The persist timer is used in TCP to (a) To detect crashes from the other end (b) To enable retransmission (c) To avoid deadlock condition (c) To timeout FIN_Wait1 condition	of the connection
Ans.	(c)	End of Solution
Q.69	An array of 2 two byte integers is stored in b below. What will be its storage pattern in Address Da $0 \times 104$ 7 $0 \times 103$ 5 $0 \times 102$ 3 $0 \times 101$ 1 (a) $0 \times 104$ 12 (b $0 \times 103$ 56 $0 \times 102$ 34 $0 \times 101$ 78 (c) $0 \times 104$ 56 (d $0 \times 103$ 78	big endian machine in byte address as shown little endian machine? ata 8 6 4 2 ) $0 \times 104$ 12 $0 \times 103$ 34 $0 \times 102$ 56 $0 \times 101$ 78 ) $0 \times 104$ 56 $0 \times 103$ 12
	$0 \times 100 - 70$ $0 \times 102 - 12$ $0 \times 101 - 34$	$0 \times 102$ 78 $0 \times 101$ 34
Ans.	(b) Big endian: 104 103 102 10 Big endian: 78 56 34 1 LB H	11 2 {lower address contain higher byte}
	104       103       102       100         Little endian:       12       34       56       7         HB       L	11 8 {lower address contain lower byte} 3 End of Solution
Corpora	ate Office: 44-A/1, Kalu Sarai, New Delhi-110016 🏾   🔀 info	@madeeasy.in   🕄 www.madeeasy.in Page 29



	ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020		
Q.73	<ul> <li>The language which is generated by the grammar S → aSa   bSb   a   b over the alphabet {a, b} is the set of</li> <li>(a) Strings that begin and end with the same symbol</li> <li>(b) All odd and even length palindromes</li> <li>(c) All odd length palindromes</li> <li>(d) All even length palindromes</li> </ul>		
Ans.	(c) The grammar $S \rightarrow aSa   bSb   a   b$ is the standard grammar for generating all the odd palindromes over the alphabet {a, b}.		
Q.74	Which of the following classes of languages can validate an IPv4 address in dotted decimal format? It is to be ensured that the decimal values are between 0 and 255(a) RE and higher(b) CFG and higher(c) CSG and higher(d) Recursively enumerable language		
Ans.	(a) As per given options (a) is most suitable		
Q.75	Minimum number of states required in DFA accepting binary strings not ending in "101" is (a) 3 (b) 4 (c) 5 (d) 6		
Ans.	(b) First design the DFA for ending with "101" as shown below: $\int_{0}^{0} \int_{0}^{1} \int_{0}^{1} \int_{1}^{0} \int_{1}^{1} \int$		
	End of Solution		

	MADE EASY ndia's Best Institute for IES, GATE & PSUs	ISRO : Computer Science Detailed Solutions : Exam held on 12.01.2020				
Q.76	Which of the following is a type of a out-of-order execution, with the reordering done					
	by a compiler	(b) dead code elimination				
	(c) strength reduction	(d) software pipelining				
Ans.	(a)					
	End of Solution					
Q.77	A stack organised computer is characterised by instructions with (a) indirect addressing (b) direct addressing					
	(c) zero addressing	(d) index addressing				
Ans.	(c)					
		End of Solution				
Q.78	A computer which issues instructions in order, has only 2 registers and 3 opcodes ADD, SUB and MOV. Consider 2 different implementations of the following basic block:					
	Case 1	Case2				
	t1 = a + b;	t2 = c + d;				
	t2 = c + d;	t3 = e - t2;				
	t3 = e - t2; t4 = t1 - t2:	t1 = a + b; t4 = t1 - t2				
	<ul><li>Assume that an operands are initial to reside in memory. Which one is bell MOV instructions?</li><li>(a) Case 2, 2</li><li>(c) Case 1, 2</li></ul>	<ul> <li>(b) Case 2, 3</li> <li>(d) Case 1, 3</li> </ul>				
Ans.	(*)					
		End of Solution				
Q.79	Which one indicates a technics of k (a) Beta cross	building cross compilers?				
	(c) Mexican cross	(d) X-cross				
Ans.	(b)					
		End of Solution				
Corporat	e Office: 44-A/1, Kalu Sarai, New Delhi-110016	⊠ info@madeeasy.in   💽 www.madeeasy.in Page 32				

	<b>MADE EASY</b> India's Best Institute for IES, GATE & PSUs	ISRO : Computer Sci Detailed Solutions : Exam held of	ence n 12.01.2020
Q.80	Consider a 2-dimensional array $x$ with a value equivalent to the product of major format. If the first element $x[0][0]$ and each element occupies only one will be holding a value of 10? (a) 1018, 1019 (c) 1013, 1014	n 10 rows and 4 columns, with each elen row number and column number. The D] occupies the memory location with ac e memory location, which all locations ( (b) 1022, 1041 (d) 1000, 1399	nent storing e array row- ldress 1000 (in decimal)
Ans.	(b)		d of Solution
Corporat	te Office: 44-A/1, Kalu Sarai, New Delhi-110016	🔀 info@madeeasy.in   📀 www.madeeasy.in	Page 33