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Important Questions for GATE 2022

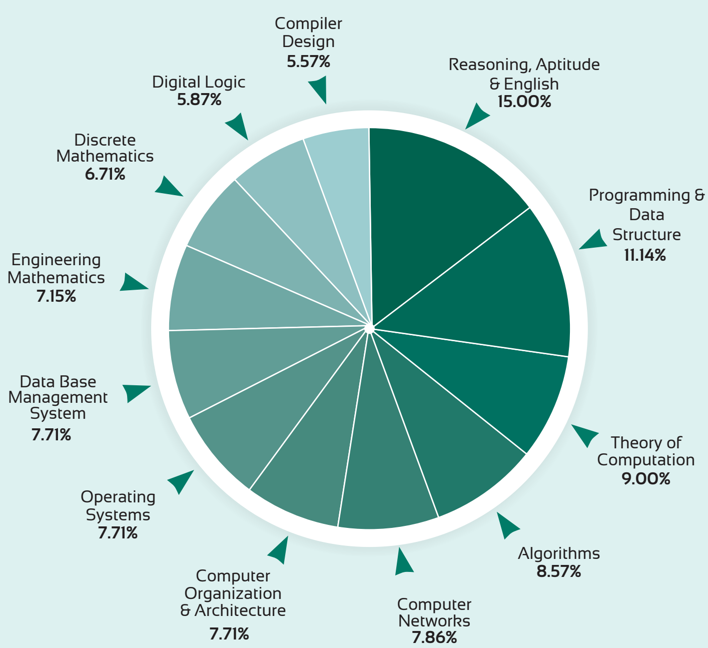
COMPUTER SCIENCE & IT

Day 7 of 8

Q.151 - Q.175 (Out of 200 Questions)

Computer Organization & Architecture + Digital Logic

SUBJECT-WISE WEIGHTAGE ANALYSIS OF GATE SYLLABUS



Subject	Average % (last 5 yrs)
Reasoning, Aptitude & English	15.00%
Programming & Data Structure	11.14%
Theory of Computation	9.00%
Algorithms	8.57%
Computer Networks	7.86%
Operating Systems	7.71%
Computer Organization & Architecture	7.71%
Data Base Management System	7.71%
Engineering Mathematics	7.15%
Discrete Mathematics	6.71%
Digital Logic	5.87%
Compiler Design	5.57%
Total	**100%**

Computer Organization & Architecture + Digital Logic

Q.151 A microprogrammed control unit is required to generate a total of 25 control signals. Assume that during any micro-instruction atmost one control signal is active. Find the minimum number of bits required in the control word to generate the required control signal.

Q.152 Which of the following is true about TLB?

(*i*) Tag entry in TLB contains a virtual page number and each data entry of the TLB holds a physical page number.

(*ii*) TLB misses can be handled either in hardware or in software.

(*iii*) TLB miss or a page fault requires using the exception mechanism.

(a) Only (*i*) and (*ii*)
(b) Only (*ii*) and (*iii*)
(c) Only (*iii*)
(d) All of the above

Q.153 A CPU, which addresses the data through its 5 registers in one of 14 different modes, is to be designed to support 10 arithmetic instructions, 15 logic instructions, 20 data moving instructions and 10 branch instructions of these instructions 20%, 60%, 60% and 50% are respectively either single-operand or zero operand instructions and rest of them are double operand type. What is the minimum size of CPU instruction word?

(a) 18
(b) 19
(c) 20
(d) 21

Q.154 Consider a system such that the number of clock cycles for a polling operation (including transferring to the polling routine, accessing the device and restarting the user program) is 400 cycles, and that the processor executes with a 500 MHz clock. Determine the fraction of CPU consumed when the mouse must be polled 30 times per second.

(a) 0.002%
(b) 0.02%
(c) 0.2%
(d) None of these

Q.155 Consider a system in which DMA technique is used to transfer 32 MB of data from an I/O device into memory. The bandwidth of I/O device is 256 KB/s. Once the data is filled into interface buffer, the DMA controller takes over the bus and transfer it to main memory in 28 sec. What percentage of the time is the CPU in blocked mode (approximately)?

(a) 18
(b) 82
(c) 35
(d) 45

Q.156 Given that 4 GB and 2 MB are the respective sizes of main memory and cache. Find the most appropriate tag bit length. Assume the block size is same in both cache and main memory and direct mapping is used with byte addressable memory.

(a) 10
(b) 11
(c) 12
(d) 13

Q.157 A 5 stage pipelined processor has IF, ID, EXE, MEM and WB. WB stage operation is divided into two parts. In the first part register write operation and in the second part register read operation is performed. The latencies of all those stages are 300, 400, 500, 500 and 300 (in nano second) respectively. Consider the following code is executed on this processor

I_1 : ADD R_3, R_2, R_4 ; $R_3 \leftarrow R_2 + R_4$

I_2 : SUB R_6, R_4, R_3 ; $R_6 \leftarrow R_4 - R_3$

I_3 : ADD R_7, R_5, R_3 ; $R_7 \leftarrow R_5 + R_3$

I_4 : SUB R_1, R_7, R_4 ; $R_1 \leftarrow R_7 - R_4$

Find minimum number of nop instructions (no operation) to eliminate hazards without using operand forwarding. (Assume each instruction takes one cycle to complete its operation in every stage)

Q.158 An instruction pipeline consist of 4 stages IF, ID, EX and WB. Four instructions need these stages for different number of cycles as shown by the table below:

Instruction	# Cycle needed for			
	IF	ID	EX	WB
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1

Find number of clock cycles needed to execute the above 4 instructions.

(a) 12 (b) 13

(c) 14 (d) 15

Q.159 Consider a pipeline 'x' consist of 5 stages named as IF, ID, OF, EX and WB with the respective stage delays of 2 ns, 5 ns, 6 ns, 8 ns and 1 ns. The alternative pipeline 'y' contain the same number of stages but EX stage is divided into 4 sub stages, (EX1, EX2, EX3 and EX4) with equal delay i.e. (8 ns/4) and ID stage is divided into 2 substages (ID1 and ID2) with equal delays of (5 ns/2). In the pipeline x and y memory reference instructions are not overlapped so the penalty of memory reference instructions in the pipeline 'x' is 4 cycles and in the pipeline 'y' is 8 cycles. If the program contain 30% of the instructions which are memory based instructions, what is the ratio of speedup of x to speedup of y?

Q.160 Consider execution of 100 instructions on a 5 stage pipeline. Let P be the probability of an instruction being a branch. What must be the value of P such that speed up is atleast 4?

(Assume each stage takes 1 cycle to perform it's task and branch is predicted on fourth stage of the pipeline)

Q.161 A Hypothetical control unit supports 5 groups of mutually exclusive signals:

Group	G_1	G_2	G_3	G_4	G_5
Control Signal	2	1	4	33	25

What is the size of control memory (in bytes), if vertical programming is used, assume control unit support 256 control word memory?

(a) 704 bytes
(b) 736 bytes
(c) 746 bytes
(d) 814 bytes

Q.162 Consider the following piece of code:

```
int x = 0, y = 0;
int i;          // x, y, i are in register
int A[4096];    // A is in memory at address 0x 10000
for (i = 0; i < 1024; i++) {
    x+ = A[i];
}
for (i = 0; i < 1024; i++) {
    y+ = A[i + 2048];
}
```

Assume that the system has a 2^{13} byte, direct-mapped data cache with 16-byte blocks. Assuming that the cache starts out empty, also Assume that an iteration of a loop in which the load hits takes 10 cycles but that an iteration of a loop in which the load misses takes 100 cycles. What is the execution time (cycles) of this snippet with the mentioned cache?

[**Note:** Assume integer size = 4 byte]

(a) 66556
(b) 66560
(c) 66500
(d) 66548

Q.163 Consider a RISC processor with an ideal CPI, where 25% of the total instructions are load and store instruction. Time to accessing main memory is 100 clock cycles and accessing of the cache memory required 2 clock cycles. If cache miss rate is 2%, then the effective CPI for the system with the cache is ________. [Upto 2 decimal placed]

Q.164 Consider two level cache hierarchies with L_1 and L_2 cache. Programs refer memory 1000 times, out of which 40 misses are in L_1 cache and 10 misses are in L_2 cache. If the miss penalty of L_2 is 200 clock cycles, hit time of L_1 is 1 clock cycle, and hit time of L_2 is 15 clock cycles, the average memory access time is ________ clock cycles. (Upto 1 decimal place)

Q.165 Consider Prof. Vamshi's writes a program given below and run on system which has 2-way set associative 16 KB data cache with 32 bytes block where each word size is 32 bits and LRU replacement policy used. If base address of array '*a*' is 0 × 0 and initially cache is empty then the number of data cache misses are there ________. (Assume integer takes 8 bytes)

```
int i, a[1024 * 1024], x = 0;
    for (i = 0; i < 1024; i++) {
        x + = a[i] + a[1024* i];
}
```

Q.166 An *X*-*Y* flip-flop, whose characteristic table is given below is to be implemented using a *J*-*K* flip-flop:

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q_n}$
1	1	0

This can be done by making

(a) $J = X, K = \overline{Y}$
(b) $J = \overline{X}, K = Y$
(c) $J = Y, K = \overline{X}$
(d) $J = \overline{Y}, K = X$

Q.167 If $Y = \overline{ABC + \overline{A}\overline{B}} + BC$ then dual and compliment of Y are respectively

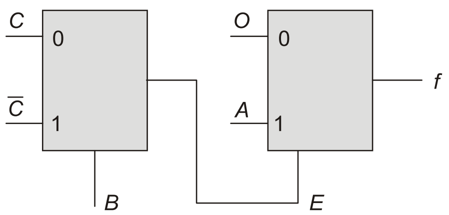
(a) $(ABC + \overline{A}\overline{B}) \cdot (B + C)$ and $\left[(\overline{A + B + C}) + (\overline{A} + \overline{B})\right] \cdot BC$

(b) $\left[(A + B + C + \overline{A} \cdot \overline{B})\right] \cdot \overline{BC}$ and $\left[ABC + (\overline{A + B})\right] \cdot \overline{BC}$

(c) $\left[(\overline{A + B + C}) + (\overline{\overline{A} + \overline{B}})\right] \cdot (B + C)$ and $(ABC + \overline{A}\overline{B}) \cdot \overline{BC}$

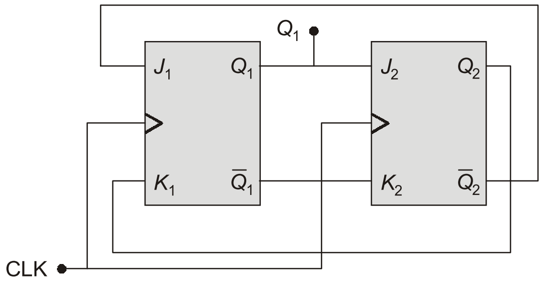
(d) $\left[\overline{ABC} + \overline{\overline{A} + B}\right] \cdot \overline{BC}$ and $\left[(A + B + C) + \overline{\overline{A}\overline{B}}\right] \cdot BC$

Q.168 The Boolean function *f* implemented in the figure using two input multiplexers is



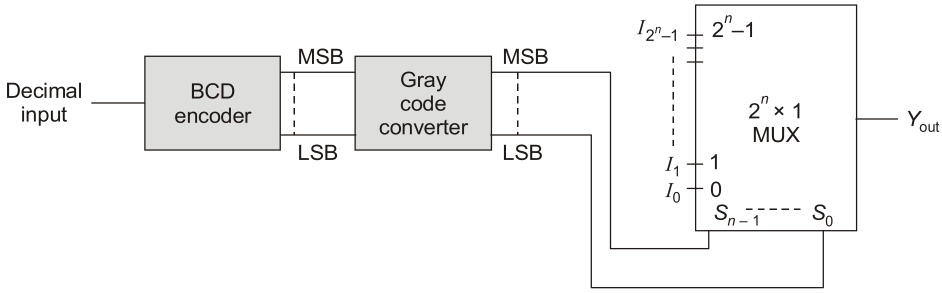
(a) $A\overline{B}C + AB\overline{C}$
(b) $ABC + A\overline{B}\overline{C}$
(c) $\overline{A}BC + \overline{A}\overline{B}\overline{C}$
(d) $\overline{AB}C + \overline{A}B\overline{C}$

Q.169 The outputs of both the flip-flops Q_1 and Q_2 in the figure shown below are initialized to 0. The sequence generated at Q_1 upon application of clock signal is



(a) 01110…
(b) 01010…
(c) 00110…
(d) 01100…

Q.170 Consider the circuit given below:



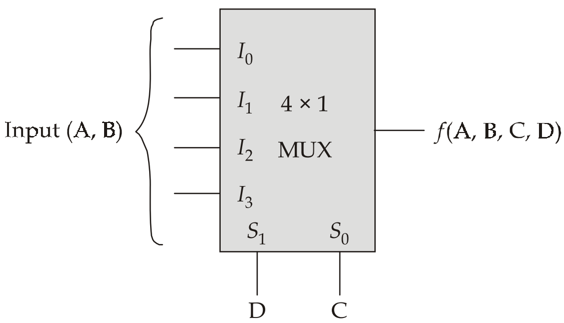
If the decimal input is 92 then Y_{out} corresponds to I_m, then value of m is ________.

Q.171 Minimum number of 2-input NOR Gates required to implement the function.

$$f = \overline{\bar{A} + \left[B + \bar{C}\left(\overline{AB + A\bar{C}}\right)\right]}$$

Q.172 The maximum number of boolean expressions that can be formed for the function $f(x, y, z)$ satisfying the relation $f(\bar{x}, y, \bar{z}) = f(x, y, z)$ is

Q.173 A 4 × 1 MUX is used to realize a 4-variable function, $f(A, B, C, D) = \Sigma m\ (0, 3, 4, 8, 9, 15)$. The inputs to the MUX are from variables A and B, then the input to the MUX from I_0 to I_3 respectively are



(a) $\bar{A} + \bar{B},\ 0,\ A\bar{B},\ A \odot B$
(b) $\bar{A},\ 0,\ \bar{A}B,\ A \oplus B$
(c) $\bar{A}\bar{B},\ 0,\ A\bar{B},\ A \odot B$
(d) $\bar{A} + \bar{B},\ 1,\ A\bar{B},\ A \oplus B$

Q.174 Which of the following is not true?

(a) The r's complement of a positive number N in base r is $(r^n - N)$.

(b) The $(r - 1)$'s complement of a positive number N in base r is $(r^n - N - 1)$.

(c) The $(r - 1)$'s complement of a positive number N having n digits and m digits in integer and fraction respectively in base r is $(r^n - r^{-m} - N)$.

(d) The $(r - 1)$'s complement of a positive number N having n digit and m digits in integer and fraction part respectively in base r is $(r^n - r^m - N)$.

Multiple Select Question (MSQ)

Q.175 Zero has two representations in:

(a) Sign magnitude
(b) 1's complement
(c) 2's complement
(d) Floating point representation.

■■■■

Detailed Explanations

151. (5)

Since none or one control signal is active at a time it is the case of vertical programming.

Number of bits required to generate control signals.

$$= \lceil \log_2 (25) \rceil = 5$$

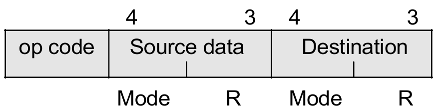
152. (d)

A TLB miss can be handled in software or hardware because it will require only a short sequence of operations to copy a valid page table entry from memory into TLB. (MIPS traditionally handles TLB miss in software).

Handling a TLB miss or a page fault requires using the exception mechanism to interrupt the active process, transfer control to the OS (operating system) and later resuming execution to interrupted process.

So (*i*), (*ii*) and (*iii*) are correct.

153. (b)



$$\text{Register} = 5 = 3 \text{ bits}$$
$$\text{Modes} = 14 = 4 \text{ bits}$$

Type	Single operand or no operand	Double operand
Arithmetic (10)	2	8
Logic (15)	9	6
Data moving (20)	12	8
Branch (10)	5	5

Total 27 double operands = 5 bits

Size of instruction word = 5 + 7 + 7 = 19

154. (a)

Clock cycle for polling 30 times = 30 × 400 = 12000 cycles per second.

$$1 \text{ processor cycle time} = \frac{1}{500 \times 10^6}$$

$\therefore$ Total poll time = 12000 × 1 processor cycle time

$$= 12000 \times \frac{1}{500 \times 10^6} = 2.4 \times 10^{-5}$$

$$\therefore \quad \text{Fractions} = \frac{2.4 \times 10^{-5}}{1} \times 100 = 0.0024\%$$

155. (a)

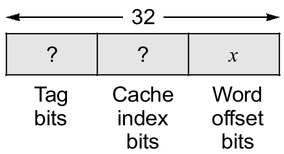
Time taken by I/O device to place data in buffer = $\frac{32\text{ MB}}{256\text{ KB}} = 128\,\text{sec}$

Percentage of time CPU blocked $\frac{28}{128+28} \times 100 = 17.94\%$

156. (b)

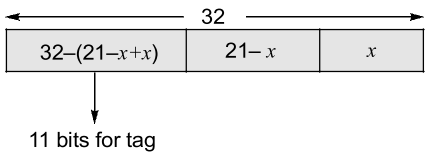
Assume each block contains 2^x words or bytes

$\therefore$ x bits as word offset.



Number of blocks in cache = $\frac{2^{21}}{2^x} = 2^{21-x}$

$\therefore$ $(21 - x)$ bits for indexing



157. (4)

Stages	1	2	3	4	5	6	7	8	9	10	11	12
WB					I_1			I_2	I_3			I_4
MEM				I_1			I_2	I_3			I_4	
EX			I_1			I_2	I_3			I_4		
ID		I_1	I_2	–	–	I_3	I_4	–	–			
IF	I_1	I_2	I_3	–	–	I_4						

Clock Cycle

Since I_1 and I_2 are dependent. So I_2 will enter into execute stage when I_1 completes WB stage. It creates 2 nop. Similarly I_3 and I_4 are dependent. They create 2 nop.
Total 4 nop instructions are required to eliminate hazards.

158. (b)

Stages of Pipeline	1	2	3	4	5	6	7	8	9	10	11	12	13
WB					I_1			I_2			I_3	I_3	I_4
EX				I_1		I_2	I_2	I_3	I_3	I_3	I_4	I_4	
ID		I_1	I_1	I_2	I_2	I_3	–	I_4	I_4	I_4			
IF	I_1	I_2	–	I_3	I_3	I_4	–						

Number of Clock Cycles

159. (1.159) [1.15 to 1.16]

Considering for large number of instruction:

$$S_x = \frac{\text{Average\_instruction\_time\_unpipelined}}{\text{Average\_instruction\_time\_pipelined}}$$

$$= \frac{\text{Sum of all stage delays}}{(1 + \text{Frequency} \times \text{Number of stalls per instruction}) \times \text{Delay time for largest stage}}$$

{Here considering sequencial execution of pipeline stages for *sum of all stage delays*}

$$S_x = \frac{22}{[1+(0.3\times 4)]\times 8} = 1.25$$

$$S_y = \frac{22}{[1+(0.3\times 8)]\times 6} = 1.078$$

$$\frac{S_x}{S_y} = 1.159$$

160. (0.08) [0.08 to 0.09]

$$\text{Speed up} = \frac{\text{Pipeline depth}}{(1 + \text{Branch frequency} \times \text{Branch penalty})} \geq 4$$

$$\frac{5}{1+P\times 3} \geq 4$$

$$4 + 12P \leq 5$$

$$12P \leq 1$$

$$P \leq \frac{1}{12}$$

161. (b)

Number of bits for control signals in vertical programming:

$$\log_2(2) + \log_2(1) + \log_2(4) + \log_2(33) + \log_2(25)$$
$$= 1 + 1 + 2 + 6 + 5 = 15 \text{ bits}$$
$$256 \text{ CW} = 8 \text{ bits}$$

VCW:

Branch condition	Flag	Control field	Control memory address
		15	8

$$\text{VCW size} = 15 + 8 = 23 \text{ bits}$$

Vertical control memory size = 256 × 23 bits

$$= \frac{256 \times 23}{8} \text{ bytes} = 736 \text{ bytes}$$

162. (b)

Cache is a direct mapped one.

For the first loop: one in 4 elements causes a miss.

Sequence: M, H, H, H, M, H, H, H, M, ...

$$\text{Number of misses} = \frac{1024}{4} = 256$$
$$\text{Number of hits} = 768$$

For the second loop: 2048 × 4 = 8192 bytes which is the capacity of the direct mapped cache.

Therefore A[i + 2048] is again mapped starting from 0 onwards.

So the sequence is same above: Miss, H, H, H, M, H, H, H, M, …

$$\text{Number of misses} = \frac{1024}{4} = 256$$
$$\text{Number of Hits} = 768$$
$$\text{Total Number of misses} = 512$$
$$\text{Number of hits} = 1536$$
$$\text{Total Execution Time} = 10 \times 1536 + 100 \times 512 = 66560 \text{ cycles}$$

163. (5.00) [4.95 to 5.05]

LOAD and STORE take 2 memory access, 1 for IF and 1 for loading/storing.

So total memory access for 100 instruction

$= 100 \text{ (IF)} + 1 \times 0.25 \times 100 \text{ (loading/storing)}$

$= 100 + 25 = 125$ memory access

Average memory access/instruction

$= \frac{125}{100} = 1.25$ memory access/instruction

Cycles per instruction for handling cache misses

= Memory accesses per instruction × Miss rate × Cycles per miss

$= 1.25 \times 0.02 \times 102$

$= 2.55$ Cycles per instruction

Cycles per instruction for handling cache hits

= Memory accesses per instruction × Hit rate × Cycles per hit

$= 1.25 \times 0.98 \times 2$

$= 2.45$ Cycles per instruction

Effective CPI = Cycles for hits + Cycles for misses

$= 2.55 + 2.45 = 5$

164. (3.6)

L_1 miss rate $= \frac{40}{1000} = 4\%$

L_2 miss rate (we need to take local miss rate) $= \frac{(10)}{40} = 25\%$

Average access time = Hit time (L_1) + Miss rate (L_1) [Hit time (L_2) + Miss rate (L_2) × Miss penalty]

$= 1 + 4\% \, [15 \text{ cc} + 25\% \times 200 \text{ cc}]$

$= 1 + 0.04 \, [15 \text{ cc} + 50 \text{ cc}]$

$= 3.6$ cc

165. (1279)

$$\text{Cache size} = 16 \text{ KB}$$
$$\text{Block size} = 32 \text{ B}$$

$$\text{Number of lines (Blocks)} = \frac{16 \text{ KB}}{32 \text{ B}} = \frac{2^{14}\text{B}}{2^5\text{B}} = 2^9$$

Since 2-way set associative,

So, $\text{Number of sets} = \frac{2^9}{2} = 2^8$

← 32 →

TAG	Sets	Block offset
19	8	5

Set 0	0 – 31 0	1024 – 1055 1
Set 1	32 – 63 0	1056 – 1087 1
Set 2	64 – 95 0	1
⋮	⋮	⋮
Set 255	0	1

1. **First access:** $\overset{\text{Miss}}{a[0]} + \overset{\text{Hit}}{a[0]}$, since $a[0]$ is miss, $a[0]$, $a[1]$, $a[2]$ and $a[3]$ are fetched to mem. Since word size is 32 bits, so 4 integer are fetched on a miss.
2. **Second access:** $\overset{\text{Hit}}{a[1]} + \overset{\text{Miss}}{a[1024]}$
3. **Third access:** $\overset{\text{Hit}}{a[2]} + \overset{\text{Miss}}{a[2048]}$

Like this, total number of miss $= \frac{1024}{4} + (1024 - 1) = 256 + 1023 = 1279$

166. (d)

X - *Y* truth table

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q_n}$
1	1	0

J - *K* truth table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Excitation table

$Q(t)$	$Q(t+1)$	J	K	X	Y
0	0	0	×	×	1
0	1	1	×	×	0
1	0	×	1	1	×
1	1	×	0	0	×

To make $(X - Y)$ FF using $(J - K)$ FF, (J) should be $(\overline{Y})$ and (K) should be (X).

167. (c)

$$Y = \overline{ABC+\bar{A}\bar{B}}+BC$$

Dual of Y

$$Y_d = \overline{(A+B+C)\cdot(\bar{A}+\bar{B})}\cdot(B+C)$$

$$= \left[\overline{(A+B+C)}+\overline{(\bar{A}+\bar{B})}\right]\cdot(B+C)$$

Compliment of Y

$$Y_c = \overline{\overline{(ABC+\bar{A}\bar{B})}+BC}$$

$$= \overline{\overline{(ABC+\bar{A}\bar{B})}}\cdot\overline{BC} = (ABC+\bar{A}\bar{B})\cdot\overline{BC}$$

168. (a)

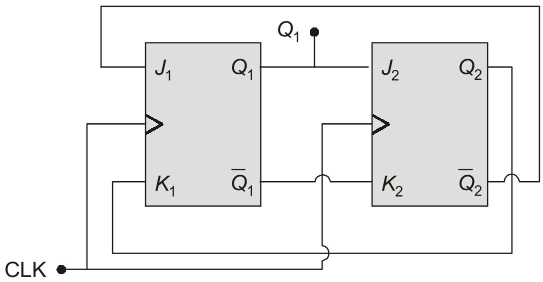
$$f = E.A$$

$$E = \bar{B}C+B\bar{C}$$

$\therefore$ $$f = A\bar{B}C+ABC\bar{C}$$

A	B	C	f
1	0	1	1
1	1	0	1

169. (d)



Initially $Q_1 = Q_2 = 0$

Truth table of *JK*:

J	K	Q_n
0	0	Previous state
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Case-1: 1st clock pulse

$$Q_1 = 0,\ \bar{Q}_1 = 1, Q_2 = 0, \bar{Q}_2 = 1$$

So, $$J_1 = 1,\ K_1 = 0 \text{ and } J_2 = 0,\ K_2 = 1$$

So $$Q_1^+ = 1,\ Q_2^+ = 0 \qquad \text{(New values of } Q_1 \text{ and } Q_2\text{)}$$

Case-2:

$$Q_1 = 1,\ Q_2 = 0$$
$$\bar{Q}_1 = 0,\ \bar{Q}_2 = 1$$

So, $J_1 = 1,\ J_2 = 1$

$$K_1 = 0\ \ K_2 = 0$$

So, $Q_1^+ = 1,\ Q_2^+ = 1$ (New values of Q_1 and Q_2)

Case-2:

$$Q_1 = 1,\ \bar{Q}_1 = 0, Q_2 = 1, \bar{Q}_2 = 0$$
$$J_1 = 0, K_1 = 1, J_2 = 1, K_2 = 0$$
$$Q_1^+ = 0,\ Q_2^+ = 1$$ (New values of Q_1 and Q_2)

So, the sequence will be 01100.

170. **(219)**

Decimal input = 92

BCD = 10010010

Output of Gray code converter = 11011011

Y_0 corresponds to I_m with (S_n ...... S_0) is = $(11011011)_2$

m = 219

171. **(3)**

$$f = \overline{\bar{A} + \left[\overline{B + \bar{C}(\overline{AB + A\bar{C}})}\right]}$$

$$= A \cdot \left[B + \bar{C}(\overline{AB + A\bar{C}})\right]$$ **[Demorgan's Law]**

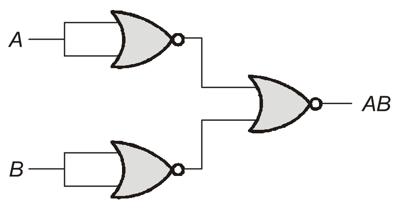
$$= A \cdot \left[B + \bar{C}(\overline{AB} \cdot \overline{A\bar{C}})\right]$$ **[Demorgan's Law]**

$$= A \cdot \left[B + \bar{C}(\bar{A} + \bar{B})(\bar{A} + C)\right]$$ **[Demorgan's Law]**

$$= A\left[B + \bar{C}(\bar{A} + \bar{B}C)\right]$$ **[Distributive property]**

$$= A\left[B + \bar{A}\bar{C}\right] = AB + A\bar{A}\bar{C}$$

$$= AB$$ (AND gate to be implemented)



⇒ Minimum number of NOR gate required = 3

172. (16)

For every combination of x, y, z the function value remains same for input $\bar{x}, y, \bar{z}$.

$x\ y\ z$	$f(x,y,z) = f(\bar{x},y,\bar{z})$
0 0 0 1 0 1	either 0 or 1
0 0 1 1 0 0	either 0 or 1
0 1 0 1 1 1	either 0 or 1
0 1 1 1 1 0	either 0 or 1

Effectively there are only four rows for the truth table of the function $f(x, y, z)$.

∴ Total Boolean expressions possible is $2^4 = 16$.

173. (a)

The input can be determined by constructing the table as below for function $f(A, B, C, D)$.

Now,

$$I_0 = \bar{A}\bar{B} + \bar{A}B + A\bar{B}$$
$$= \bar{A}(B + \bar{B}) + A\bar{B}$$
$$= \bar{A} + A\bar{B}$$
$$= \bar{A} + \bar{B}$$
$$I_1 = 0$$
$$I_2 = A\bar{B}$$
$$I_3 = \bar{A}\bar{B} + AB = A \odot B$$

	$\bar{C}\bar{D}$ I_0	$C\bar{D}$ I_1	$\bar{C}D$ I_2	CD I_3
$\bar{A}\bar{B}$	(0)	2	1	(3)
$\bar{A}B$	(4)	6	5	7
$A\bar{B}$	(8)	10	(9)	11
AB	12	14	13	(15)
	$\bar{A}+\bar{B}$	0	$A\bar{B}$	$A \odot B$

174. (d)

175. (a, b, d)

Zero has two representation in sign's magnitude:

1 – MSB is 0

2 – MSB is 1

Both of these representation have equal value that is 0.

Also zero have two representation in 1's compliments:

1 – All bits are Zero.

2 – All bits are 1

IEEE 754 floating point also have 2 representation for zero.

■■■■