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Prelims Through Questions

for

ESE 2021

Electronics & Telecommunication

Day 3 of 11

Q.91 - Q.140

(Out of 500 Questions)

Control Systems + Microprocessor & Microcontroller

Control Systems + Microprocessor & Microcontroller

Q.91 The transfer function of three blocks connected in cascade is given by $\frac{(s+1)}{s(s+2)(s+3)}$. If block 1 has transfer function of $\frac{1}{s(s+2)}$ and block 2 has transfer function of $\frac{(s+2)}{(s+3)}$ then the transfer function of the 3rd block is

(a) $(s+1)(s+2)$ (b) $\frac{(s+1)}{(s+2)}$

(c) $\frac{(s+1)}{s(s+3)}$ (d) $\frac{(s+1)^2}{(s+2)^2}$

91. (b)

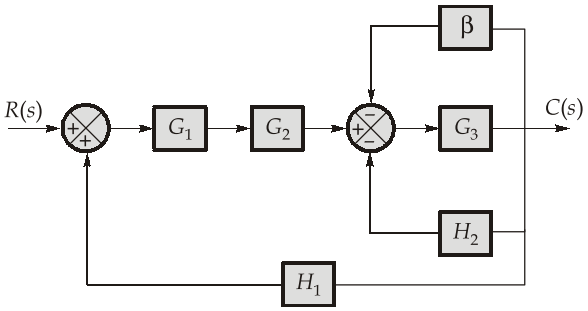
As the three blocks are connected in cascade the overall transfer function is given by the multiplication of individual blocks.

$$\therefore \quad x_1 \times x_2 \times x_3 = \frac{(s+1)}{s(s+2)(s+3)}$$

$$\frac{1}{s(s+2)} \times \frac{(s+2)}{(s+3)} \times x_3 = \frac{(s+1)}{s(s+2)(s+3)}$$

$$x_3 = \frac{(s+1)}{(s+2)}$$

Q.92 Consider the block diagram shown below:



If the transfer function of this system is

$$T(s) = \frac{G_1G_2G_3}{1+G_3H_2+G_2G_3(H_3-G_1H_1)}$$

then, the value of β is

(a) H_3 (b) G_2H_3

(c) $G_3G_2H_3$ (d) G_1H_3

92. **(b)**

The closed loop transfer function of the given system is,

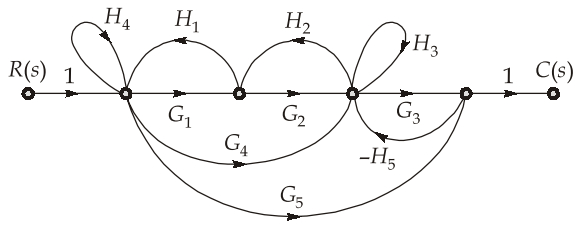
$$T(s) = \frac{G_1G_2G_3}{1 - G_1G_2G_3H_1 + G_3H_2 + G_3\beta}$$

On comparing the above equation with the given transfer function, we get,

$$G_3\beta = G_2G_3H_3$$

$$\therefore \quad \beta = G_2H_3$$

Q.93 Consider the signal flow graph shown below:



Which one of the following is not a forward path gain of the given signal flow graph?

(a) $G_1G_2G_3$ (b) G_4G_3

(c) G_5 (d) $G_1G_2H_3G_3$

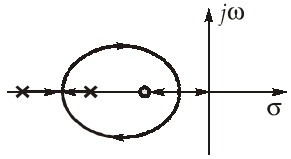
93. **(d)**

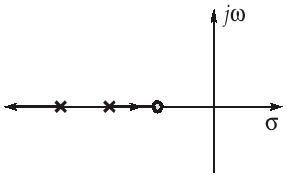
A self-loop does not contribute to the forward path gain.

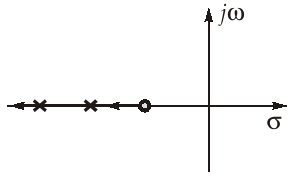
Q.94 The forward path transfer function of a unity feedback system is given by,

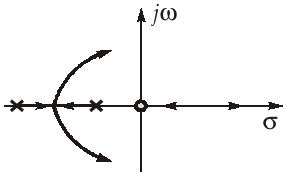
$$G(s) = \frac{K(s+1)}{(s+2)(s+3)}$$

The general form of root locus plot of above system is

(a)


(b)


(c)


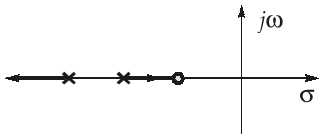
(d)


94. **(b)**

$$\text{Centroid} = \frac{\sum P - \sum Z}{P - Z} = \frac{-(2+3)+1}{1} = -4$$

$$\text{Angle of asymptotes} = \frac{(2q+1)180^\circ}{P-Z} = 180^\circ, 540^\circ \text{ and } 900^\circ$$

$\therefore$ Approximated plot is,



Q.95 The polar plot touches the negative real axis only at the origin. The gain margin is

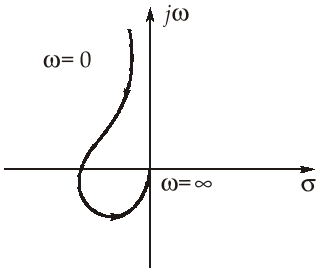
(a) 0 (b) Negative

(c) Finite positive value (d) Infinite

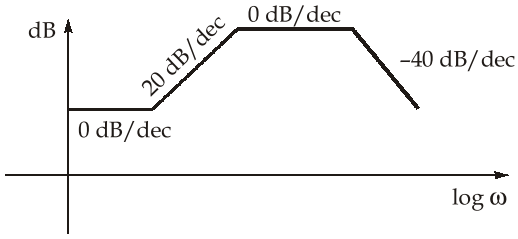
95. (d)

When the polar plot does not intersect negative real axis, the phase cross over frequency cannot be determined and thus, the gain margin is assumed to be ∞.

Q.96 The polar plot and Bode magnitude plot of two systems are given in the figure below,



System I



System II

(a) Both the systems are type 1 system.

(b) System I is type -3 and system II is type 1 system.

(c) System I is type 1 and system II is type 0 system.

(d) System I is type 3 and system II is type 0 system.

96. (d)

At ω = 0, the plot for system I, started from –270° hence it represents a type 3 system.

At ω = 0, the plot for system II has slope of 0 dB/dec and therefore it is a type 0 system.

Q.97 A second order system with closed loop transfer function $T(s) = \dfrac{25}{s^2 + \beta s + 25}$ was initially at rest. When it is subjected to a unit step input at $t = 0$, the second overshoot in the response occurred at $\dfrac{3\pi}{4}$ sec. Then the value of parameter β is

(a) 2 (b) 5

(c) 6 (d) 8

97. (c)

For peak overshoot, the peak time $\tau_p = \dfrac{n\pi}{\omega_d}$ Here $n = 3$ (for second overshoot)

$$\therefore \quad \frac{3\pi}{4} = \frac{3\pi}{\omega_d}$$

or $$\omega_d = 4 \text{ rad/sec} = \omega_n\sqrt{1-\xi^2}$$

$$\therefore \quad 4 = 5\sqrt{1-\xi^2} \quad (\because \omega_n^2 = 25 \text{ for given transfer function})$$

$$-\xi^2 = \left(\frac{4}{5}\right)^2 - 1$$

$$\xi^2 = \frac{25-16}{25} = \frac{9}{25}$$

or $$\xi = \frac{3}{5}$$

$$\therefore \quad \beta = 2\xi\omega_n = 2\times\frac{3}{5}\times 5 = 6$$

Q.98 The open loop transfer function of a unity negative feedback control system is, $G(s) = \frac{(s+4A)}{s(s+4)(s+8)}$. For which one of the following values of 'A', the system is stable?

(a) 75 (b) 100
(c) 125 (d) 150

98. (a)

The characteristic equation of the given system is,

$s(s+4)(s+8) + (s+4A) = 0$

$s^3 + (4+8)s^2 + 32s + s + 4A = 0$

$s^3 + (12)s^2 + (33)s + 4A = 0$

For Stability, $(12 \times 33) > 4A$

$396 > 4A$

or $A < 99$ for stability.

Q.99 The first two row of Routh's array of a third order system are given as

s^3	4	4
s^2	3	3

Which of the following option is correct for the given system?

(a) The characteristic equation has one root in the RHS of s-plane.
(b) The characteristic equation has two roots on the $j\omega$ axis.
(c) The characteristic equation has two roots in LHS of s-plane.
(d) The characteristic equation has one root at RHS of s-plane and two roots in $j\omega$ axis.

99. (b)

The Routh's table can be formed as

s^3	4	4
s^2	$3(s^2)$	$3(0)$
s^1	$(0)6$	(0)
s^0	$\frac{18-0}{6} = 3$	

as there is no sign change in the first column of Routh array thus, there will be no pole lie on the RHS of s-plane. Also the row of zero occurs that indicates the complex conjugate poles exists on $j\omega$ axis.

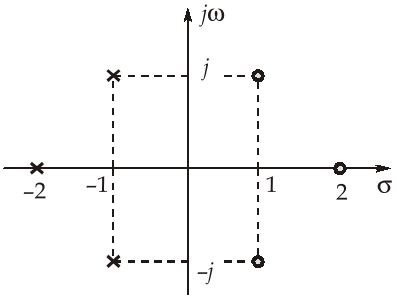
Q.100 The open loop transfer function of a system is given by

$$G(s)H(s) = \frac{(s-2)(s^2-2s+2)}{(s+2)(s^2+2s+2)}$$

The above system is a

(a) Stable system
(b) Minimum phase system
(c) Non-minimum phase system
(d) All pass system

100. (d)



Q.101 Which one of the following statements is correct?
A plant is controlled by a proportional controller. If a time delay element is introduced in the loop, its

(a) phase margin remains the same but gain margin decreases.
(b) phase margin increases but gain margin decreases.
(c) both phase margin and gain margin decrease.
(d) both phase margin and gain margin increase.

101. (c)
The introduction of a time delay element decreases both phase margin and gain margin.

Q.102 Consider the following statements regarding Routh's array:

1. The situation of a row of zeros indicates the presence of symmetrically located roots.
2. The order of the auxiliary equation obtained from the elements of the Routh's table is always odd.
3. If the first element of any row is zero with other non-zero elements the system is unstable.

Which of the above statements is/are correct?

(a) 1 only
(b) 1 and 2 only
(c) 2 and 3 only
(d) 1 and 3 only

102. (d)

Q.103 The characteristic equation of a system given by

$$s^3 + 5s^2 + 8s + 6 = 0$$

The largest time constant of this system is

(a) 0.33 sec
(b) 1 sec
(c) 1.33 sec
(d) 2 sec

103. (b)

The roots of the characteristic equation is given by $(s + 3)(s^2 + 2s + 2) = 0$

$\therefore \quad s = -3, -1 \pm j$

for $\quad s = -3$

$$T = \frac{1}{3} = 0.33 \text{ sec}$$

For, $\quad s = -1 \pm j$

$\xi\omega_n = 1$ (by comparing it with standard second order system)

$\therefore \quad T = \dfrac{1}{\xi\omega_n} = 1 \text{ sec}$

Q.104 The state space description of a system given by

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}-2 & 4\\ 0 & -1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ 1\end{bmatrix}u$$

$$y = \begin{bmatrix}1 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}$$

The state transition matrix of this system is

(a) $\begin{bmatrix}e^{-2t} & 4e^{-t} - 4e^{-2t}\\ 0 & e^{-t}\end{bmatrix}$ (b) $\begin{bmatrix}e^{-t} & -2e^{t} + 2e^{-2t}\\ 0 & e^{-2t}\end{bmatrix}$

(c) $\begin{bmatrix}e^{-2t} & 4e^{-2t} - 4e^{-t}\\ 0 & e^{-t}\end{bmatrix}$ (d) $\begin{bmatrix}e^{-t} & -2e^{-2t} + 2e^{-t}\\ 0 & e^{-2t}\end{bmatrix}$

104. (a)

The state transition matrix is given by

$$e^{A(t)} = L^{-1}[sI - A]^{-1}$$

Here $$(sI - A) = \begin{bmatrix}s & 0\\ 0 & s\end{bmatrix} - \begin{bmatrix}-2 & 4\\ 0 & -1\end{bmatrix} = \begin{bmatrix}s+2 & -4\\ 0 & s+1\end{bmatrix}$$

$$(sI - A)^{-1} = \frac{1}{(s+1)(s+2)}\begin{bmatrix}s+1 & 4\\ 0 & s+2\end{bmatrix} = \begin{bmatrix}\dfrac{1}{s+2} & \dfrac{4}{(s+1)(s+2)}\\ 0 & \dfrac{1}{(s+1)}\end{bmatrix}$$

$$L^{-1}(sI - A)^{-1} = \begin{bmatrix}e^{-2t} & 4e^{-t} - 4e^{-2t}\\ 0 & e^{-t}\end{bmatrix}$$

Q.105 A unity feedback control system is characterized by the open loop transfer function

$$G(s) = \frac{4}{s(0.4s + 1)(0.15s + 1)}$$

The steady state error for ramp input of $3tu(t)$ will be

(a) 0.25 (b) 0.75

(c) 1.33 (d) 4

105. **(b)**

For ramp input, $K_v = \lim_{s\to 0} sG(s)H(s)$

$$= \frac{4}{(1)\times(1)}$$

$$K_v = 4$$

$$\therefore \quad e_{ss} = \frac{A}{K_v} = \frac{3}{4} = 0.75$$

Q.106 Consider the following statements:

S_1: The addition of open loop zeros in the system pulls the root locus towards left from the $j\omega$-axis and system becomes more stable.

S_2: The addition of open loop poles in the system pulls the root locus towards $j\omega$-axis and system response becomes faster.

Which of the above statements is/are correct?

(a) S_1 only (b) S_2 only

(c) Both S_1 and S_2 (d) Neither S_1 nor S_2

106. **(a)**

The addition of open loop poles in the system pulls the root locus towards right and the system response become slow.

Q.107 Consider the following loop transfer function:

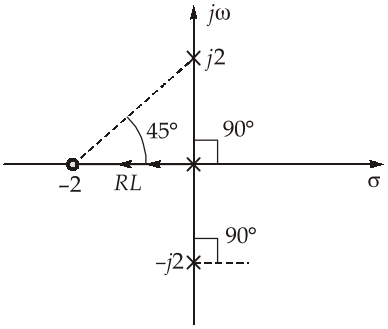
$$G(s)H(s) = \frac{K(s+2)}{s(s^2+4)}$$

The angle of departure at $s = j2$ for $K > 0$ is

(a) 90° (b) 75°

(c) 45° (d) 135°

107. **(c)**



Given, $G(s)H(s) = \frac{K(s+2)}{s(s^2+4)}$

Here, $P = 3$, $Z = 1$, $P - Z = 2$

No. of branches of RL terminating at zero = 1.

No. of branches of RL terminating at infinity = 2.

Here, two branches of RL has to terminate at infinity.

Thus, the two imaginary poles will terminate at infinity.

Hence, we need to find angle of departure for which we join all poles and zeros with the imaginary pole at $s = j2$.

Now, $\phi = \Sigma(\phi_z - \phi_P)$

Here, $\Sigma\phi_z = 45°$

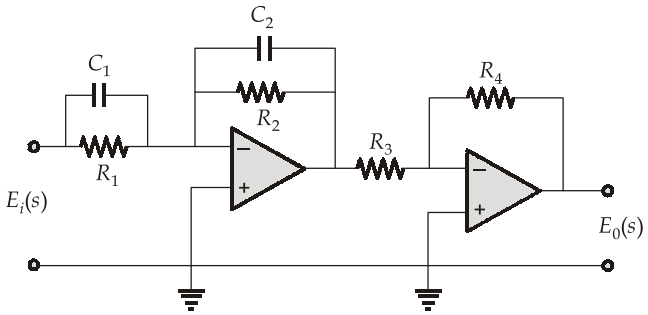
and $\Sigma\phi_P = 90° + 90° = 180°$

Thus, $\phi = 45° - 180° = -135°$

$\therefore$ Angle of departure is,

$$\phi_D = 180° + \phi = 180° - 135° = 45°$$

Q.108 The following circuit represents a



(assume $T_1 > T_2$)

(a) lead network
(b) lag network
(c) lag lead network
(d) lead lag network

108. (a)

The transfer function of the above circuit is,

$$\frac{E_0(s)}{E_i(s)} = \frac{R_2R_4(R_1C_1s+1)}{R_1R_3(R_2C_2s+1)} = \frac{R_4C_1}{R_3C_2}\left(\frac{s+\frac{1}{R_1C_1}}{s+\frac{1}{R_2C_2}}\right)$$

$$= K\alpha\left(\frac{1+sT}{1+\alpha sT}\right) = K_c\left(\frac{s+\frac{1}{T}}{s+\frac{1}{\alpha T}}\right)$$

Here, $T = R_1C_1$ and $\alpha T = R_2C_2$

If $R_1C_1 > R_2C_2$ then $\alpha < 1$.

Thus, it represents a phase lead network.

Q.109 The open loop transfer function of a unity negative feedback control system is given by

$$G(s) = \frac{2s^2 + as + 50}{(s+1)^2(s+2)}$$

The possible value of 'a' to make the given system stable is

(a) 1
(b) 2
(c) 3
(d) 4

109. (d)

The CE of the given system is,

$$1 + G(s) = 0$$

$$1 + \frac{2s^2 + as + 50}{(s+1)^2(s+2)} = 0$$

$(s^2 + 2s + 1)(s + 2) + 2s^2 + as + 50 = 0$

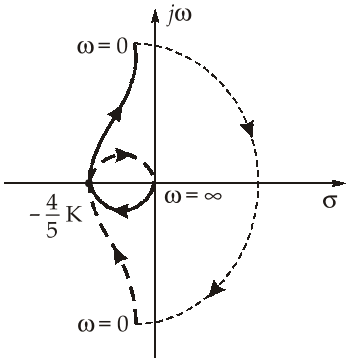
$s^3 + 2s^2 + s + 2s^2 + 4s + 2 + 2s^2 + as + 50 = 0$

$s^3 + 6s^2 + (5 + a)s + 52 = 0$

For system to be stable

$$(5 + a)6 > 52$$
$$30 + 6a > 52$$
$$6a > (52 - 30)$$
$$a > \frac{22}{6}$$
$$a > 3.667$$

Q.110 The Nyquist plot of a stable system is given by



For $K > \frac{5}{4}$, the total number of RHS poles of characteristic equation will be

(a) 0 (b) 1
(c) 2 (d) 3

110. (c)

As the system is said to be stable,
Therefore, no open loop pole in the RHS.

$$\therefore \quad P = 0$$

The intersection point $\left(-\frac{4}{5}K, 0\right)$ and $K > \frac{5}{4}$.

$$\therefore \quad \frac{4}{5}K > 1$$

or $$-\frac{4}{5}K < -1$$

That means the Nyquist plot encircles the critical point two times in the clockwise direction

Hence, $N = -2$
$\Rightarrow$ $N = P - Z$
$\Rightarrow$ $-2 = -Z$ or $Z = 2$

Q.111 A unity feedback closed loop control system has

$$G(s)H(s) = \frac{4}{(s+2)^2}$$

Its root locus technique will give

1. Stable system for $K > -4$
2. GM = 1
3. PM = 180°

The correct statements are

(a) 2 and 3 (b) 1 and 3

(c) 1 and 2 (d) All

111. (b)

Let $K = 4$ then,

$$G(s)H(s) = \frac{K}{(s+2)^2}$$

Characteristic equation = $1 + G(s)H(s) = s^2 + 4s + (4 + K) = 0$

Routh array

s^2	1	$(4+K)$
s^1	4	0
s^0	$4+K$	

For stability $K > -4$

now, calculating ω_{pc}

$$-180° = 2\tan^{-1}\omega_{pc}$$

or $$\omega_{pc} = \infty$$

Hence $$GM = 0 \text{ dB} = \infty$$

and $$|G(\omega)H(\omega)| = \frac{4}{\left(\sqrt{(\omega_{gc})^2 + 2^2}\right)^2} = 1$$

$$\frac{4}{\left(\omega_{gc}^2 + 4\right)} = 1$$

or $$\omega_{gc}^2 = 0$$

$$\omega_{gc} = 0$$

$$PM = 180° - \tan^{-1}\frac{\omega_{gc}}{2} - \tan^{-1}\frac{\omega_{gc}}{2}$$

$$= 180°$$

Q.112 A compensating network has its open loop transfer function $G(s) = \frac{5(1+0.25s)}{1+0.01s}$. The maximum phase compensation occurs at a frequency of

(a) 200 rad/sec (b) 100 rad/sec

(c) 20 rad/sec (d) 5 rad/sec

112. **(c)**

On comparing the given transfer function with standard equation is $\frac{\alpha(1+Ts)}{(1+\alpha Ts)}$.

We have, $T = 0.25$ and $\alpha T = 0.01$

$$\therefore \quad \omega_m = \frac{1}{T}\sqrt{\frac{1}{\alpha}} = \sqrt{\frac{1}{T}\times\frac{1}{\alpha T}} = \sqrt{\frac{1}{0.25}\times\frac{1}{0.01}} = \sqrt{400}$$
$$= 20 \text{ rad/sec}$$

Q.113 The state space representation of a control system is given as,

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}-\frac{1}{\alpha} & 0\\ 0 & -\frac{1}{\beta}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}1/\alpha\\ 1/\beta\end{bmatrix}u$$

this system becomes uncontrollable, if

(a) $\alpha = \beta$ (b) $\alpha > \beta$

(c) $\alpha < \beta$ (d) None of these

113. **(a)**

For controllability,

$$Q_C = [B : AB]$$

$$Q_C = \begin{bmatrix}\frac{1}{\alpha} & -\frac{1}{\alpha^2}\\ \frac{1}{\beta} & -\frac{1}{\beta^2}\end{bmatrix}$$

$$\because \quad |Q_c| \neq 0$$

$$\therefore \quad \alpha \neq \beta$$

Thus, for $\alpha = \beta$, the system becomes uncontrollable.

Q.114 A microprocessor using a 3 MHz clock has three '*T*' states in each machine cycle. If an instruction cycle needs 4 machine cycles, how much time will be taken to complete the execution of this instruction?

(a) 333 ns (b) 1333 ns

(c) 1 μs (d) 4 μs

114. **(d)**

$t_i \rightarrow$ time for completion of an instruction cycle

$t_i = 4\ t_m$; $t_m \rightarrow$ time for machine cycle

$t_m = 3T$; $T \rightarrow$ time for each T-state

$$f = 3 \text{ MHz}$$

$$T = \frac{1}{f} = \frac{1}{3\times10^6}$$

$$t_i = 12T = \frac{12}{3\times10^6} = 4\times10^{-6} = 4\,\mu\text{sec}$$

Q.115 Which one of the following statements is correct?
In 8085 μP, the READY signal is useful when the CPU communicates with
(a) a PPI chip
(b) a DMA controller chip
(c) a slow peripheral chip
(d) a fast peripheral chip

115. (c)
READY – Active high signal, input to 8085 as an external request from slow peripheral to indicate that peripheral is not yet ready for data transfer between processor and peripheral device.

Q.116 Which of the following is not a vectored interrupt?
(a) TRAP
(b) INTR
(c) RST 7.5
(d) RST 3

116. (b)

Q.117 When a program is being executed in an 8085 microprocessor, its Program Counter contains
(a) the number of instructions in the current program that have already been executed.
(b) the total number of instructions in the program being executed.
(c) the memory address of the instruction that is being currently executed.
(d) the memory address of the instruction that is to be executed next.

117. (d)
Program counter contains the memory address of the instruction that is to be executed next.

Q.118 The 8085 assembly language instruction that stores the content of *H* and *L* registers into the memory locations 2050_H and 2051_H, respectively is
(a) SPHL 2050_H
(b) LHLD 2051_H
(c) SHLD 2050_H
(d) STAX 2050_H

118. (c)
Instruction SHLD 2050_H stores the content of L to memory location 2050_H and content of register H to next memory location 2051_H.

Q.119 What is the addressing mode of JMP instruction?
(a) Register addressing mode
(b) Register indirect addressing mode
(c) Immediate addressing mode
(d) Implied addressing mode

119. (c)

Q.120 An Intel 8085 processor is executing the program given below.

```
        MVI A, 10 H
        MVI B, 10 H
Back:   NOP
        ADD B
        RLC
        JNC BACK
        HLT
```

The number of times that the operation *NOP* will be executed is equal to
(a) 1
(b) 2
(c) 3
(d) 4

120. **(c)**

First loop,

ADD *B*

Accumulator-20H | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

RLC | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Second loop:

A	0	1	0	0	0	0	0	0
	0	0	0	1	0	0	0	0
	0	1	0	1	0	0	0	0
RLC	1	0	1	0	0	0	0	0

Third loop:

A	1	0	1	0	0	0	0	0	CY 0
	0	0	0	1	0	0	0	0	
	1	0	1	1	0	0	0	0	
RLC	0	1	1	0	0	0	0	0	CY 1

Carry is generated. Now program will halt. So NOP instruction is executed 3 times.

Q.121 Consider the following instructions executed in 8085 microprocessor

XRA A
MVI B, 10 H
ADI, 01 H
ORA B
HLT

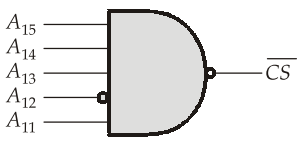
After execution, contents of the Register A and B are respectively

(a) 01 H and 10 H
(b) 10 H and 01 H
(c) 11 H and 10 H
(d) 11 H and 01 H

121. **(c)**

XRA A $\Rightarrow$ A = 00 H
MVI B, 10 H $\Rightarrow$ B = 10 H
ADI 01 H $\Rightarrow$ A = 01 H (Add the data '01 H' with accumulator)
ORA B $\Rightarrow$ A = 11 H

Q.122 The logic circuit used to generate the active low chip select (CS) by an 8085 microprocessor to address a peripheral is shown in figure. The peripheral will respond to addresses in the figure.



(a) E800-EFFF
(b) 000E-FFFE
(c) 1000-FFFF
(d) 0001-FFF1

122. **(a)**

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	.....	A_0
1	1	1	0	1	0	.....	0
1	1	1	0	1	1	.....	1

$\Rightarrow$ E800 – EFFF

Q.123 Consider the following modes of data transfer:
1. Memory to register
2. Register to memory
3. Memory to memory
4. Register to register

Which of the above modes are allowed by the data transfer group of instructions of an 8085 microprocessor?
(a) 1 and 2 only
(b) 3 and 4 only
(c) 1, 2 and 4 only
(d) 1, 2, 3 and 4

123. **(c)**
Memory to memory transfer is not allowed by the data transfer group of instructions of an 8085 microprocessor.

Q.124 The circuit that allows the processor to move to any location in memory upon reset is called as
(a) Call-on-reset circuit
(b) Locate-on-reset circuit
(c) Jump-on-reset circuit
(d) No such circuit exists

124. **(c)**
Jump-on-reset circuit allows the processor to move to any location in memory upon reset.

Q.125 In a particular operation of 8086 microprocessor, the segment address is 2000H and the offset address is 5000H. The effective or physical address corresponding to the operation will be
(a) 20000H (b) 52000H
(c) 25000H (d) 50000H

125. **(c)**
Effective address = 20000H + 5000H = 25000H

Q.126 Which of the following flags is not used in 8051 microcontroller?
(a) Carry flag (b) Parity flag
(c) Trap flag (d) Overflow flag

126. (c)

Q.127 Which one of the following is not true about RS232 standard?
(a) It establishes the way data is coded (b) It defines signal voltage levels
(c) It does not decide data transmission rate (d) It defines standard connector configurations

127. (c)

Q.128 The register banks in 8051 microcontroller can be switched
(a) by programming the program counter
(b) by programming the stack pointer
(c) by programming the SCON register
(d) by programming the program status word

128. (d)

Q.129 Consider the following features of mode-0 (Basic I/O mode) of a programmable I/O port (8255):
1. Two 8-bit ports and two 4-bit ports are available.
2. Any port can be used as an input or output port.
3. Output ports are latched.
4. Input ports are not latched.

Select the correct features of mode-0.
(a) 1 and 3 only
(b) 1, 2 and 3 only
(c) 2 and 4 only
(d) 1, 2, 3 and 4

129. **(d)**
All the given features are related with Mode-0 of 8255.

Q.130 A microcontroller is to be programmed to generate square waveforms with minimum and maximum time periods of 100 ns and 10 ms. The minimum clock frequency required by the microcontroller is
(a) 100 Hz
(b) 1 kHz
(c) 1 MHz
(d) 10 MHz

130. **(d)**
To generate a square wave, the required condition is,

$$T_{clock} \leq T_{square\ wave}$$

To generate a square wave with a time period of 100 ns,

$$T_{clock} \leq 100\ ns$$

$$f_{clock} \geq \frac{10^9}{100} Hz = 10\ MHz$$

$$f_{clock} \geq 10\ MHz \quad ...(i)$$

To generate a square wave with a period of 10 ms,

$$T_{clock} \leq 10\ ms$$

$$f_{clock} \geq \frac{1000}{10} = 100\ Hz$$

$$f_{clock} \geq 100\ Hz \quad ...(ii)$$

From equations (i) and (ii),

$$f_{clock} \geq 10\ MHz$$

$$f_{clock(min)} = 10\ MHz$$

Q.131 Consider the following steps involved in the ADC interfacing:

S_1: Ensure the stability of analog input applied to the ADC.
S_2: Issue start of conversion (SOC) pulse to ADC.
S_3: Read end of conversion (EOC) signal from ADC.
S_4: Read digital data from ADC after conversion.

Which of the above steps are necessary to follow while interfacing Analog-to-Digital converters to microprocessors?

(a) S_1 and S_3 only
(b) S_2, S_3 and S_4 only
(c) S_2 and S_3 only
(d) S_1, S_2, S_3 and S_4

131. (d)

All the given steps are necessary.

Q.132 Microcontrollers support "embedded" applications because

1. the control software is so small that, it can be embedded within the microcontrollers' ROM.
2. since minimum external circuitry is required, the microcontroller can be embedded within a product.
3. a hard disc can be embedded within the computer system supporting the application.

Which of the above statements are correct?

(a) 1 and 2 only
(b) 2 and 3 only
(c) 1 and 3 only
(d) 1, 2 and 3

132. (a)

Q.133 Which of the following devices are available on-chip of a microcontroller?

1. RAM
2. EPROM
3. PORTS

Select the correct answer using the codes given below:

(a) 1 and 2 only
(b) 2 and 3 only
(c) 1 and 3 only
(d) 1, 2 and 3

133. (d)

Q.134 The DMA transfer technique where one word data is transferred at a time is called

(a) Memory-stealing
(b) Cycle-stealing
(c) Hand-shaking
(d) Byte-transfer

134. (b)

Q.135 In an 8085 microprocessor, if the status lines $IO/\overline{M}$, S_1 and S_0 are 0, 1 and 0 respectively, then the operation going on in the microprocessor system will be

(a) Read I/O port
(b) Read memory
(c) Write I/O port
(d) Write memory

135. (b)

$IO/\overline{M} = 0 \Rightarrow$ accessing memory

S_1	S_0	Operation
0	0	Halt
0	1	Write
1	0	Read
1	1	Opcode fetch

So, the operation going on in the processor system is memory read.

Q.136 Which one of the following is not a valid instruction of the 8085 microprocessor?

(a) STC (b) CMA

(c) CLC (d) CMC

136. (c)

STC ⇒ Set carry

CMA ⇒ Complement the accumulator

CMC ⇒ Complement carry

"CLC" is not a valid instruction of the 8085 microprocessor.

Direction (Q.137 to Q.140): The following items consists of two statements, one labelled as **Statement (I)** and the other labelled as **Statement (II)**. You have to examine these two statements carefully and select your answers to these items using the codes given below:

Codes:

(a) Both Statement (I) and Statement (II) are true and Statement (II) is the correct explanation of Statement (I).

(b) Both Statement (I) and Statement (II) are true but Statement (II) is not a correct explanation of Statement (I).

(c) Statement (I) is true but Statement (II) is false.

(d) Statement (I) is false but Statement (II) is true.

Q.137 Statement (I): If the system is stable, we can determine the relative stability of the system by its settling time.

Statement (II): If the settling time is less than that of the other system, then the system is said to be relatively more stable.

137. (a)

The settling time is inversely proportional to the real part of the dominant roots. If the settling time is less compared to other system, then the system has poles more left from the $j\omega$-axis and it will be relatively more stable.

Q.138 Statement (I): Location of poles of a transfer function in the s-plane affects greatly the transient response of the system and hence its stability.

Statement (II): The poles that are close to the imaginary axis in the left half of s-plane give rise to transient responses that will decay relatively slowly, whereas the poles that are far away from the imaginary axis corresponds to the fast decaying time responses.

138. (a)

Q.139 **Statement (I):** In an 8085 microprocessor, an input port and an output port can have same port address.

Statement (II): $\overline{RD}$ is used to enable the input port and $\overline{WR}$ is used to enable the output port.

139. (a)

Q.140 **Statement (I):** The data transfer using direct memory access is an example of peripheral-controlled data transfer.

Statement (II): In direct memory access, the DMA controller sends a HOLD signal to the microprocessor, then the microprocessor releases its data bus and the address bus to the DMA controller.

140. (a)

■■■■