GATE PSUs
State Engg. Exams

MADE EASY Workbook 2024

Detailed Explanations of Try Yourself *Questions*

Computer Science & IT

Digital Logic

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1 Number Systems and Binary Codes

Detailed Explanation of Try Yourself Questions

T3 : Solution

Converting into decimal number system

$$x^2 + 3x + 5 + 8^2 + 4 \times 8 + 4 = 2(x+2)^2 + x + 2 + 4$$
$$x^2 + 3x + 105 = 2x^2 + 8 + 8x + x + 6$$
$$x^2 + 5x - 91 = 0$$
$$(x + 13)(x - 7) = 0$$
$$x = -13, 7$$

base can't be negative

$$\Rightarrow \quad x = 7$$

T4 : Solution

$$(36)_7 = (27)_{10}$$
$$(67)_8 = (55)_{10}$$
$$(98)_{10} = (98)_{10}$$
$$(Z)_5 = (Z)_5$$
$$(241)_9 = (199)_{10}$$
$$\therefore \quad (Z)_5 = (199)_{10} - (27)_{10} - (55)_{10} - (98)_{10}$$
$$(Z)_5 = (19)_{10}$$
$$\therefore \quad Z = 34$$

T5 : Solution

Given that,

$$(110)_r = 4r$$

so, $r^2 + r = 4r$

$$\Rightarrow \quad r^2 = 3r$$
$$\Rightarrow \quad r = 3$$

so, $(010)_3 = 3$

So, the answer is 3 and 3.

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T6 : Solution

(d)

Given that,

$$(10)_x \times (10)_x = (100)_x$$
$$x \times x = x^2$$

and
$$(100)_x \times (100)_x = (10000)_x$$
$$x^2 \times x^2 = x^4$$

So, above conditions are valid for all values of x.

T7 : Solution

Since, $(123)_5 = (x8)_y$

$\Rightarrow$ $38 = xy + 8y$

So, the equation has 3 solution.

T8 : Solution

(d)

Given that,

$$73_x = 54_y$$

$\Rightarrow$ $7x + 3 = 5y + 4$

from the above equation we can see that option (d) is correct.

T9 : Solution

The 1's complement representation of –127 is 10000000 and 2's complement representation of –127 is 10000001 so the answer is $\frac{2}{1}$.

T12 : Solution

(d)

For example:

Let, $\left.\begin{matrix} X = +6, & n = 4 \\ Y = -5, & n = 4 \end{matrix}\right\} \Rightarrow (X - Y) = +11$

So Z = 11 which required 5 bits which is $(n + 1)$ bits.

T13 : Solution

Let number N is given to the system.

Output after 1's complement = $15 - N$

Output after 2's complement = $16 - 15 + N = N + 1$

3 such systems are connected in cascade.

So, Final output = Input + $(3)_{10}$ = 1010 + 0011 = 1101

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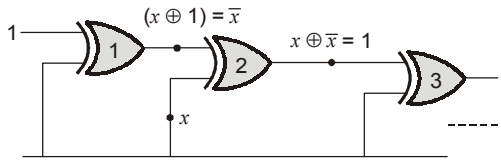
2 Boolean Algebra, Logic Gates and K-Maps

Detailed Explanation of Try Yourself Questions

T1 : Solution

(b)



Output of odd XOR is $\overline{x}$.
Output of even XOR is 1.

T2 : Solution

(d)

$$X * Y = XY + X'Y'$$
$$\& \quad Z = X * Y = XY + X'Y'$$
$$\overline{Z} = X'Y + XY'$$
$$P : Y * Z = YZ + Y'Z'$$
$$= Y[XY + X'Y'] + Y'[X'Y + XY']$$
$$= XY + XY'$$
$$= X \quad \text{True}$$
$$Q : X * Z = XZ + X'Z'$$
$$= X[XY + X'Y'] + X'[X'Y + XY']$$
$$= XY + X'Y$$
$$= Y \text{ True}$$
$$R : \underline{X * Y} * Z = Z * Z$$
$$= 1 \quad \text{True}$$

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T3 : Solution

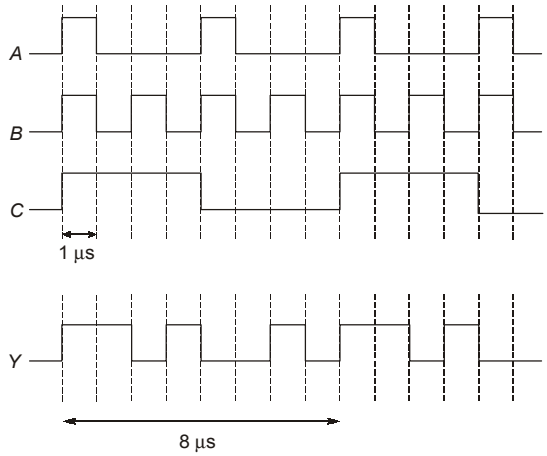
(a)

EXNOR gate on logic in called coincidence logic.

So, $f = AB + A'B'$

So option (a) is correct.

T4 : Solution



Frequency of output $= \dfrac{1}{8\,\mu s} = 125\,kHz$

T5 : Solution

(c)

$$f_1 = \Sigma m(0, 1, 3, 5)$$
$$f_2 = \Sigma m(4, 5)$$
$$f_3 = ?$$
$$f = \Sigma m(1, 4, 5)$$

and $f = ((f_1 + f_2)' + f_3')'$

$$f = (f_1 + f_2) \cdot f_3$$

So, $\Sigma m(1, 4, 5) = (\Sigma m(0, 1, 3, 5) + \Sigma m(4, 5)) \cdot f_3$

$\Rightarrow$ $\Sigma m(1, 4, 5) = (\Sigma m(0, 1, 3, 4, 5)) \cdot f_3$

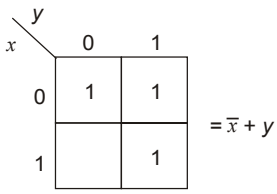
So, f_3 has to be zero for 0, 3 and should be 1 for 1, 4, 5 and dont care for 2, 6, 7.

So, answer is (c).

T8 : Solution

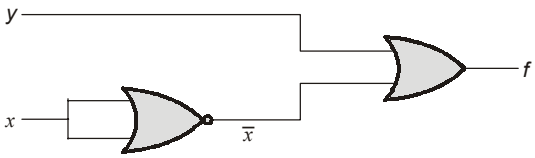
(d)

x	y	f
0	0	1
0	1	1
1	0	0
1	1	1



$= \bar{x} + y$

Since complements are not available.



$\therefore$ 2 units.

T10 : Solution

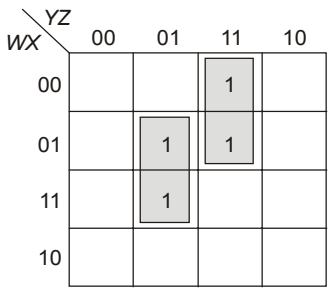
(d)

$$\begin{aligned} Y &= a + \bar{a}b + \bar{a}\bar{b}c + ... \\ &= a + \bar{a}(b + \bar{b}c) + ... \\ &= a + \bar{a}(b + \bar{b})(b + c) + ... \\ &= a + \bar{a}b + \bar{a}c + ... \\ &= (a + \bar{a})(a + b) + (a + \bar{a})(a + c).... \\ &= a + b + c... \end{aligned}$$

T11 : Solution

$$Y = \bar{x}yz + \bar{w}yz + \bar{w}xz$$

So,



$\Rightarrow$ $Y = w'yz + xy'z$

So, Gate (3) is redundant.

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T12 : Solution

(b)

D will be '1' majority of input is 1, so

$$D = ABC + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

T13 : Solution

(a)

$f =$

AB \ BC	00	01	11	10
00	0	0	1	0
01	0	0	0	1

so, $f = B(A + C)(A' + C')$

T14 : Solution

Let the 3 locks are A, B, C

0 - key not inserted

1 - key inserted

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	X

A \ BC	00	01	11	10
0			1	
1			1 (X)	1

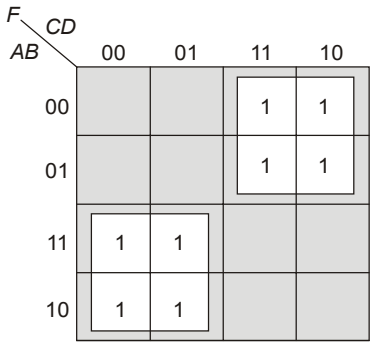
$Y = AB + BC + AC$

The expression for Y is similar to carry in full adder circuit.

So, Number of NAND Gates required are = 6.

T15 : Solution

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



$$F = \overline{A}C + A\overline{C} = A \oplus C$$

T16 : Solution

(b)

$$f = A + B'C$$

so,

$f =$

A \ BC	00	01	11	10
0		1		
1	1	1	1	1

so,

$$f = \Sigma m(1, 4, 5, 6, 7)$$

T17 : Solution

(a)

Function 'f' is 1 when x and y are different.

Clearly we can say that,

$$f = x \oplus y = xy' + x'y$$

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T18 : Solution

(c)

It is given $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$

	x_1	x_2	x_3	x_4	$x_1 \oplus x_2 \oplus x_3 \oplus x_4$
0	0	0	0	0	0 ←
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0 ←
4	0	1	0	0	1
5	0	1	0	1	0 ←
6	0	1	1	0	0 ←
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0 ←
10	1	0	1	0	0 ←
11	1	0	1	1	1
12	1	1	0	0	0 ←
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0 ←

For the minterms

m_0, m_3, m_5, m_6, m_9, m_{10}, m_{12} and m_{15}

$$x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$$

[i.e. whenever even number of variables are 1, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$]

Option (a) fails whenever

$$x_1 = x_2 = x_3 = x_4 = 1$$

Option (b) fails whenever

x_1, x_2, x_3 and x_4 are 0 1 0 0 [and for few more combinations]

Options (d) fails whenver

x_1, x_2, x_3 and x_4 are 0 0 1 1 [and for few more combinations]

Options (c) satisfies for every combination.

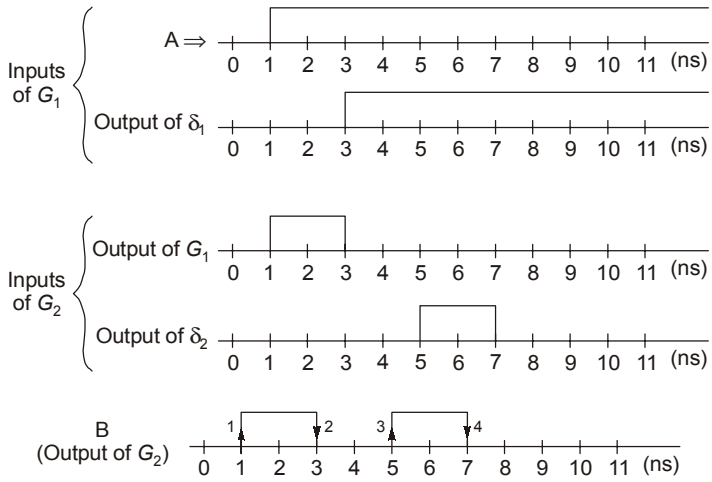
Hence option (c) is correct.

T19 : Solution

(d)

Consider left side EX-OR gate as G_1 and right side EX-OR gate as G_2.

1. To find number of transitions at B i.e. the output of gate G_2, it is required to identify the inputs of gate G_2.
2. To identify gate G_2 inputs it is required to find gate G_1 output waveform.
3. To find gate G_1 output waveform, it is required to identify δ_1 output waveform.



Total numbers of transitions at B during interval from 0 to 10 ns are '4'.
Hence option (d).

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3 Combinational Logic Circuits

Detailed Explanation of Try Yourself Questions

T1 : Solution

(d)

From the figure we can see that,

$$O_3 = I_3$$
$$O_2 = I_2 \oplus I_3$$
$$O_1 = (I_2 + I_3)(I_2 \oplus I_3) \oplus I_1$$
$$= I_2 \oplus I_3 \oplus I_1$$
$$O_0 = (I_1 + (O_2 (I_2 + I_3))) \times O_1 \oplus I_0$$
$$= I_0 \oplus I_1 \oplus I_2 \oplus I_3$$

From this we can see that, if input is gray code then output is its binary.

T4 : Solution

(a)

The look ahead block has delay of 2 logic gates but input ot the block is given through XOR gate and for sum we need one gate delay so answer is 4.

T5 : Solution

(–1)

A and B are 8 bit numbers in 2's complement form.

$A = +1 \Rightarrow 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1$

B = ? so that longest latency in the 8 bit ripple carry adder if $B = -1$ then there will be longest latency whenever $A = +1$.

Verification

$A = +1$	0 0000 001
$A = -1$	1 1111 111
Carry out →	(1) 0 0000 000

Carry is propagating from LSB to MSB. Hence it is longest latency.

T6 : Solution

(c)

$$S_1 = A \oplus B$$
$$C_1 = AB$$
$$S = (A \oplus B) \oplus AB = (A \oplus B) \cdot \overline{AB} + (\overline{A \oplus B}) \cdot AB$$
$$= (A\bar{B} + \bar{A}B)(\bar{A} + \bar{B}) + (AB + \bar{A}\bar{B})(A, B)$$
$$= A\bar{B} + \bar{A}B) + AB = A + B$$
$$C = (A \oplus B) \cdot AB$$
$$= (A\bar{B} + \bar{A}B) \cdot AB = 0$$

T9 : Solution

(a)

So, $$Y = \bar{A}\bar{B}\bar{C}I_0 + \bar{A}\bar{B}\bar{C}I_1 + \bar{A}B\bar{C}I_2 + \bar{A}BCI_3 + A\bar{B}\bar{C}I_4 + A\bar{B}CI_5 + \bar{A}B\bar{C}I_6 + ABCI_7$$

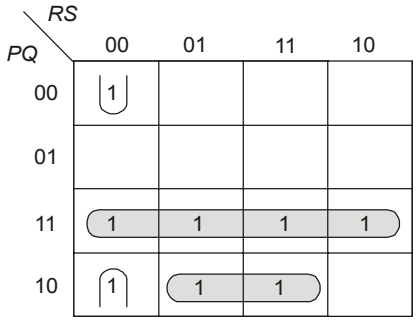
So, $$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BC + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$$
$$= \bar{A}\bar{B}\bar{D} + A\bar{C}\bar{D} + \bar{A}BC + \bar{A}B\bar{C}D + \bar{A}\bar{B}\bar{D} + A\bar{C}\bar{D} + \bar{A}B\bar{C} + \bar{A}BD$$
$$= \bar{A}D + A\bar{C}\bar{D} + \bar{A}BC$$

T11 : Solution

(a)

$$Z = PRS + PQR\bar{S} + P\bar{R}S + (P + \bar{Q})\,\bar{R}\bar{S}$$

Mapping above terms in Karnaugh map



$$Z = PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$$

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T13 : Solution

(b)

$a = 1$

$b = \bar{P}_2$ ...1 (NOT)

$c = \bar{P}_1$ ...1 (NOT)

$d = 1 = c + e$

$e = P_1 + \bar{P}_2$ ...1 (OR)

$f = \bar{P}_1 + P_2$ ...1 (OR)

$g = P_1 + P_2$ ... 1 (OR)

$\Rightarrow$ $g = P_1 + P_2$

$d = 1 = c + e$

P_1	P_2	a	b	c	d	e	f	g
0	0	1	1	1	1	1	1	0
0	1	1	0	1	1	0	1	1
1	0	1	1	0	1	1	0	1
1	1	1	0	0	1	1	1	1

T14 : Solution

(d)

2 – NOT gates

3 – OR gates

T15 : Solution

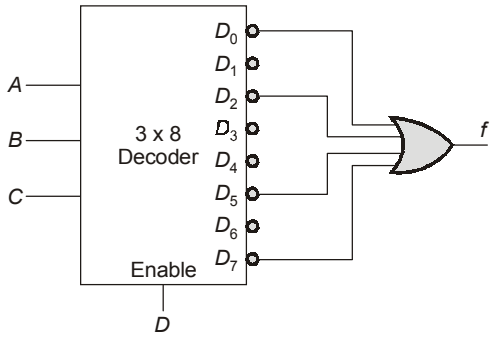
$$\frac{64}{8} + \frac{8}{8} = 8 + 1 = 9$$

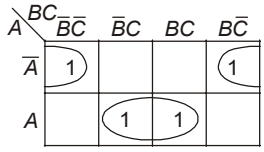
T16 : Solution

(b)

Redrawing the circuit

A	B	C	D	f
X	X	X	0	0
0	0	0	1	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

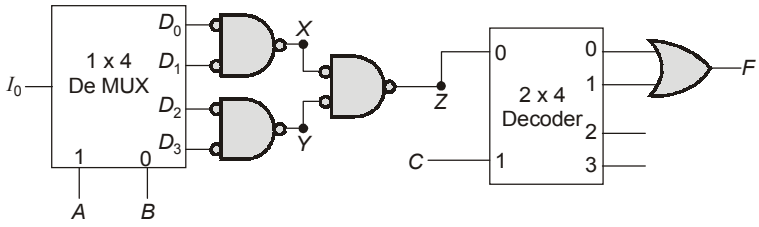




$$f = D(\bar{A}\bar{C} + AC)$$

T17 : Solution

(a)



$$X = \overline{\bar{D}_0\bar{D}_1}\, I_0 = (D_0 + D_1)I_0$$
$$= (\bar{A}\bar{B} + \bar{A}B)I_0 = \bar{A}I_0$$
$$Y = \overline{\bar{D}_2\,\bar{D}_3}\, I_0 = (D_2 + D_3)I_0$$
$$= (A\bar{B} + AB)I_0 = AI_0$$
$$Z = (\overline{\bar{X}\cdot\bar{Y}}) = X + Y$$
$$= \bar{A}\cdot I_0 + AI_0 = I_0$$
$$F = (\bar{Z}\bar{C} + Z\bar{C}) = \bar{C}(\bar{I}_0 + I_0)$$
$$= \bar{C}$$

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4 Sequential Circuits

Detailed Explanation of Try Yourself Questions

T1 : Solution

(a)

When $A = 1$ and $B = 1$

$X = \overline{Y}$

$Y = \overline{X}$

Now $A = 1$ and $B = 0$

$Y = 1$

$X = 0$

Now $A = 1$ and $B = 1$

$X = \overline{Y} = 0$

$Y = \overline{X} = 1$

So, the outputs x and y will be fixed at 0 and 1 respectively.

T2 : Solution

(b)

For NAND gates: Inputs [(0,1); (1,1)]

$\Rightarrow$ Output [(1, 0) ; (1, 0)]

For NOR gates : Inputs [(0, 1); (1,1)]

$\Rightarrow$ Output [(1,0); (0,0)]

T3 : Solution

(a)

Given that,

if $X = Y = 1$ then $Q^+ = 1$

$X = Y = 0$ then $Q^+ = 0$

$X = Y' = 0$ then $Q^+ = Q'$

$X = Y'$ = then $Q^+ = Q$

so,

X	Y	Q	Q^+
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$Q^+ =$

X \ YQ	00	01	11	10
0	0	0	0	1
1	1	1	1	1

$\Rightarrow \quad Q^+ = XQ + YQ'$

T4 : Solution

(c)

	A	B	C_i	S	C_o
After 1st CP	1	1	0	0	1
After 2nd CP	1	1	1	1	1

T7 : Solution

$Q_2Q_1Q_0 = 011$

1st Clk $\rightarrow$ $Q_2Q_1Q_0 = 100$

$\bar{Q}_0 = 1$ (triggers T_1)

$\bar{Q}_1 = 1$(triggers T_2)

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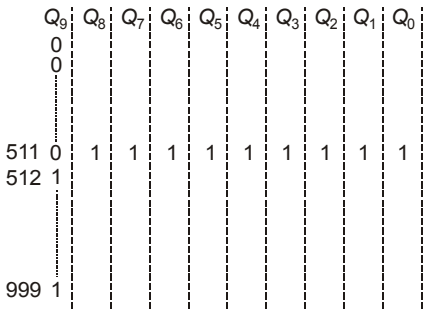
T9 : Solution



$$\text{Duty cycle of MSB} = \frac{999-511}{1000}\times 100 = 48.8\%$$

T11 : Solution

8-bit up counter has initial value

$$(10101100)_2 = (172)_{10}$$

and to reach $(00100111)_2 = (39)_{10}$

So it need 123 clocks.

T12 : Solution

(a)

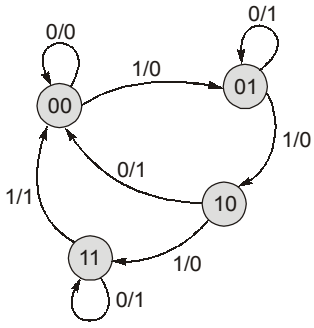
10 flip-flops initially at '0'.

After 2048 clocks all flip-flop will be '0' again so after 2060 clock count will be 12 i.e. 1100.

T14 : Solution

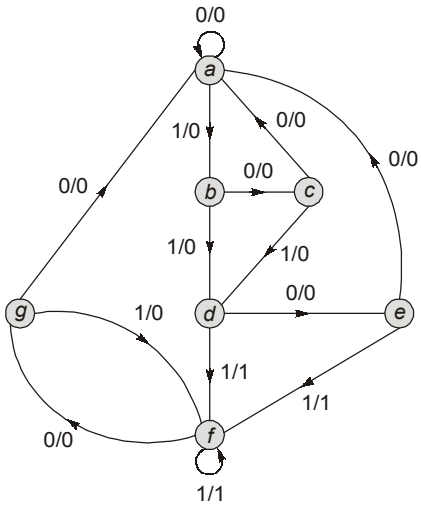
(b)

If we draw the state diagram of the system we get,



To reach 11 from 00 we need 1110 input sequence. So answer is (b).

T15 : Solution



Considering the input sequence 01010110100 starting from the initial state a. Each input of 0 or 1 produces an output of 0 or 1 and causes the circuit to go the next state. From the state diagram, we obtain the output and state sequence for the given input sequence as follows. With the circuit in initial state a, an input of 0 produces an output of 0 and circuit remains in state a. With present state at a and input of 1 and the output is 0 and the next state is b. With present state b and an input of 0, the output is 0 and the next state is c. Continuing this process, we find the complete sequence to be as follows:

State	*a*	*a*	*b*	*c*	*d*	*e*	*f*	*f*	*g*	*f*	*g*	*a*
Input	0	1	0	1	0	1	1	0	1	0	0	
Output	0	0	0	0	0	1	1	0	1	0	0	

In each column, we have the present state, input value and output value. The next state is written on top of the next column.

- We now proceed to reduce the number of states. Two states are said to be equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state. **"When two states are equivalent one of them can be removed without altering the input-output relationship."**

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State Table:

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*a*	*b*	0	0
b	*c*	*d*	0	0
c	*a*	*d*	0	0
d	*e*	*f*	0	1
e	*a*	*f*	0	1
f	*g*	*f*	0	1
g	*a*	*f*	0	1

- Now apply the statement written above under inverted comma, we look for two present states that go to the same next state and have the same output for both input combinations. Such states are *g* and *e*. They both go to states a and *f* and have outputs of 0 and 1, for $x = 0$ and $x = 1$ respectively. Therefore states *g* and e are equivalent, and one of these states can be removed. The row with present state *g* is removed, and state *g* is replaced by state *e*.

Reducing State Table:

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*a*	*b*	0	0
b	*c*	*d*	0	0
c	*a*	*d*	0	0
d	*e*	*f*	0	1
e	*a*	*f*	0	1
f	*e*	*f*	0	1

- Present state *f* now has next states *e* and *f* and outputs 0 and 1 for $x = 0$ and $x = 1$, respectively. The same next states and outputs appear in the row with present state *d*. Therefore states *f* and *d* are equivalent, and state *f* can be removed and replaced by *d*. The final reduced table is shown below:

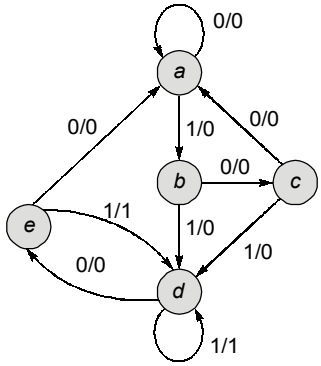
Reduced State Table:

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*a*	*b*	0	0
b	*c*	*d*	0	0
c	*a*	*d*	0	0
d	*e*	*d*	0	1
e	*a*	*d*	0	1

- The state diagram for the reduced table consists of only five states. This state diagram satisfies the original input-output specifications and will produce the required output sequence for any given input sequence.

State	*a*	*a*	*b*	*c*	*d*	*e*	*d*	*d*	*e*	*d*	*e*	*a*
Input	0	1	0	1	0	1	1	0	1	0	0	
Output	0	0	0	0	0	1	1	0	1	0	0	

Reduced state diagram:



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