

# ESE

## **MADE EASY** **WORKBOOK 2024**



**Detailed Explanations of  
Try Yourself Questions**

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**Electronics Engineering**  
**Computer Organization & Architecture**



**MADE EASY**  
Publications

# 1

## Data Representation



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

0	0 1 1 1 1 1 1 1	000 0000 0000 0000 0000 0000
1 bit	8 bit	23 bit

1. Sign = 0 (positive)

2. BE = 01111111

$$\begin{aligned} \text{Bias} &= +(2^{8-1} - 1) \\ &= +127 \end{aligned}$$

∴ Actual exponent = BE - bias

$$\begin{array}{r} \text{i.e.} \quad 01111111 \\ \quad 01111111 \\ \hline \quad 00000000 = 0 \end{array}$$

3. Mantissa = 0000....23 bits (0's)  
= 0

∴ Normalized mantissa = 1 M  
= 1.0

$$\begin{aligned} \text{Actual number} &= +1.0 * 2^0 \\ &= +1 \end{aligned}$$

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# 2

## Basic CPU Architecture



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

(d)

In the horizontal programming control signals are expressed in a decoded binary format. So all the (a), (b) and (c) options are correct.

#### T2 : Solution

(b)

Average instruction execution time =  $\Sigma(IC_i \times CPI_i)$  cycle time

$$\Rightarrow (0.3 \times 8) + (0.2 \times 4) + (0.3 \times 12) + (0.2 \times 12)$$

$$\Rightarrow (2.4 + 0.8 + 3.6 + 2.4)$$

$$\Rightarrow 9.2 \text{ cycles}$$

So, execution time =  $9.2 \times \frac{1}{2.3} \text{ ns} = 4 \text{ ns}$

1 Instruction  $\triangleleft$  4 ns

# Instruction  $\triangleleft$  1 ns

$$\Rightarrow 250 \text{ MIPS}$$

#### T3 : Solution

(b)

Maximum bits required =  $20 + 70 + 2 + 10 + 23$

When the groups are horizontal = 125

Minimum bits required =  $\log_2 20 + \log_2 70 + \log_2 2 + \log_2 10 + \log_2 23$

When the groups are vertical =  $5 + 7 + 1 + 4 + 5 = 22$

# bits save =  $(125 - 22) = 103$

#### T4 : Solution

(c)

In the instruction fetch process, CPU reads the instruction from the memory based on a program counter.



# 3

## Memory Organization



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

(a)

$$\begin{aligned}\text{\# chips required} &= \frac{\text{Needed}}{\text{given}} \\ &= \frac{256 \text{ kB}}{32 \text{ k} \times 1} \\ &= \frac{2^8 \times 2^{10} \times 2^3}{2^5 \times 2^{10} \times 2^0} = \frac{2^{21}}{2^{15}} = 2^6 = 64\end{aligned}$$

#### T2 : Solution

(c)

$$\begin{aligned}\text{\# chips required} &= \frac{2 \text{ M} \times 32}{512 \text{ K} \times 8} \\ &= \frac{2^1 \times 2^{20} \times 2^5}{2^9 \times 2^{10} \times 2^3} \\ &= \frac{2^{26}}{2^{22}} = 2^4 = 16\end{aligned}$$

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# 4

## Input-Output Organization



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

(c)

Interrupt occurs during the execution of a current instruction. So, CPU will be respond to a interrupt after 12 cycles.

#### T2 : Solution

(d)

Temperature sensor is a critical component in the CPU design. So it is a non-maskable interrupt.  
∴ High priority is associated.

#### T3 : Solution

(b)

Vectored interrupt contain the interrupt vector so, vector address is calculated based on this vector.

#### T4 : Solution

(a)

DMA steals the control of a data bus and address bus to transfer the data from IO to main memory.

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