

ESE GATE PSUs

State Engg. Exams

MADE EASY
WORKBOOK 2024



**Detailed Explanations of
Try Yourself *Questions***

ELECTRICAL ENGINEERING

Digital Electronics



MADE EASY
Publications

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Number Systems and Binary Codes



Detailed Explanation of Try Yourself Questions

T1. Sol.

$$\begin{array}{r} 1\ 1\ 1\ 1\ 1 \\ -\ 1\ 0\ 0\ 1\ 1 \\ \hline 1\ 1\ 0\ 0 \\ +\ 1 \\ \hline 1\ 1\ 0\ 1 \end{array}$$

$$(1101)_2 = (13)_{10}$$

Therefore, the decimal equivalent value = -13.

T2. (d)

Given that,

$$\begin{aligned} (10)_x \times (10)_x &= (100)_x \\ x \times x &= x^2 \end{aligned}$$

$$\begin{aligned} \text{and } (100)_x \times (100)_x &= (10000)_x \\ x^2 \times x^2 &= x^4 \end{aligned}$$

so, above conditions are valid for all values of x .

T3. (c)

Converting both sides into decimal

$$\begin{aligned} (2^4 \times 1 + 0 + 2^2 \times w + 2^1 \times 1 + 2^0 \times z) \times 15 &= 2^8 y + 2^6 \times 1 + 2^4 \times 1 + 2^3 \times 1 + 2^0 \times 1 \\ (18 + 4w + z) \times 15 &= 256y + 64 + 16 + 8 + 1 \\ 270 + 60w + 15z &= 256y + 89 \end{aligned}$$

Only $w = 1$, $z = 1$ and $y = 1$ satisfies.

T4. (a)

$$\begin{array}{r} 9\ 9\ 9\ 9\ 9 \\ -2\ 5\ .\ 6\ 3\ 9 \\ \hline 7\ 4\ .\ 3\ 6\ 0 \end{array}$$





Detailed Explanation of Try Yourself Questions

T1. (c)

Bulb is On when both switch S1 and S2 are in same state, either off or on.

S1	S2	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	ON

Above truth table derives EX-NOR operation.

T2. (a)

EXNOR gate on logic is called coincidence logic.

So, $f = AB + A'B'$

T3. (b)

D will be '1' majority of input is 1, so

$$D = A \oplus B \oplus C$$

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Combinational Logic Circuits



Detailed Explanation of Try Yourself Questions

T1. (c)

Since the delay is of 1 μsec the output will a square wave with time period of 2 μsec .
So, frequency = 0.5 MHz

T2. (a)

Multiplexer function, $f = X\bar{Z} + YZ$

Given Boolean function, $f = T + R$

Let $X = R$, $Y = 1$ and $Z = T$

$$\begin{aligned} f &= R\bar{T} + 1 \cdot T = R\bar{T} + T \\ &= R\bar{T} + T(1 + R) = R\bar{T} + TR + T \\ &= R(\bar{T} + T) + T = R + T \end{aligned}$$

T3. (b)

Output will be 1 if $A > B$.

- If $B = 00$ then there will be three combinations for which output will be 1 i.e. when $A = 01, 10$, or 11 .
- If $B = 01$ there will be two conditions i.e. $A = 10$ and 11 .
- If $B = 10$ there will be one condition i.e. $A = 11$.

So total 6 combinations are there for which output will be 1.

T4. (c)

T5. (b)

The number of AND gates in carry generator circuit in 'n' bit adder = $\frac{n(n+1)}{2}$

If $n = 4 \Rightarrow \frac{4(5)}{2} = 10$.

The number of OR gates in carry generator circuit in 'n' bit adder = n.

If $n = 4 \Rightarrow 4$

T6. (b)

So, the input to adder is y and 1's complement x since carry input in 1.
So, output is complement of $x + 1$, so output is $y - x$.

T7. (b)

P_1	P_2	a	b	c	d	e	f	g
0	0	1	1	1	1	1	1	0
0	1	1	0	1	1	0	1	1
1	0	1	1	0	1	1	0	1
1	1	1	0	0	1	1	1	1

$$a = 1$$

$$b = \bar{P}_2 \quad \dots 1 \text{ (NOT)}$$

$$c = \bar{P}_1 \quad \dots 1 \text{ (NOT)}$$

$$d = 1 = c + e$$

$$e = P_1 + \bar{P}_2 \quad \dots 1 \text{ (OR)}$$

$$f = \bar{P}_1 + P_2 \quad \dots 1 \text{ (OR)}$$

$$g = P_1 + P_2 \quad \dots 1 \text{ (OR)}$$

$\Rightarrow$

$$g = P_1 + P_2$$

$$d = 1 = c + e$$

T8. (d)

2 – NOT gates

3 – OR gates

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Sequential Circuits



Detailed Explanation of Try Yourself Questions

T1. (76.92)

Total propagation delay
 $= (t_{pd} + t_{\text{set-up}})_{\text{max}} = 8\text{ns} + 5\text{ns} = 13\text{ns}$
 $\therefore$ Frequency of operations
 $= \frac{1000}{13} \text{MHz} = 76.92 \text{MHz}$

T2. (c)

T3. (6)

JK Flip-flop 1 and 2 form a synchronous sequential circuits and they are synchronized with the output of 0th JK Flip-flop.

J_1	K_1	J_2	K_2	Q_2	Q_1	Q_0	
1	1	0	1	0	0	0	$\left. \begin{array}{l} T_1 \\ T_2 \\ T_3 \end{array} \right\}$
1	1	1	1	0	1	1	
0	1	0	1	1	0	0	
1	1	0	1	0	0	0	

Number of cycles = 3 i.e. equal to 6 clock cycles.

T4. (d)

$D = \bar{X}Z + Y\bar{Z}$, $D = \bar{K}Q + J\bar{Q}$
 $Y = J$, $X = K$, $D = Q$ (for D flip-flop)

T5. (d)

Trick up/down = $CP \oplus Q$, 1 for up and 0 for down.

CP = (clock pulse)

Q = (O/P)

0 = -ve edge; $Q = 1$

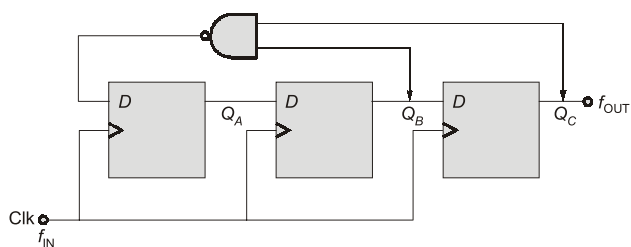
1 = +ve edge; $\bar{Q} = 1$

= $1 \oplus 1 = 0$ (down counter)

Counting sequence

1	1	1
1	1	0
1	0	1
1	0	0
0	1	1 (preset state) so Mod 5

T6. (b)



$\overline{Q_B} \cdot \overline{Q_C}$	Q_A	Q_B			
D_A	D_B	D_C	Q_A	Q_B	Q_C
			0	0	0
1	0	0	1	0	0
1	1	0	1	1	0
1	1	1	1	1	1
0	1	1	0	1	1
0	0	1	0	0	1
1	0	0	1	0	0
1	1	0	1	1	0

} Cycle
Repeated

mod 5 counter

So, frequency will be divided by 5.

T7. Sol.

Clock	Q_A	Q_B	Q_C	Q'_A	Q'_B	Q'_C	$Q_A \oplus Q'_A$	$Q_B \oplus Q'_B$	$Q_C \oplus Q'_C$	Z
0	1	0	0	1	0	0	0	0	0	0
1	0	1	0	1	1	0	1	0	0	1
2	0	0	1	1	1	1	1	1	0	1
3	1	0	0	0	1	1	1	1	1	1
4	0	1	0	0	0	1	0	1	1	1
5	0	0	1	0	0	0	0	0	1	1
6	1	0	0	1	0	0	0	0	0	0

The output Z will again become zero after 6 clock cycles.

T8. (c)

The counter represents a Johnson counter. Thus, total number of states = $2n$. Where $n = 3$.

Therefore the MOD of the counter = $2 \times 3 = 6$

T9. (d)

In a 2^8 Counter the range would be from 0-255.

Hence to go from 10101100 (172) to 00100111 (39), the counter has to go initially from 172 to 255 and then from 0 to 39.

Hence to go from 172 to 255, $255 - 172 = 83$ Clock pulses would be required.

From 255 to 0, again 1 clock pulse would be required.

Then from 0 to 39, 39 clock pulses would be required.

Hence in total $83 + 1 + 39 = 123$ Clock pulses would be required.



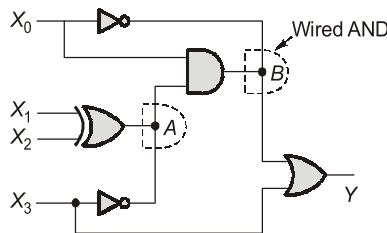
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Integrated-Circuit Logic Families



Detailed Explanation of Try Yourself Questions

T1. (8)



$$A = (X_1 \oplus X_2) \bar{X}_3$$

$$B = [(X_1 \oplus X_2) \bar{X}_3 X_0] \cdot \bar{X}_0 = 0$$

$$Y = B + X_3 = 0 + X_3 = X_3$$

Out of 16 possible combinations of $X_3 X_2 X_1 X_0$, X_3 will be high for 8 combinations. So, Y will be high for 8 combinations.

T2. (a)

T3. (b)

It is CMOS gate where 2 PMOS are parallel and in series with 2 NMOS (series combination of NMOS).

It is equivalent to NAND gate.

Series combination of NMOS equivalent to parallel combination of PMOS.

T4. (c)

Truth table:

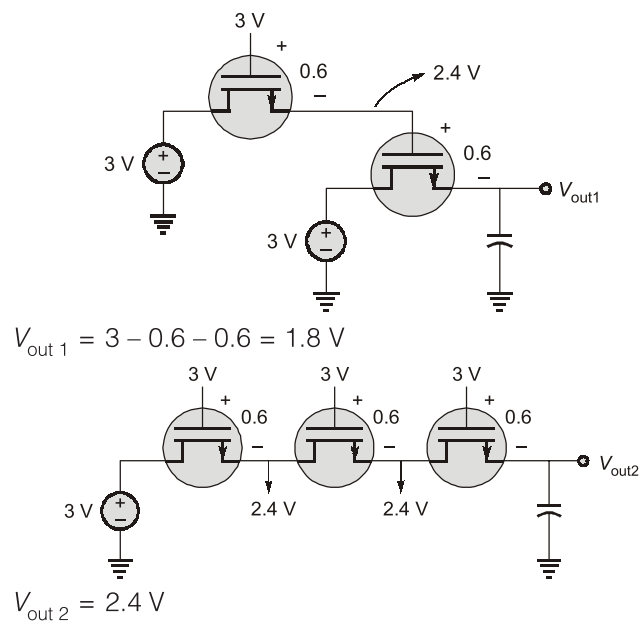
X	Y	V_0
0	0	1
0	1	0
1	0	0
1	1	0

$$V_0 = \overline{X+Y}$$

T5. (a)

Series combination of n-mos is equivalent to AND and parallel combination is equivalent to OR.

$$\text{So, } Y = \overline{C} \cdot (A+B) = \overline{C} + \overline{(A+B)} = \overline{C} + \overline{A} \cdot \overline{B}$$

T6. (c)**T7. (a)****T8. (c)**

- HTL → High noise immunity
- CMOS → Highest fanout
- I^2L → Lowest of product power and delay
- ECL → Highest speed of operation

T9. (a)

For TTL logic floating input = 1

$$\therefore Y = (AB + 1)' = \overline{AB} \cdot 0 = 0$$

T10. (a)

ECL is the fastest logic family.

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Detailed Explanation of Try Yourself Questions

T1. (a)

Sequence of Johnson counter is

Q_2	Q_1	Q_0	D_2	D_1	D_0	V_0
0	0	0	0	0	0	0
1	0	0	1	0	0	4
1	1	0	1	1	0	6
1	1	1	1	1	1	7
0	1	1	0	1	1	3
0	0	1	0	0	1	1
0	0	0	0	0	0	0

T2. (a)

- (i) Conversion time is the time taken for a new digital output to appear in response to a change in the input voltage.
- (ii) Flash converter is the fastest converter. It uses no clock signal.
- (iii) **Type of N -bit ADC** **Max. conversion time**
 - Successive approximation N clock cycles
 - Counter ramp $2^N - 1$ clock cycles

T3. (c)

Initial stage of the counter = $(111)_2 = (7)_{10}$

So output will be equal to 7 V.

Next state of counter = $(110)_2 = (6)_{10}$

So output should be = 6 V

But output is 3 V that means LSB of counter is connected to MSB of DAC and MSB of counter is connected to LSB of DAC.

Similarly next state of counter = $(101)_2 = (5)_{10}$

Input to DAC = $(101)_2 = (5)_{10}$

So output = 5 V

When counter goes to $(100)_2$ then input to DAC = $(001)_2 = (1)_{10}$

So output = 1 V

So connections are not proper.

T4. (c)

No. of comparators in a flash ADC is equal to $2^n - 1$ where n = no. of bits.

$$2^4 - 1 = 15$$

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