2020

RANK Improvement WORKBOOK

Answer key and Hint of Objective & Conventional *Questions*

Electrical Engineering

Digital Electronics

MADE EASY Publications

1 Boolean Algebra, Logic Gates

LEVEL 1 Objective Solutions

1. (c)

2. (c)

3. (c)

LEVEL 2 Objective Solutions

4. (1)

5. (c)

6. (d)

7. (a)

8. (c)

9. (b)

■■■■

LEVEL 3 Conventional Solutions

Solution : 1

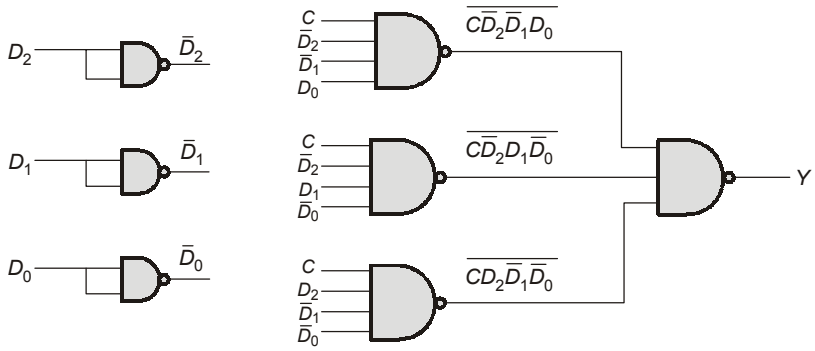
(i)

$$AB + AC + B\bar{C} = AB(C + \bar{C}) + AC + B\bar{C} \qquad (\because C + \bar{C} = 1)$$
$$= ABC + AC + AB\bar{C} + B\bar{C}$$
$$= (B + 1)AC + (A + 1)B\bar{C} \qquad (\because A + 1 = 1)$$
$$= AC + B\bar{C}$$

(ii)

$$\overline{AB + BC + CA} = \left(\overline{AB}\right)\left(\overline{BC}\right)\left(\overline{CA}\right)$$
$$= (\bar{A} + \bar{B})(\bar{B} + \bar{C})(\bar{C} + \bar{A})$$
$$= (\bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B} + \bar{B}\bar{C})(\bar{C} + \bar{A})$$
$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$$
$$= \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A} + \bar{A}\bar{B}\bar{C}$$
$$= \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}(1 + \bar{B})$$
$$= \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A} \qquad (\because 1 + \bar{B} = 1)$$

Solution : 2



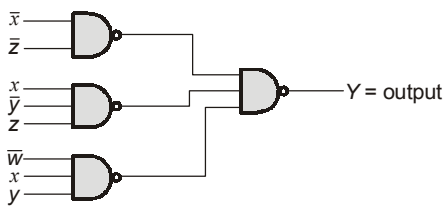
Solution : 3

(i) Prime implicates: $\bar{w}\bar{x}\bar{z}, x\bar{y}z, \bar{w}xy, w\bar{x}\bar{z}$

(ii) Minimal representation: $\bar{w}\bar{x}\bar{z} + w\bar{x}\bar{z} + x\bar{y}z + \bar{w}xy$

$$= \underbrace{\bar{x}\bar{z}} + \underbrace{x\bar{y}z} + \underbrace{\bar{w}xy}$$

(iii) Two-level realization using NAND Gates only,



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2 Combinational Circuits

LEVEL 1 Objective Solutions

1. (a)

2. (c)

LEVEL 2 Objective Solutions

3. (a)

4. (a)

5. (12)

6. (a)

7. (50)

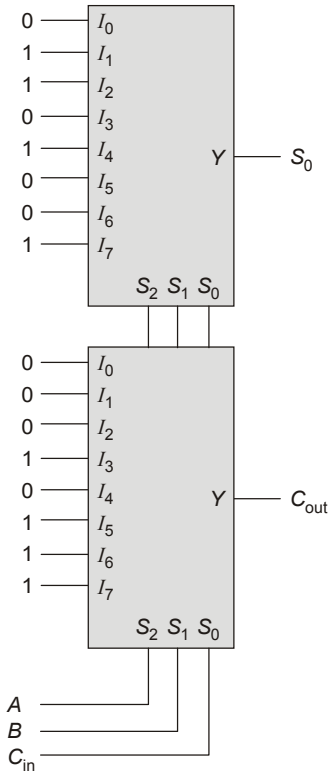
8. (a)

■■■■

LEVEL 3 Conventional Solutions

Solution : 1

(i)



(ii) $\therefore$ $P_1 = \bar{a}\,b$

$P_2 = a\,c$

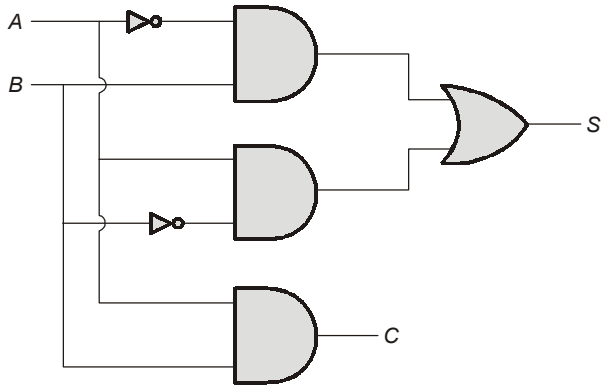
$P_3 = b\bar{c}$

If $P_4 = \bar{a}\bar{b}$, then $P_5 = bc$

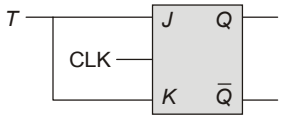
and if $P_4 = b\,c$, then $P_5 = \bar{a}\bar{b}$

Solution : 2

(i)

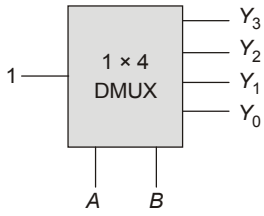


(ii)



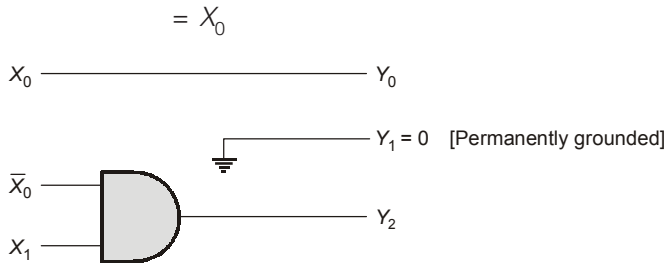
Toggle flip-flop

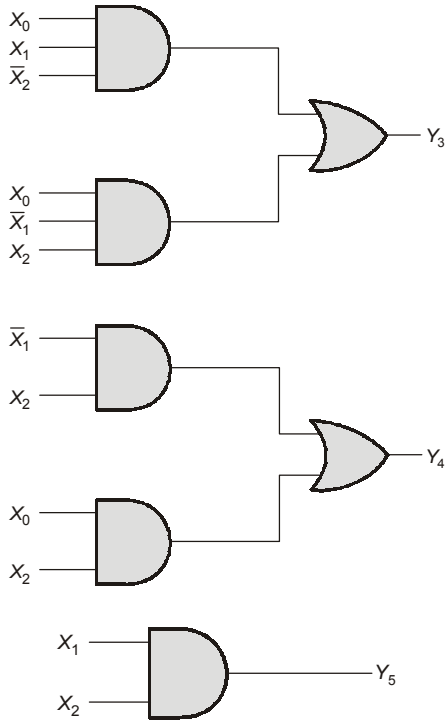
(iii)



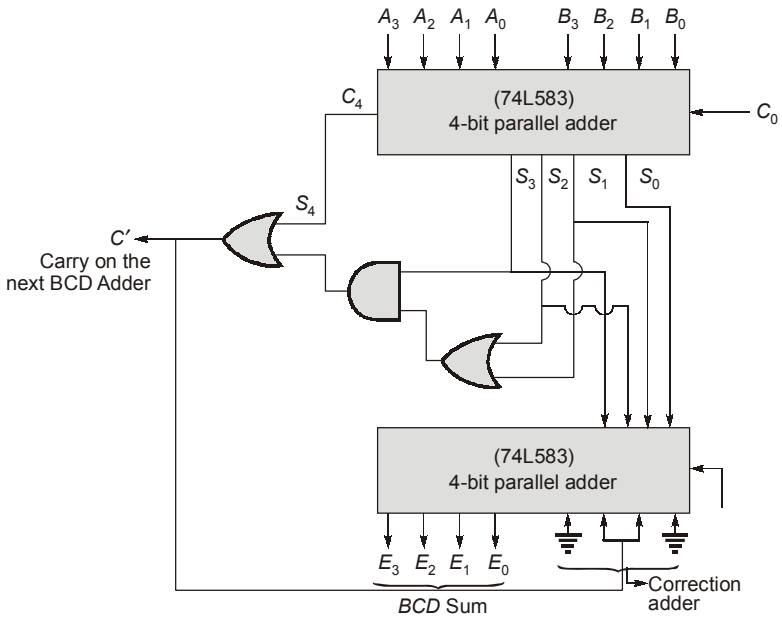
2 to 4 decoder

Solution : 3

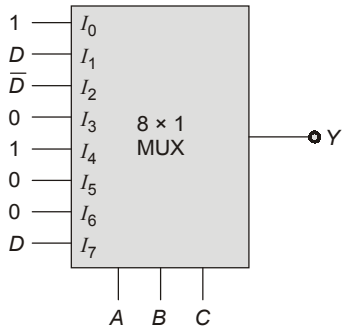



X_0
X_1
$\overline{X}_2$
Y_3
X_0
$\overline{X}_1$
X_2
$\overline{X}_1$
X_2
Y_4
X_0
X_2
X_1
X_2
Y_5

Solution : 4

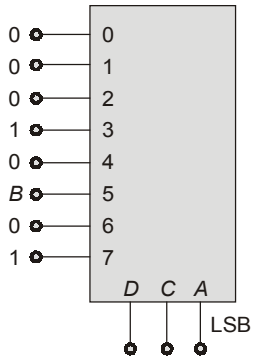

A_3 A_2 A_1 A_0
B_3 B_2 B_1 B_0
C_4
(74L583)
4-bit parallel adder
C_0
S_3 S_2 S_1 S_0
S_4
C'
Carry on the
next BCD Adder
(74L583)
4-bit parallel adder
E_3 E_2 E_1 E_0
BCD Sum
Correction
adder

Solution : 5



Solution : 6

(a)



(b) It can not be realized with a 4 to 1 multiplexer as 5^{th} and 7^{th} lines are being used.

■■■■

3 Sequential Circuits

LEVEL 1 Objective Solutions

1. (d)

2. (10)

LEVEL 2 Objective Solutions

3. (0.8415)

4. (b)

5. (c)

6. (6)

7. (b)

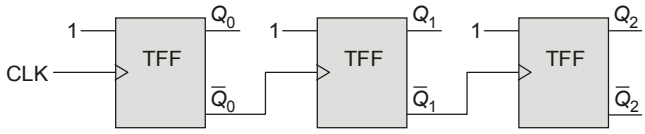
8. (a)

9. (d)

■■■■

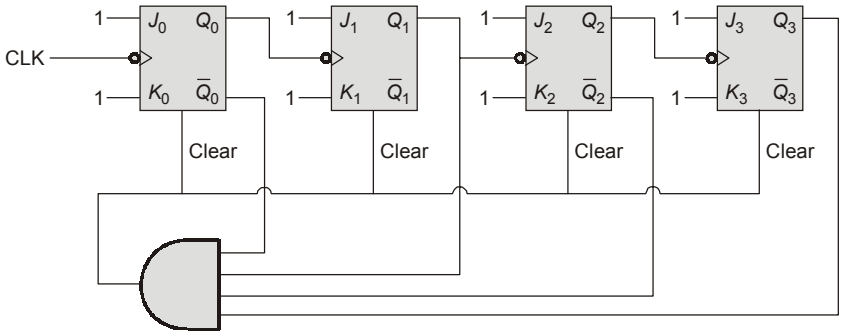
LEVEL 3 Conventional Solutions

Solution : 1



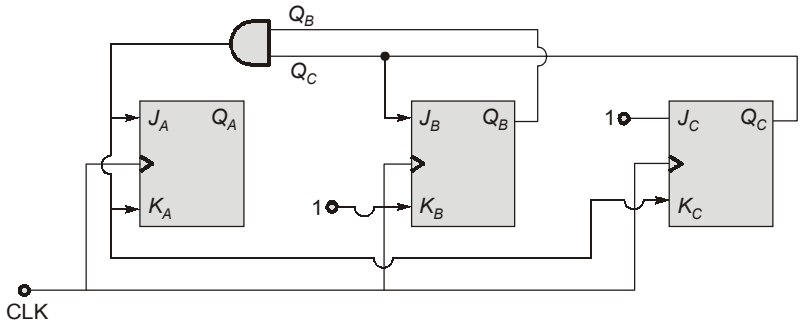
Logic Diagram

Solution : 2



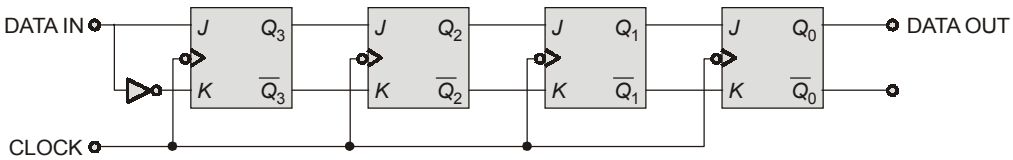
Solution : 3

Realizations of counter using above results:

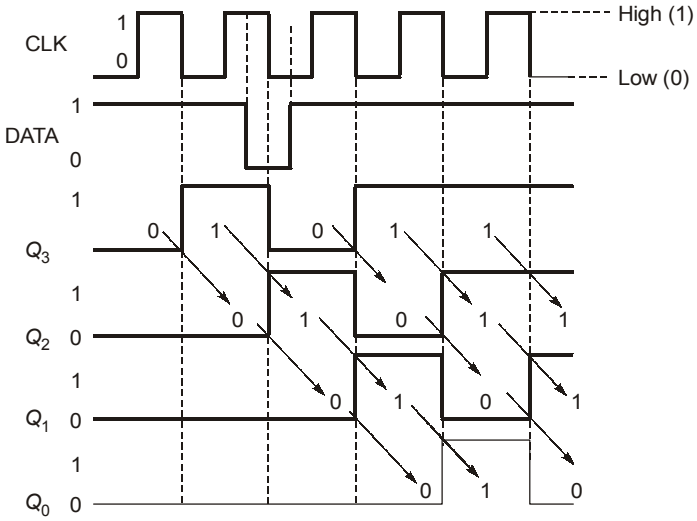


Solution : 4

The diagram of a 4-bit shift register using JK flip-flops is shown below:

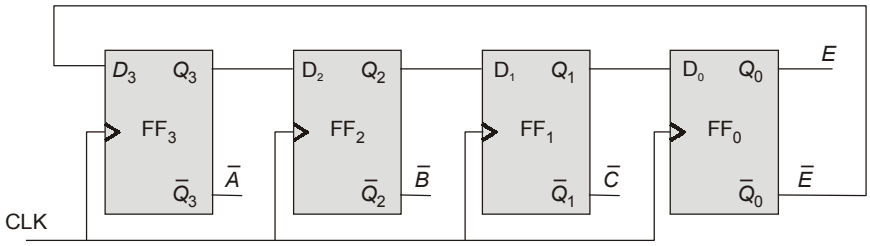


The output waveforms of all flip-flops as for the given data are shown below

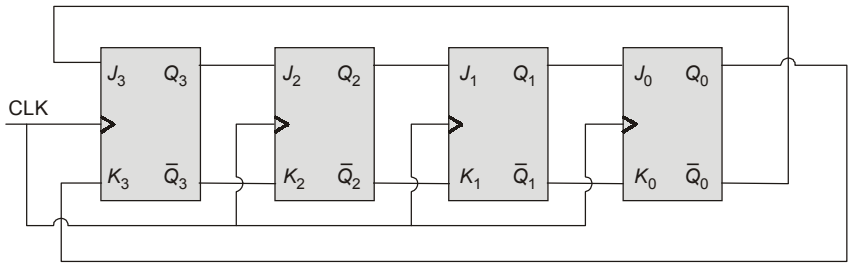


Solution : 5

Johnson counter is twisted ring counter

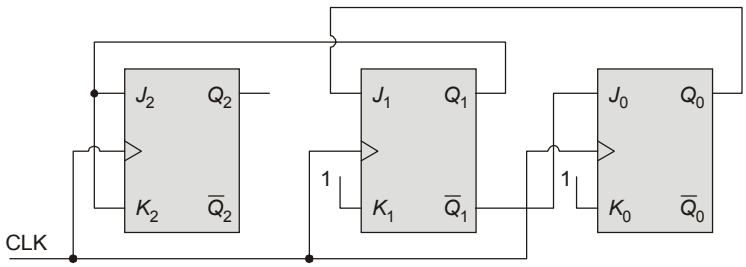


4 bit Ring counter using D flip-flop



4 bit Ring counter using J-K flip-flop

Solution : 6



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4 A/D and D/A Converters

LEVEL 1 Objective Solutions

1. (a)

LEVEL 2 Objective Solutions

2. (a)

3. (a)

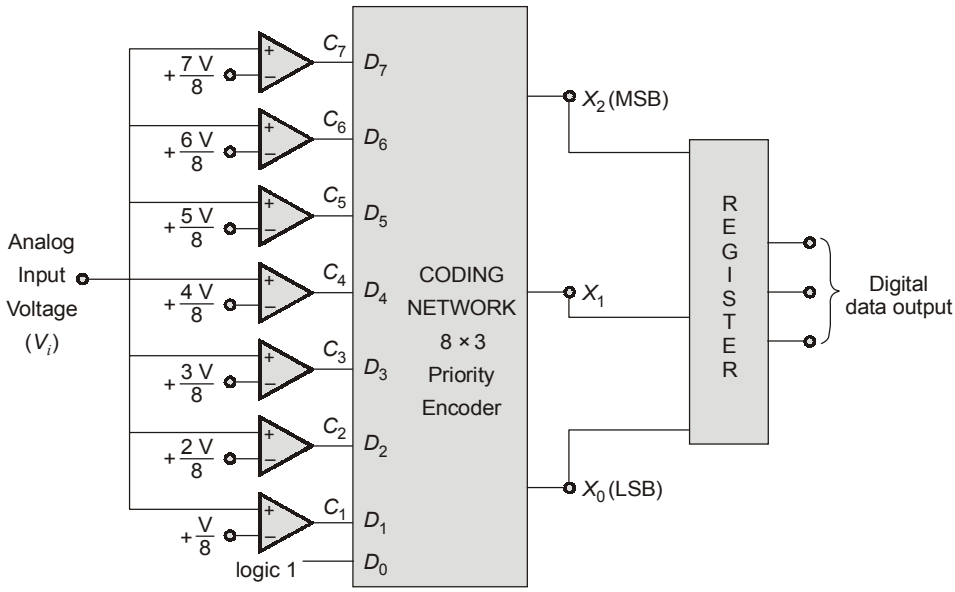
■■■■

Solution : 1

This type of ADC uses an array of comparators connected in parallel, each comparator switching on in a definite ratio of the reference voltage.

Simultaneous 3-bit *A*/*D* converter: "Flash type Converter"

The block diagram of simultaneous 3-bit *A*/*D* converter is shown below:



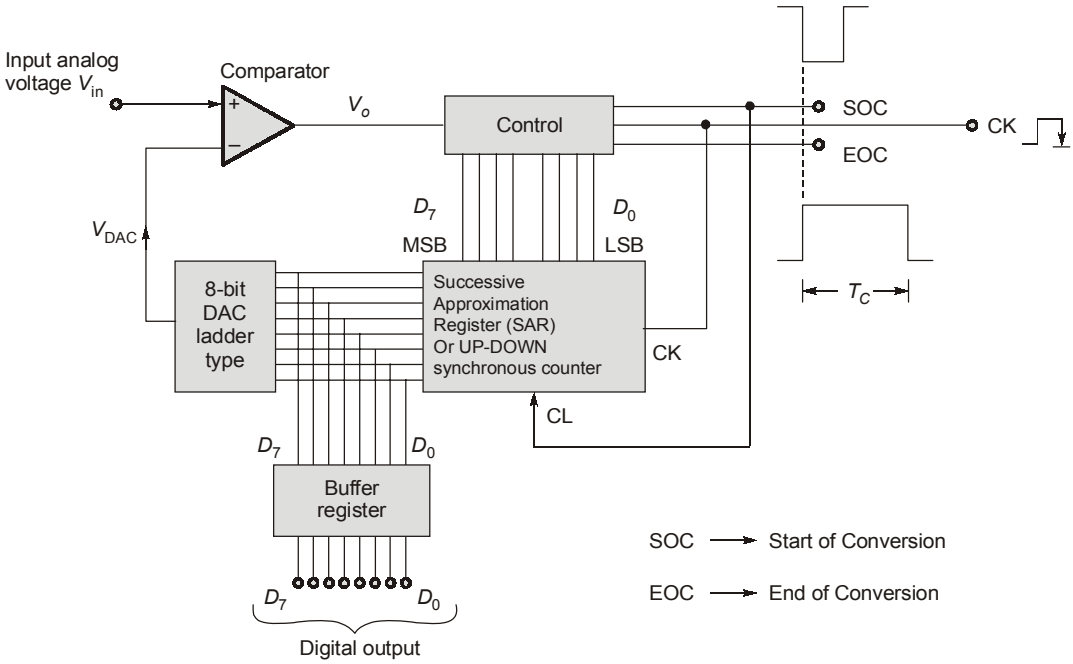
⇒ The simultaneous 3-bit *A*/*D* converter uses 7 comparators to convert an analog input voltage into the digital output. The reference voltages used are $\frac{V}{8}, \frac{2V}{8}, \ldots, \frac{7V}{8}$ for any input voltage between 0 and $+V$.

⇒ If the analog input voltage (V_i) exceeds the reference voltage of a comparator, the output of the comparator goes high. i.e. 1 and vice-versa.

⇒ The outputs of the comparators are fed into a coding network which gets stored in register of 3 bit and provide the digital output of 3-bit corresponding to the input analog voltage.

Solution : 2

The 8-bit successive approximation *A*/*D* converter is shown below



Solution : 3

Dual-slope < single-slope < successive approximation < flash

maximum conversion time for converting *n*-bit

$$= n \times T_{CLK} = 8 \times \frac{1}{f_{CLK}} = 8 \times 10^{-6} \text{ second} = 8\ \mu\text{-sec.}$$

Solution : 4

(i) Resolution = 1 mV as transducer is able to distinguish a minimum change of 1 mV in its signal input.

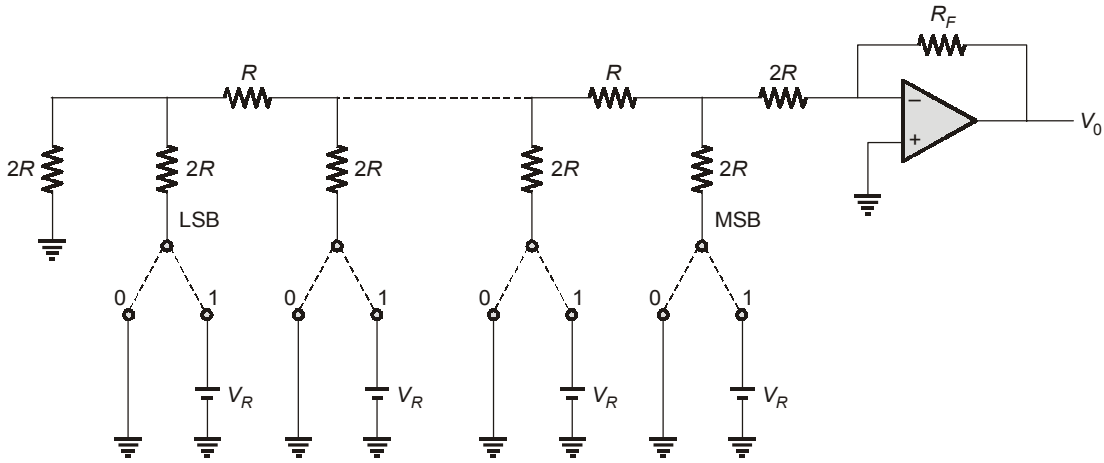
(ii) Total number of quantized levels = $\frac{10}{1 \times 10^{-3}} = 10000$

So, minimum number of bits required = 14 [As $2^{13} < 10000, 2^{14} > 10000$]

(iii) Quantization interval = $\frac{1}{2^{(\text{Number of bits})}} = \frac{1}{2^{14}} = 6.1 \times 10^{-5}$ V

(iv) Number of decision levels = $2^n - 1 = 2^{14} - 1 = 16383$

Solution : 5



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5 Logic Families

LEVEL 1 Objective Solutions

1. (b)

LEVEL 2 Objective Solutions

2. (0.63)

3. (b)

4. (c)

■■■■

Solution : 1

Differences between ECL and TTL are as follows:

1. In ECL, the positive end of the supply is connected to ground while in TTL, the negative end of the supply is connected to ground.
2. In TTL, the inputs are connected to emitter while in ECL the inputs are connected to bases
3. ECL uses transistors in difference amplifier configuration while TTL uses a multiple emitter transistor.

Merits and demerits of TTL:

Merits:

1. Current drawn from the input source is very small.
2. It has high output drive capability.
3. No damage is done to TTL devices if inputs are left unconnected.

Demerits:

1. High power consumption.
2. High current drain.

Merits and demerits of ECL:

Merits:

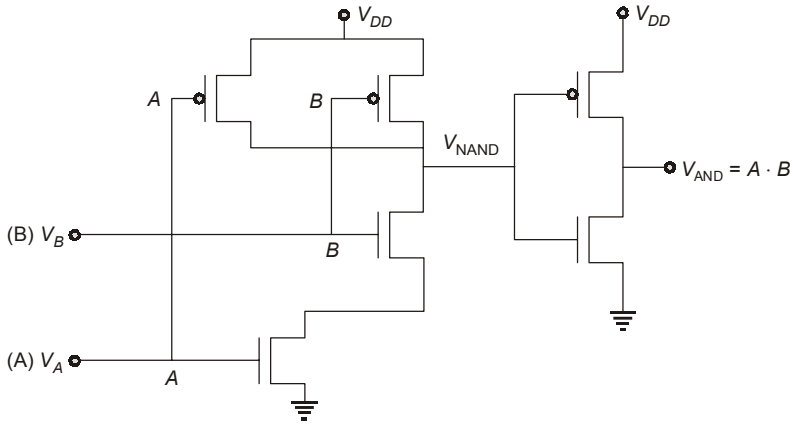
1. It is the fastest of all logic families.
2. Input impedance is high.
3. Output impedance is low
4. High fanout.
5. Outputs of ECL gates can be connected to obtain additional logic.

Demerits:

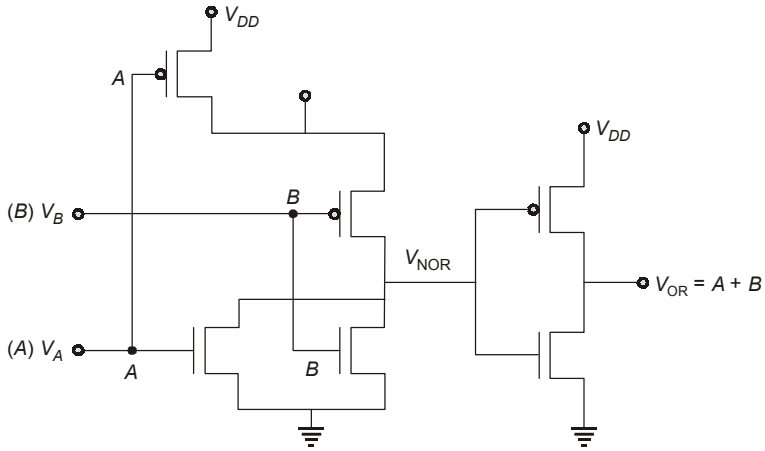
1. High power consumption.
2. ECL gates are not readily compatible with other logic families.

Solution : 2

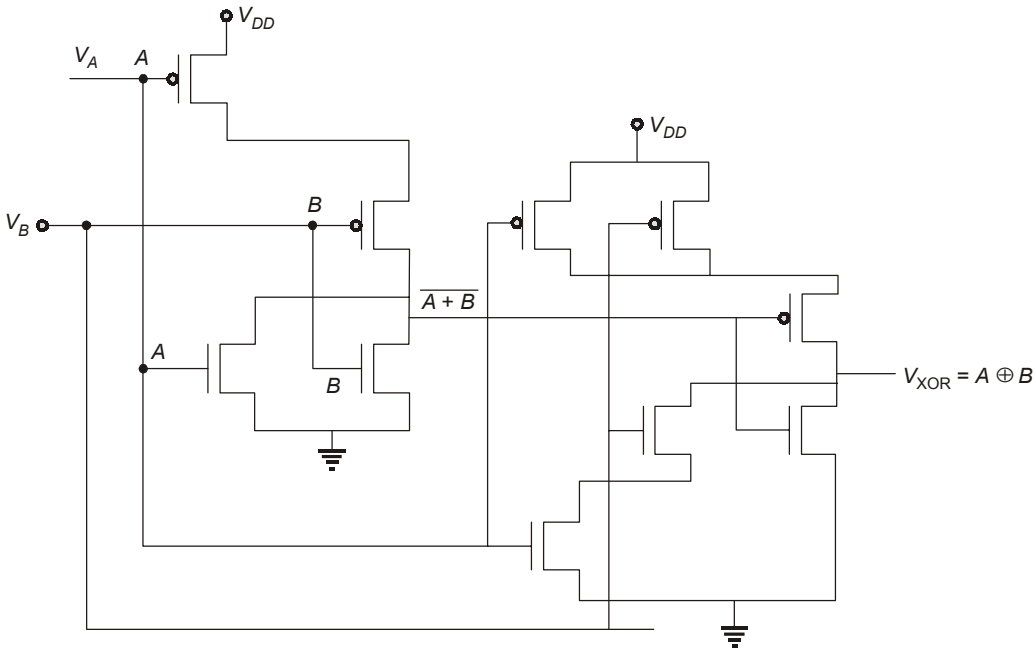
(i) $Y = A \cdot B$



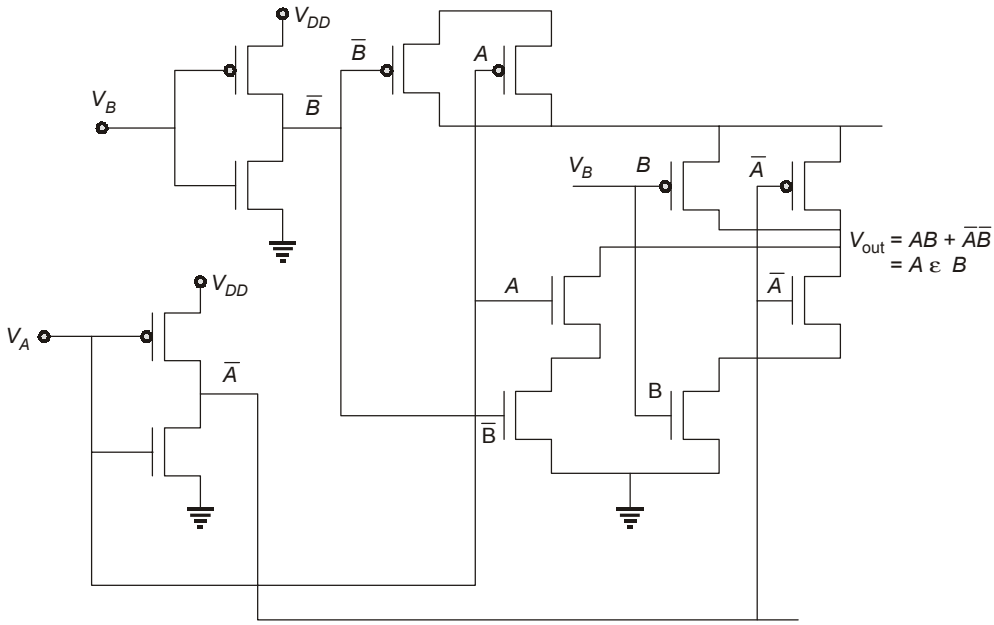
(ii) $Y = A + B$



(iii) $Y = A \oplus B$

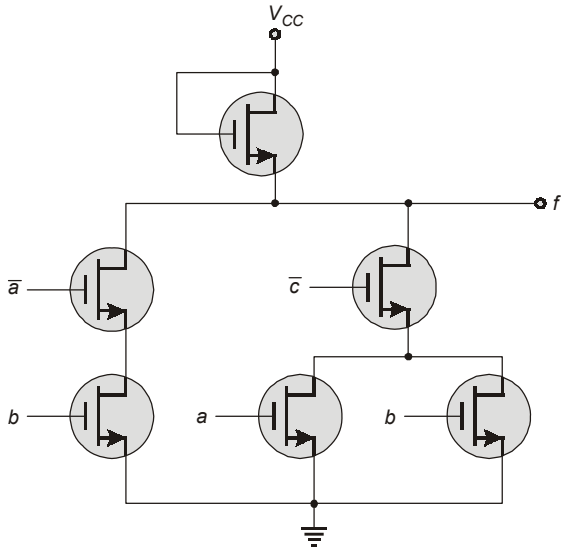


(iv) $Y = A \odot B$



Solution : 3

As single NMOS acts as an inverter, implementing $\overline{f}$ would realize $f(a, b, c)$



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