

2020

RANK *Improvement* **WORKBOOK**



**Detailed Explanations of
Objective & Conventional Questions**

Electronics Engineering
Advanced Electronics



MADE EASY
Publications

1

Doping and Oxidation

LEVEL 1 Objective Solutions

1. (a)

2. (b)

3. (a)

4. (b)

5. (d)

6. (a)

7. (c)

8. (c)

9. (d)

10. (a)

11. (c)

12. (b)

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13. (c)

14. (b)

15. (c)

16. (d)

17. (d)

18. (a)

19. (d)

20. (c)

21. (b)

22. (a)

23. (a)

24. (c)

25. (c)

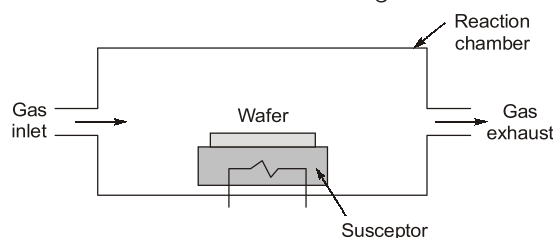
26. (b)

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LEVEL 2 Conventional Solutions**Solution : 1**

- Chemical Vapor Deposition (CVD) is an extremely versatile process that can be used to process almost any metallic or ceramic compound. For example, CVD is used to deposit polysilicon layer in CMOS fabrication.
- Materials are deposited from the gaseous state during CVD and these precursor gases are often diluted in carrier gases and delivered into the reaction chamber. As they pass over or come into contact with a heated substrate, they react or decompose forming a solid phase and are deposited onto the substrate. The substrate temperature is critical and can influence what reactions will take place.
- The basic steps in CVD film growth are production of appropriate source gas, transport of gas to substrate, adsorption of gas on substrate, reaction on substrate and the transport of waste products away from substrate. The growth of films depends on all these kinetics.

A simple prototype thermal CVD reactor is shown in the figure below:



A simple prototype thermal CVD reactor

A CVD apparatus consists of the following basic components:

- **Gas delivery system:** For the supply of precursors to the reactor chamber
- **Reactor chamber:** Chamber within which deposition takes place
- **Substrate loading mechanism:** A system for introducing and removing substrates
- **Energy source:** Provides the energy/heat that is required to get the precursors to react/decompose
- **Vacuum system:** For removal of all other gaseous species other than those required for the reaction/deposition.
- **Exhaust system:** System for removal of volatile by-products from the reaction chamber.
- **Exhaust treatment systems:** In some instances, exhaust gases may not be suitable for release into the atmosphere and may require treatment or conversion to safe/harmless compounds.
- **Process control equipment:** Gauges, controls etc. to monitor process parameters such as pressure, temperature and time. Alarms and safety devices would also be included in this category.

Operation: First the wafers are kept in the chamber and the chamber is evacuated. Then the wafers will be heated to the desired temperature. Next the gases are supplied and they react only on the surface of the wafer and deposit the material.

Example: $\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}$ [used in silicon manufacturing]

(Trichloro Si Lane)

$\text{SiHCl} \rightarrow \text{Si} + 2\text{H}_2$ (using in polysilicon deposition)

(Si Lane)



2

Silicon Manufacturing, Photolithography and Fabrication Sequences

LEVEL 1 Objective Solutions

1 (c)

2. (c)

3. (b)

4. (d)

5. (a)

6. (b)

7. (c)

8. (d)

9. (a)

10. (d)

11. (c)

12. (c)

13. (a)

14. (d)

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3

Sequence Detectors

LEVEL 1 Objective Solutions

1. (d)

2. (d)

3. (d)

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4

8051 Microcontroller and Embedded System

LEVEL 1 Objective Solutions

1. (c)

2. (a)

3. (a)

4. (a)

5. (d)

6. (b)

7. (d)

8. (c)

9. (d)

10. (a)

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11. (d)

12. (d)

13. (b)

14. (b)

15. (b)

16. (b)

17. (c)

18. (b)

19. (b)

20. (b)

■■■■

LEVEL

2

Conventional Solutions

2



2

2

8-bit registers. The serial data buffer is actually two separate registers : a transmit buffer and a receiver buffer register.

The 8051 has been provided with 4 banks of working registers. Each bank consists of 8 working registers, R0 - R7. Physically these banks occupy the first 32 bytes of on-chip data RAM (address 0 - 1 F hex). Only one bank is active at a time. Bits 3 and 4 of PSW decide which bank is to be made active. As the 8051 is a bit as well as byte microcontroller, some of its registers are both bit as well as byte addressable.

I/O lines : Most of the 8051 microcontrollers contain four 8-bit parallel ports : P0, P1, P2 and P3. Altogether there are 32 I/O lines. All ports in 8051 are bidirectional. The I/O lines of 8051 are not simply input/output lines, rather they are multifunctional lines. If an application does not need any external memory besides on-chip memory, then all four ports can be used as input/output ports. If external memory is used, then Port 0 and Port 2 act as a multiplexed address/data bus. Two pins of Port 3 act as Rx/D and Tx/D for serial data transmission. Two pins of Port 3 can be used as external input for timers, one for Timer 0 and one for Timer 1. Two pins of Port 3 can be used as external interrupts.

The 8051 interrupts: The 8051 microcontrollers have 4-level priority interrupts. The important interrupt sources are : one from the serial port, two from timers, two from external interrupts INT0 and INT1. Each of the interrupts can individually be enabled/disabled by settling/clearing a bit in the special function register IE (Interrupt Enable). The IE register also contains a global disable bit, which disables all the interrupts. Each interrupt can also be programmed to one of the priority Register). A low-priority interrupt can be interrupted by a high-priority interrupt, but it can not be interrupted by another low-priority interrupt. A high-priority interrupt cannot be interrupted by a low-priority interrupt.

Boolean Processor : The ALU of 8051 can process one-bit data types besides 8-bit data types. Individual bits can be set, cleared, complemented, moved, tested and used in logic computations. These features are very useful in control applications. Such applications make use of algorithms involving Boolean (true/false) input/output variables. Due to this type of capability the 8051 is said to possess Boolean Processor capability.

Solution : 3

The PSW the program status word is an 8-bit register in 8051 microprocessor. It is also referred to as flag register. In PSW only 6 out of 8 bits are used. The two unused bits are the user defined flag. Four of the flags are the conditional flag and they are CY (carry flag), AC (auxiliary carry), P (parity) and OV (over flow).

CY	AC	FO	RS1	RS0	OV	-	P
----	----	----	-----	-----	----	---	---

CY	-	PSW.7	-	Carry flag
AC	-	PSW.6	-	Auxiliary carry
FO	-	PSW.5	-	Available for user for general purpose
RS1	-	PSW.4	-	Resistor bank selector bit-1
RS0	-	PSW.3	-	Resistor bank selector bit-0
OV	-	PSW.2	-	Over flow flag
	-	PSW.1	-	User defined bit
P	-	PSW.0	-	Parity flag

RS1	RS0	Register bank	Address
0	0	0	
0	1	2	
1	0		
1	1	3	

The carry flag: This flag is set whenever there is a carry-out from the D7bit. The flag bit is affected after an 8-bit addition or subtraction.

Auxiliary carry: If there is a carry from D3 to D4 during an ADD or SUB operation, this bit is set; otherwise.

Parity flag: The parity reflects the number of 1s in the A (accumulator) register only. If the A register contains an odd number of 1s then $P = 1$.

Overflow flag: The flag is set whenever the result of a signed number operation is too large, causing the high order bit to overflow into the sign bit.

Solution : 4

```

MOV    R0, #50H
MOV    R1, #10H
MOV    B, #0
BACK:  MOV    A, #R0
        CJNE  A, B, LOOP
        JC    LOOP1
        MOV    B, A
        INC R0
        DJNZ  R1, BACK
        SJMP  NEXT
LOOP1: INC R0
        DJNZ  R1, BACK
        MOV    A, B
        MOV    60H, A
        END
    
```

Solution : 5

```

MOV R2, #10H    ; R2 is used as counter
MOV R0, #45H    ; R0 points to first source location
MOV R1, #79H    ; R1 points to first destination location
BACK: MOV A, @R0 ; Move source byte to A
      ADD A, #02 ; Add 2 to it
      MOV @R1, A ; Move it to destination
      INC R0
      DEC R1
      DJNZ R2, BACK
    
```

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