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ESE 2019 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

Electronics & Telecommunication Engineering

Test-2: Network Theory + Microprocessors and Microcontroller

Digital Circuits-1 + Control Systems-1

Name : .....

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Student's Signature

Instructions for Candidates

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. Answer must be written in English only.
3. Use only black/blue pen.
4. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
5. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
6. Last two pages of this booklet are provided for rough work. Strike off these two pages after completion of the examination.

FOR OFFICE USE

Question No.	Marks Obtained
Section-A	
Q.1	41
Q.2	—
Q.3	—
Q.4	40
Section-B	
Q.5	48
Q.6	42
Q.7	—
Q.8	45
Total Marks Obtained	216

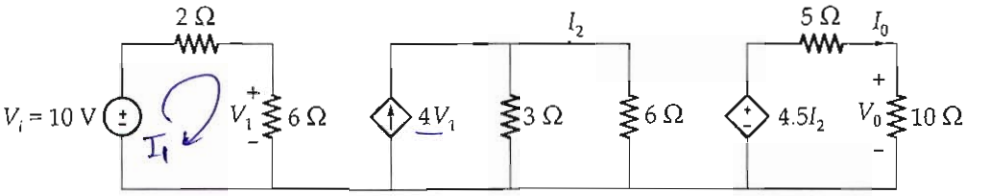
→ Good writing skills
→ V. Good handwriting.

Signature of Evaluator .....

Cross Checked by .....

Section A : Network Theory + Microprocessors and Microcontroller

Q.1 (a) Consider the circuit shown below:



Determine the output voltage (V_0), output current (I_0) and voltage gain (V_0/V_i).

[12 marks]

$I_1 = \frac{10}{8}$ Amp

$V_1 = \frac{10}{8} \times 6 = 7.5$V

$4V_1 = 7.5 \times 4 = 30$ Amp

$I_2 = \frac{3 \times 30}{9}$

$I_2 = 10$ Amp

$4.5I_2 \Rightarrow 45$ V

$I_0 = \frac{45}{15}$

$I_0 = 3$ Amp

$V_0 = 10 \times I_0$

$V_0 = 10 \times 3$

$V_0 = 30$ V

Voltage gain =

$$\frac{V_o}{V_i} = \frac{I_o \times 10}{V_i}$$

$$\frac{V_o}{V_i} = \frac{3 \times 10}{10}$$

$$\boxed{\frac{V_o}{V_i} = 3}$$

So output :-

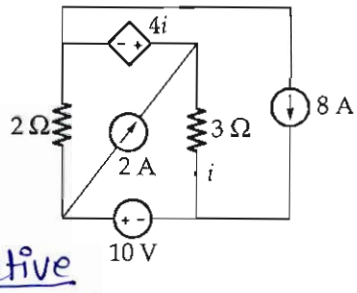
$$\boxed{V_o = 30\,V}$$

$$\boxed{I_o = 3\,Amp}$$

$$\boxed{\frac{V_o}{V_i} = 3}$$

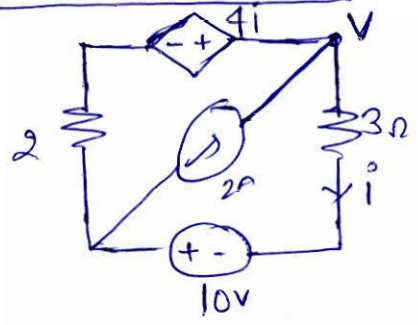
10

Q.1 (b) For the circuit shown in the figure below, find the current (i), using superposition theorem.



[12 marks]

10V source is active



Nodal at V

$$\frac{V-4i}{2}+\frac{V+10}{3}=2 \quad \text{—①}$$

$$i=\frac{V+10}{3}$$

$$V=3i-10 \quad \text{—②}$$

put ② in ①

$$\frac{3i-10-4i}{2}+i=2$$

$$-\frac{10+i}{2}+i=2$$

$$-10-i+2i=4$$

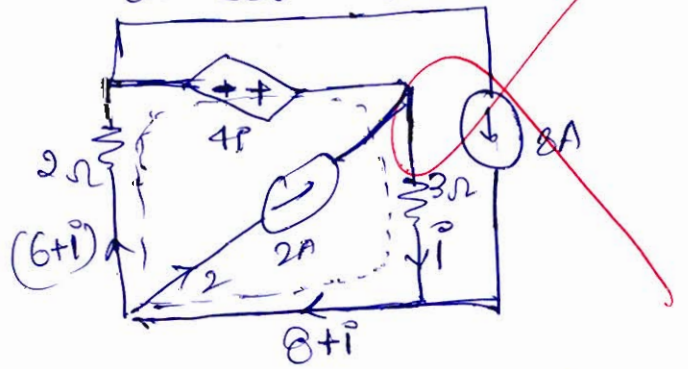
$$i_1=14 \text{ Amp}$$

wrong approach

cal error

So $i_1 = 14$ Amp

When 8A source is active



KVL in dotted line

$$-4i+3i+2(6+i)=0$$

$$-i+12+2i=0$$

$$i=-12 \text{ Amp}$$

$\boxed{i_2 = -12 \text{ Amp}}$

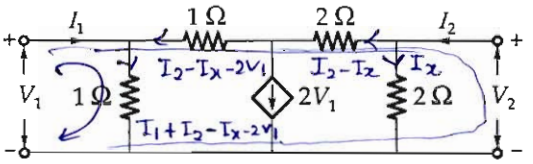
SO $i = i_1 + i_2$

$i = 14 - 12$

$\boxed{i = 2 \text{ Amp}}$

$I_2 - I_x = 2V_1 + I'$

Q.1 (c) Obtain Z-parameter matrix for the circuit shown in the figure below:



[12 marks]

Sol→ From the diagram

$$-V_1 + I_1 + I_2 - I_x - 2V_1 = 0$$

$$\boxed{+3V_1 = I_1 + I_2 - I_x} \quad \text{—— (1)}$$

$$V_2 = 2I_x \quad \text{—— (2)}$$

KVL at dotted line

$$-V_1 - 1(I_2 - I_x - 2V_1) - 2(I_2 - I_x) + V_2 = 0$$

$$V_1 + I_2 - I_x - 2V_1 + 2I_2 - 2I_x - V_2 = 0$$

$$3I_x = -V_1 + 3I_2 - V_2$$

$$I_x = \frac{-V_1 + 3I_2 - V_2}{3} \quad \text{—— (3)}$$

put (3) in (2)

$$V_2 = \frac{2}{3}\left[-V_1 + 3I_2 - V_2\right]$$

$$V_2 = -\frac{2}{3}V_1 + 2I_2 - \frac{2}{3}V_2$$

$$\frac{5}{3}V_2 = -\frac{2}{3}V_1 + 2I_2$$

$$5V_2 = -2V_1 + 6I_2$$

$$\boxed{V_2 = \frac{-2V_1 + 6I_2}{5}} \quad \text{—— (4)}$$

put I_x in ①

$$3V_1 = I_1 + I_2 - \left[\frac{-V_1 + 3I_2 - V_2}{3}\right]$$

$$3V_1 = I_1 + I_2 + \frac{V_1}{3} - I_2 + \frac{V_2}{3}$$

$$\frac{8}{3}V_1 = \frac{V_1}{3} + I_1$$

$$8V_1 = V_2 + 3I_1 \quad — ⑤$$

put V_2

$$8V_1 = \frac{-2V_1 + 6I_2}{5} + 3I_1$$

$$40V_1 = -2V_1 + 6I_2 + 15I_1$$

$$\boxed{V_1 = \frac{15}{42}I_1 + \frac{6}{42}I_2} \quad — ⑥$$

put ⑥ in ④

$$V_2 = -\frac{2\left[\frac{15}{42}I_1 + \frac{6}{42}I_2\right] + 6I_2}{5}$$

$$V_2 = -\frac{\frac{15}{21}I_1 - \frac{6}{21}I_2 + 6I_2}{5}$$

$$V_2 = \frac{-\frac{15}{21}I_1 + \frac{120}{21}I_2}{5}$$

$$V_2 = \frac{-3}{21}I_1 + \frac{24}{21}I_2 \Rightarrow \frac{-1}{7}I_1 + \frac{8}{7}I_2 \quad — ⑦$$

So using ⑦ and ⑧

$$[Z] = \begin{bmatrix} 5/14 & 2/14 \\ -1/7 & 8/7 \end{bmatrix} = \begin{bmatrix} 5/14 & 1/7 \\ -1/7 & 8/7 \end{bmatrix}$$

Q.1 (d) Consider the following subroutine program of an 8085 microprocessor, which is operating with a clock frequency of 2 MHz:

```
        MVI B, DATA_8 bit   → 7T
LOOP:   DCR B       N
        JNZ LOOP    N-1     10T | 7T
        RET         1       ↓True  False
```

Let "*N*" is the decimal equivalent of the DATA_8 bit stored in B register. By analyzing the above program, derive an expression for the overall time delay produced by the subroutine. Using the result obtained, determine the value of "*N*" required to produce the overall time delay of 70 μs.

[12 marks]

as Over all delay

$= 7T + N \times 4T + [(N-1)\,10T + 7T] + 10T$

$= (10+7)T + 4TN + 10NT - 10T + 7T$

$\Rightarrow 14T + 14TN$

$\Rightarrow (14+14N)T$

as $f_{clock} = 2MHz$

$T = \frac{1}{2}$ μsec

So Delay $= (14+14N)\frac{1}{2}$ μsec

$= (7+7N)$ μsec

$= 7(1+N)$ μsec

to produce the overall delay of 70μs the value of N.

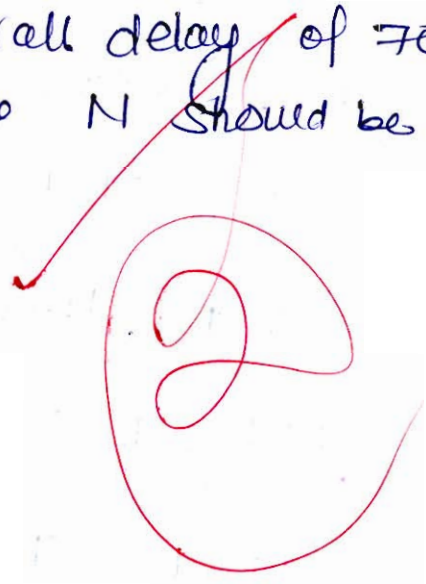
~~70 μsec = 7 (N+1) μsec~~

$N+1 = 10$

$\boxed{N = 9}$

to Reduce the overall delay of 70 μsec we required the N should be

(9)



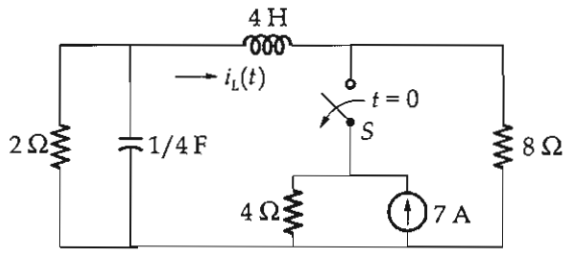
Q.1 (e) Differentiate between embedded and general purpose computing systems.

[12 marks]

Embedded System	General purpose system
It is one of the system which is consist of Hardware and software along with DMA.	It is consist of Hardware as well as software part. There is NO use of DMA in this system
It is very fast as compare to others.	Slow as compare to embedded system.
Direct memory transfer through DMA.	No direct memory transfer.
It is having very high speed.	very slow Response.
More complex system then the other	Less complex as the Number of component is less.
Cost of the embedded system is more compare to General purpose system	Relatively less cost as we are not using DMA controller.
Large Number of features are available in the embedded system.	Less Number of features are available in this system.

Can explain better.

Q.2 (a) In the circuit shown in the figure below, the switch S is closed for a long time and opened at $t = 0$. Find the time domain expression of the current $i_L(t)$ for $t > 0$.



[20 marks]

Q.2 (b) The reduced incidence matrix of a linear graph is given below:

$$A = \begin{array}{c} \begin{matrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 \end{matrix} \leftarrow \text{Branches} \\ \begin{bmatrix} 0 & 0 & 1 & 1 & 1 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 1 & 1 \\ -1 & 0 & -1 & 0 & 0 & -1 & 0 \end{bmatrix} \end{array}$$

The branches [2, 3, 4] constitute a tree.

(i) Without drawing the graph, determine the f-cutset matrix Q_C.

(ii) Determine the number of trees possible for the graph.

(iii) Draw the graph and verify the result for Q_C.

[20 marks]

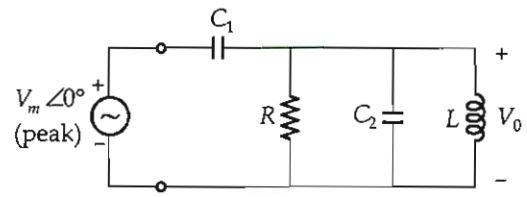
Q.2 (c) (i) Complete the following table by indicating the logic level (1 or 0) on each control or status pin of 8085 microprocessor for various machine cycles shown.

Machine Cycle	$\overline{RD}$	$\overline{WR}$	IO/$\overline{M}$	S_1	S_0
Memory read					
Memory write					
I/O read					
I/O write					
Opcode fetch					
Halt					

(ii) Draw the timing diagram of data flow when the 8085 instruction MOV C, A (machine code 4FH), stored in the memory location 2005H, is being fetched.

[8 + 12 marks]

Q.3 (a) Consider the circuit shown in the figure below:



(i) Derive an expression for the resonant frequency of the above circuit.

(ii) If $V_m = 10$ V, $R = 1$ kΩ, $C_1 = 2$ nF, $C_2 = 8$ nF and $L = 5$ mH, then determine the effective value of the voltage V_0 at resonant frequency by using the result obtained in part (i).

[25 marks]

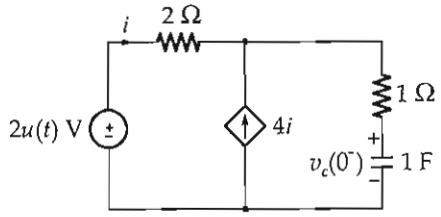
Q.3 (b) Assuming the microprocessor is completing an RST7.5 interrupt request, check to see if RST6.5 is pending. If it is pending, enable RST6.5 without affecting any other interrupt; otherwise, return to the main program.

[15 marks]

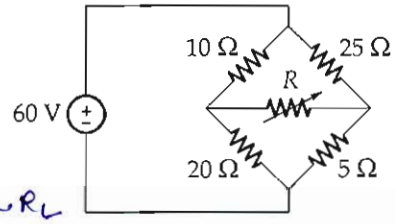
Q.3 (c) Write an 8085 assembly language program to arrange a data array in ascending order. The array is stored from the memory location 2501H and the length of the array is stored at 2500H. The resultant array should be stored from the memory location 2601H. Assume that the numbers in the data array are represented in unsigned 8-bit format.

[20 marks]

Q.4 (a) **(i)** In the circuit shown below, the initial voltage across the capacitor is $v_c(0^-) = 1$ V. Find the expression of the voltage $v_c(t)$ for $t > 0$.



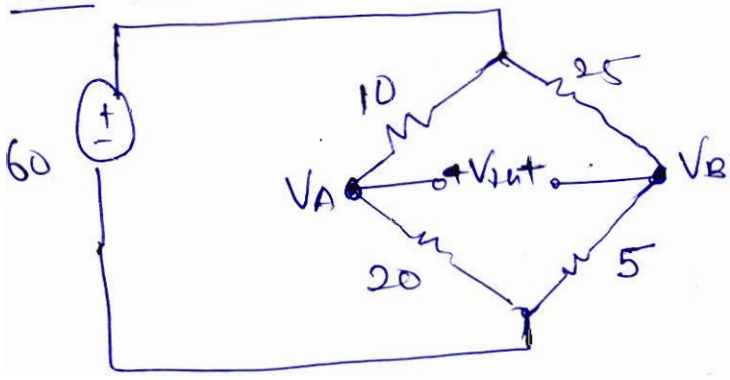
(ii) Determine the maximum power that can be delivered to the variable resistor R in the circuit shown below.



[13 + 12 marks]

(ii)

V_{th} :- Remove R_L

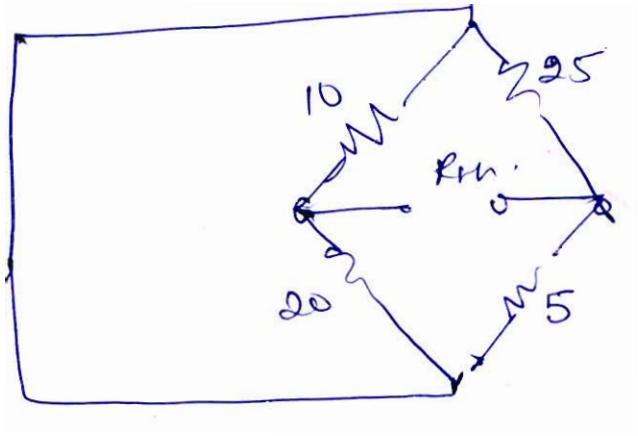


$V_A = \frac{60 \times 10}{30} \Rightarrow 20$ Volt

$V_B = \frac{25 \times 60^2}{30} \Rightarrow 50$ Volt

$V_{th} = 50 - 20$ $\quad V_{th} = 30V$

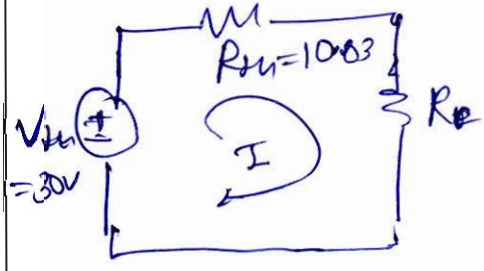
R_L :- to find R_{th}



$R_{Th} = 10 \| 20 + 25 \| 15$

$R_{Th} = 6.66 + 4.1666$

$\boxed{R_{Th} = 10.832\ \Omega}$

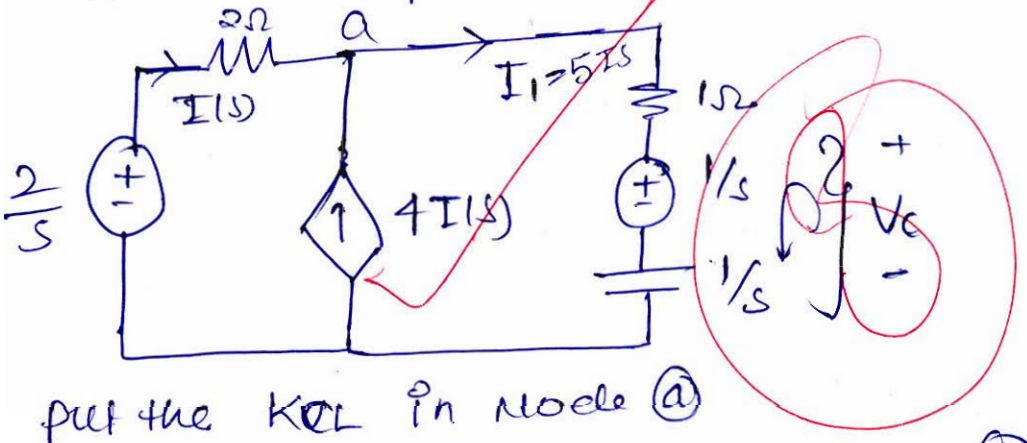


$\boxed{R_L = R_{Th} = 10.832\ \Omega}$

So power $= \dfrac{V_{Th}^2}{4R} = \dfrac{(30)^2}{4 \times 10.83} = 20.775\ W$

$\boxed{P_{max} = 20.775\ W}$

(i) Convert into Laplace domain



put the KCL in Node (a)

$I_1 = I(s) + 4I(s) = 5I(s)$ — (1)

KCL at Node (a)

$I(s) + 4I(s) = \dfrac{V_a - 1/s}{1 + 1/s}$

$5I(s) = \dfrac{V_a - 1/s}{\frac{s+1}{s}} = \dfrac{sV_a - 1}{s+1}$

$sV_a - 1 = 5I(s)(s+1)$

$$V_a = \frac{1}{s}\left[1 + 5I(s)(s+1)\right]$$

KVL at outloop

$$-\frac{2}{s} + 2I(s) + 5I(s) * 1/s + \frac{5I(s)}{s} = 0$$

$$I(s)\left[2 + 5 + \frac{5}{s}\right] = 1/s$$

$$I(s) = \frac{(1/s)}{(7 + 5/s)} \rightarrow \frac{1}{7s+5} \quad \text{— (2)}$$

KVL for V_c

$$-V_c + \frac{1}{s} + I(s) \cdot 1/s = 0$$

$$V_c(s) = \frac{1}{s} + \frac{1}{s} \cdot \frac{1}{7s+5}$$

$$V_c(s) = \frac{1}{s} + \frac{1}{s} \cdot \frac{1}{7(s+5/7)} = \frac{1}{s} + \frac{A}{s} + \frac{B}{(s+5/7)}$$

$$\frac{1}{7} = A(s+5/7) + Bs \qquad s = 0$$

$$\boxed{A = 5} \qquad s = -5/7$$

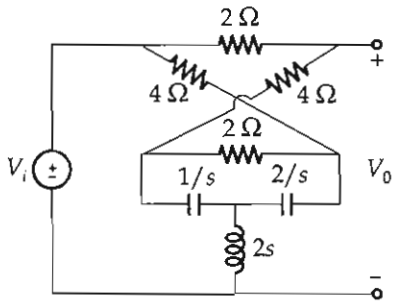
$$B = -5$$

$$V_c(s) = \frac{1}{s} + \frac{5}{s} - \frac{5}{s+5/7}$$ wrong cal

$$V_c(s) = \frac{6}{s} - \frac{5}{s+5/7}$$ take inverse transform.

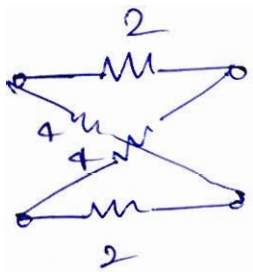
$$\boxed{V_c(t) = \left(6 - 5e^{-5/7\,t}\right)u(t) \quad \text{volt}}$$

Q.4 (b) For the network shown in the figure below, find the voltage gain V_0 / V_i.



[15 marks]

Solution



$$Z_1 = \begin{bmatrix} \frac{4+2}{2} & \frac{4-2}{2} \\ \frac{4-2}{2} & \frac{4+2}{2} \end{bmatrix}$$

$$Z_1 = \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix}$$

$$Z_2 = \begin{bmatrix} \frac{1}{s}+2s & 2s \\ 2s & 2s+\frac{2}{s} \end{bmatrix}$$

$$\text{So } Z_{eq} = Z_1 + Z_2 = \begin{bmatrix} 3 & 1 \\ 1 & 3 \end{bmatrix} + \begin{bmatrix} \frac{1}{s}+2s & 2s \\ 2s & 2s+\frac{2}{s} \end{bmatrix}$$

$$Z_{eq} = \begin{bmatrix} \frac{1}{s}+2s+3 & 2s+1 \\ 2s+1 & 2s+\frac{2}{s}+3 \end{bmatrix}$$

$$= \begin{bmatrix} \frac{2s^2+3s+1}{s} & 2s+1 \\ 2s+1 & \frac{2s^2+3s+2}{s} \end{bmatrix}$$

$2s^2+2s+s+1$

$2s(s+1)+1(s+1)$

$(2s+1)(s+1)$

$2s^2+2s+s+1$

$\frac{V_o}{V_i} = ?$

$V_o = Z_{21} I_1 + Z_{22} I_2$ $\quad I_2 = 0$

$\frac{V_o}{Z_{21}} = I_1$

$V_i = Z_{11} I_1 + Z_{12} I_2$ (0)

$V_i = Z_{11} \cdot \frac{V_o}{Z_{21}}$

$\frac{V_o}{V_i} = \frac{Z_{21}}{Z_{11}}$

put the value from Zeq

$\frac{V_o}{V_i} = \frac{2s+1}{\frac{2s^2+3s+1}{s}}$

$\frac{V_o}{V_i} = \frac{2s^2+s}{2s^2+3s+1}$

So voltage ccein

$$\boxed{\frac{V_o}{V_i} = \frac{s(2s+1)}{2s^2+3s+1}}$$

$\frac{V_o}{V_i} = \frac{s(2s+1)}{(2s+1)(s+1)}$

$$\boxed{\frac{V_o}{V_i} = \frac{s}{s+1}}$$

Q.4 (c) (i) Explain different addressing modes of 8086 microprocessor for sequential control flow instructions, with an example for each addressing mode.

(ii) Write a short note on the flag register of 8086 microprocessor. [12 + 8 marks]

Ans:- 8086 supports large Number of addressing mod.

① Immediate Type of addressing Mode →

In this type of addressing mode data is very immediate to addressing mode.

Example MOV AX, 0010H;

In this instruction the data 0010H will move to AX and store in that accumulator.

② Direct addressing mode →

In this type of addressing mode data is directly in the instruction part only.

Example → MOV AX [0010H];

In this instruction the memory content of [0010H] will be move to AX Register.

③ Register - Register addressing mode →

In this type of addressing mode the content of one register will be move to another Register.

Example MOV AX, BX;

2

In the above Instruction the content of BX Register will move to AX Register.

④ Register indirect addressing mode →

In this addressing mode the content of one Register memory location will be move to another Register.

Example. MOV AX [BX];

In this Instruction the data from memory location of BX will be move to Register AX.

⑤ Index addressing mode →

In this addressing mode the content of SI Index will be move to Register.

Example –: MOV AX, [SI]

⑥ Base Index addressing mode.

⑦ Register index addressing mode

(ii) Flag Register in 8086 –:

X	X	X	X	X	TF	IF	DF	S	Z	X	Ac	X	P	X	Cy

Various types of Flag present in 8086.

Sign Flag-: It is one type of Flag which is used to represent the sign magnitude of output if after operation 1 means Negative Number.

Parity Flag-: 8086 Follows even parity scheme. If the Number of '1' present in the output is even then it will be treated as '1' Others wise. zero.

Carry Flag-: It represents the carry after performing of operation. It Represent the carry at msB side.

Zero Flag-: When after operation. When the output is 0 then it will be as '1' Other wise it will be '0'.

Auxillary Flag-:

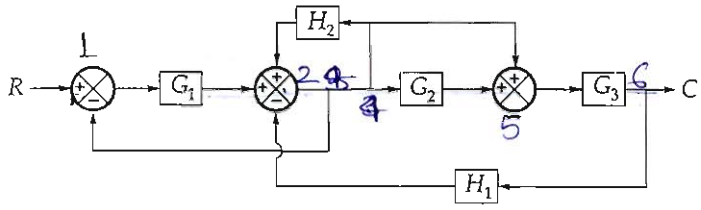
When the lower Nibble gets carry it will be represented by the Auxillary Carry Flag.

Trap Flag-: It is applicable when. maskable interrupt occurs.

need to explain more. direction flag, overflow flag, Interrupt flag ?

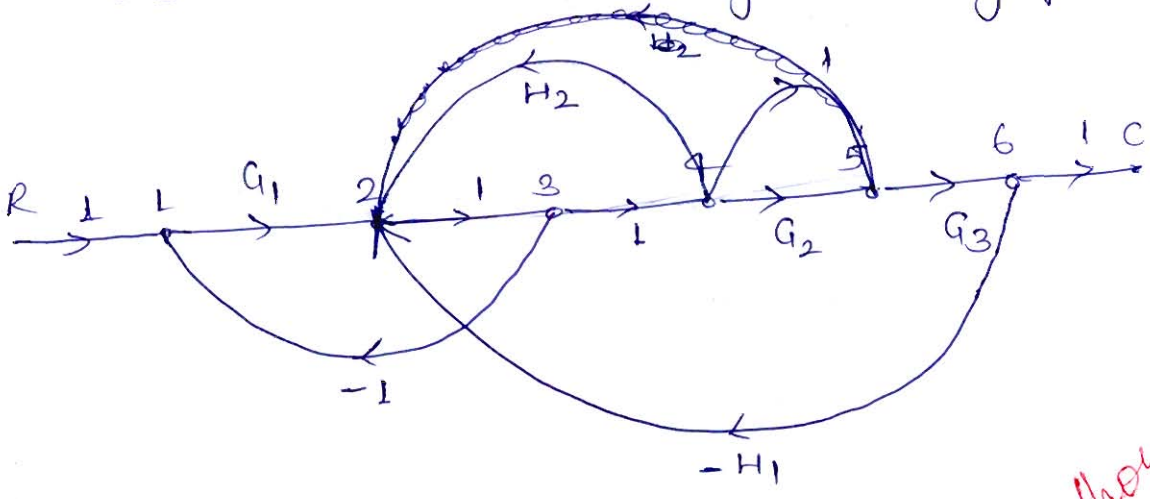
Section B : Digital Circuits-1 + Control Systems-1

Q.5 (a) Find transfer function for the block diagram shown in the figure below:



[12 marks]

Sol-: As we can convert into signal flow graph.



using Mason formula

$$TF = \frac{\sum P_K \Delta_K}{\Delta}$$

Forward path Gain $= G_1 G_2 G_3$, $G_1 G_3$

Individual Loops

$l_1 = -G_1$

$l_2 = H_2$

$l_3 = -G_3 H_1$

$l_4 = -G_2 H_1 G_3$

Should explained better

$$TF = \frac{G_1 G_2 G_3 + G_1 G_3}{1 - [G_1 + H_2 - G_3 H_1 - G_1 G_3 H_1]}$$

$$TF = \frac{G_1 G_3 [G_2 + 1]}{1 + G_1 - H_2 + G_3 H_1 + G_1 G_3 H_1}$$

Q.5 (b) The transfer function of a first order control system is $T(s) = \frac{K}{(s+a)}$. When a step input is applied, the system response reaches 50% of its steady state value in 5 sec. Find the time required by the same response to reach 90% of steady state value.

[12 marks]

Sol-:

$$\frac{C(s)}{R(s)} = \frac{K}{s+a} \qquad C(s) = \frac{K}{s(s+a)} = \frac{A}{s} + \frac{B}{s+a}$$

$$K = A(s+a) + Bs$$

$s = 0$

$$A = \frac{K}{a} \qquad s = -a \qquad B = -\frac{K}{a}$$

$$C(s) = \frac{\frac{K}{a}}{s} - \frac{\frac{K}{a}}{s+a}$$

Inverse Laplace Transform

$$C(t) = \frac{K}{a}\left[1 - e^{-at}\right] u(t) \quad \text{—①}$$

$$C(\infty) = \frac{K}{a}$$

$$0.5\frac{K}{a} = \frac{K}{a}\left[1 - e^{-a\times 5}\right]$$

$$\frac{1}{2} = 1 - e^{-a\times 5}$$

$$\frac{1}{2} = e^{-a\times 5}$$

$$e^{a5} = 2 \qquad 5a = \ln 2$$

$$\boxed{a = 0.138}$$

$$C(t) = \frac{K}{a}\left[1 - e^{-at}\right] \text{ to Reach 90\% of steady state value}$$

$$0.9\frac{K}{a} = \frac{K}{a}\left[1 - e^{-at}\right]$$

$$0.9 = 1 - e^{-at}$$

$$0.1 = e^{-at}$$

$$2.302 = at$$

$$t = \frac{2.302}{a}$$

$$t = \frac{2.302}{0.138}$$

$$\boxed{t = 16.68 \text{ sec}}$$

So to Reach 90% of steady state value we required 16.68 sec.

11

Q.5 (c) (i) Implement the following multiple output combinational logic circuit using 4-line to 16-line decoder.

$f_1 = \Sigma m(1, 2, 4, 7, 8, 11, 12, 13)$

$f_2 = \Sigma m(2, 3, 9, 11)$

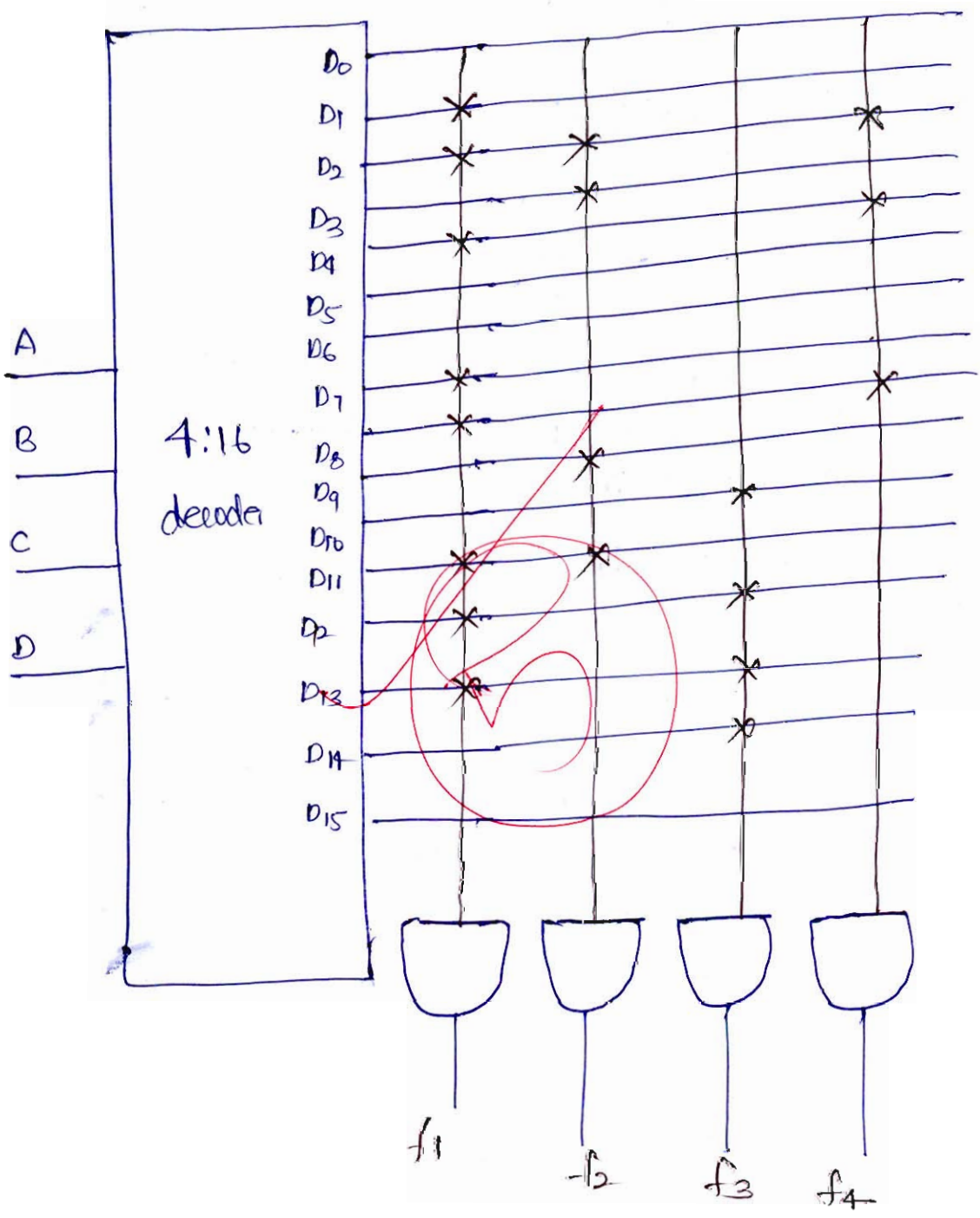
$f_3 = \Sigma m(10, 12, 13, 14)$

$f_4 = \Sigma m(2, 4, 8)$

(ii) Implement $f(A, B, C) = \Sigma m(0, 1, 4, 6, 7)$ using a 4×1 MUX by connecting A and B to its select lines.

[6 + 6 marks]

4:16 decoder



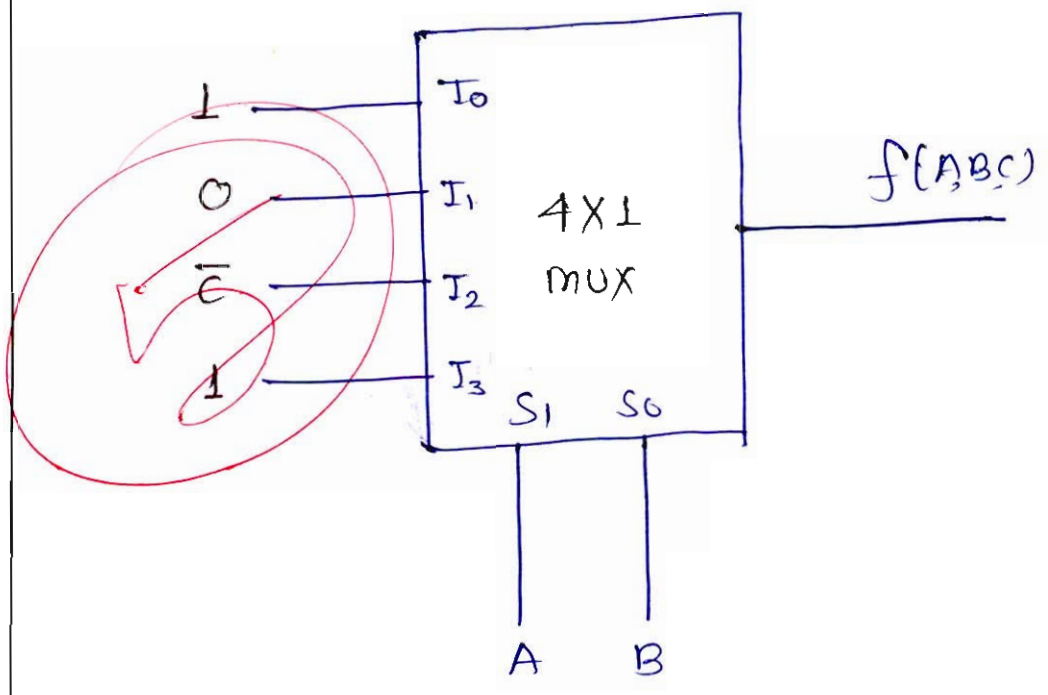
(ii) 4×1 MUX

Using Reduction procedure.

	$\bar{A}\bar{B}$ I_0	$\bar{A}B$ I_1	$A\bar{B}$ I_2	AB I_3
$\bar{C}$	$\bar{A}\bar{B}\bar{C}$	$\bar{A}B\bar{C}$	$A\bar{B}\bar{C}$	$AB\bar{C}$
C	$\bar{A}\bar{B}C$	$\bar{A}BC$	$A\bar{B}C$	ABC
	1	0	$\bar{C}$	1

So using 4×1 mux and A & B as the select line

Digital circuit diagram —:



Q.5 (d) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number using a 8 × 4 ROM circuit. **[12 marks]**

Truth Table

A	B	C	output b_0	b_1	b_2	b_3	b_4	b_5
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

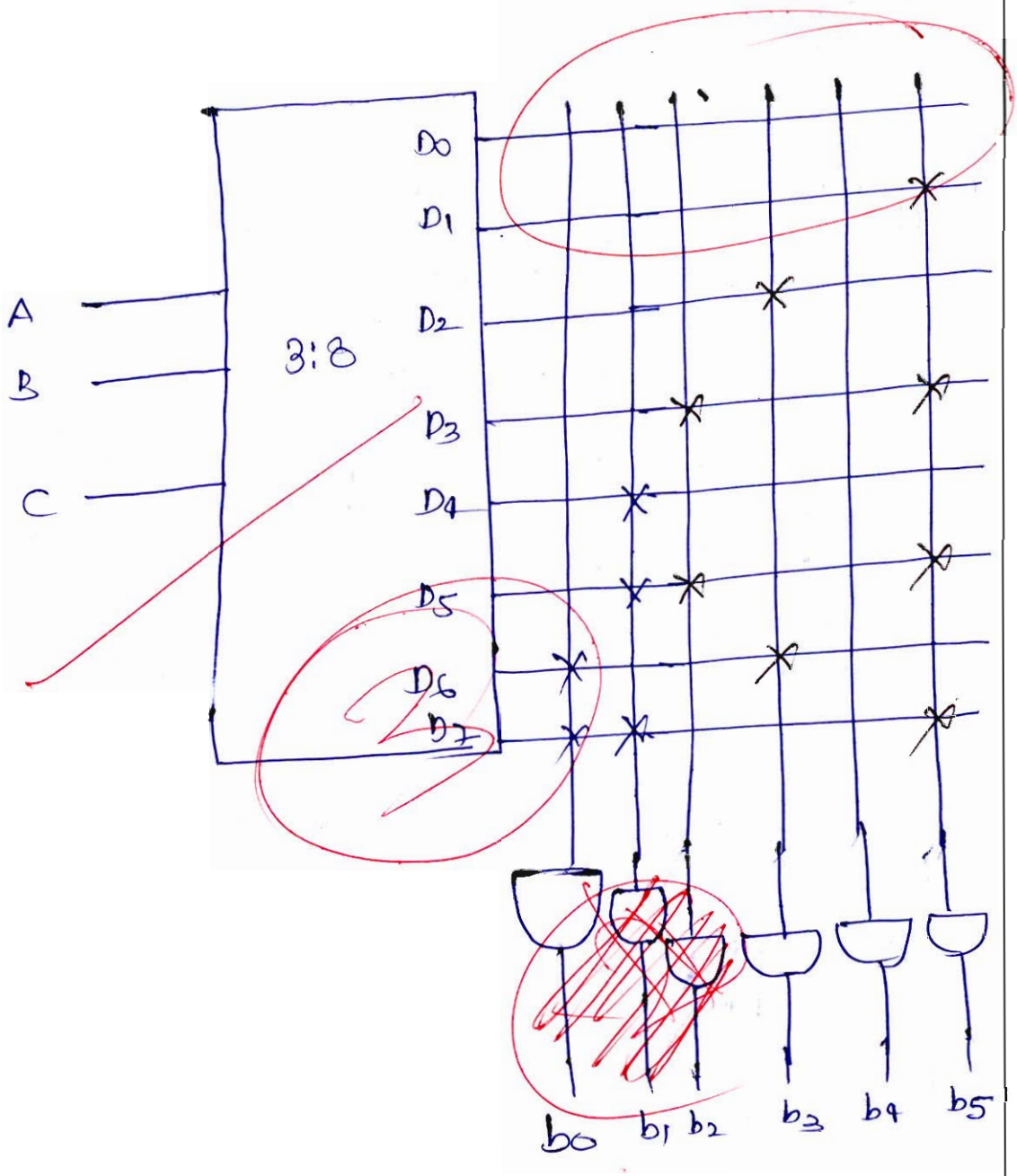
As the truth table of Binary number equal to the square of the input Number.

Using 8X4 ROM.

$2^3 \times 4$

$n = 3$

So we can use 3:8 decoder



Asked to design upto 8×4 ROM

Q.5 (e) Design CMOS logic circuits to implement the following expressions:

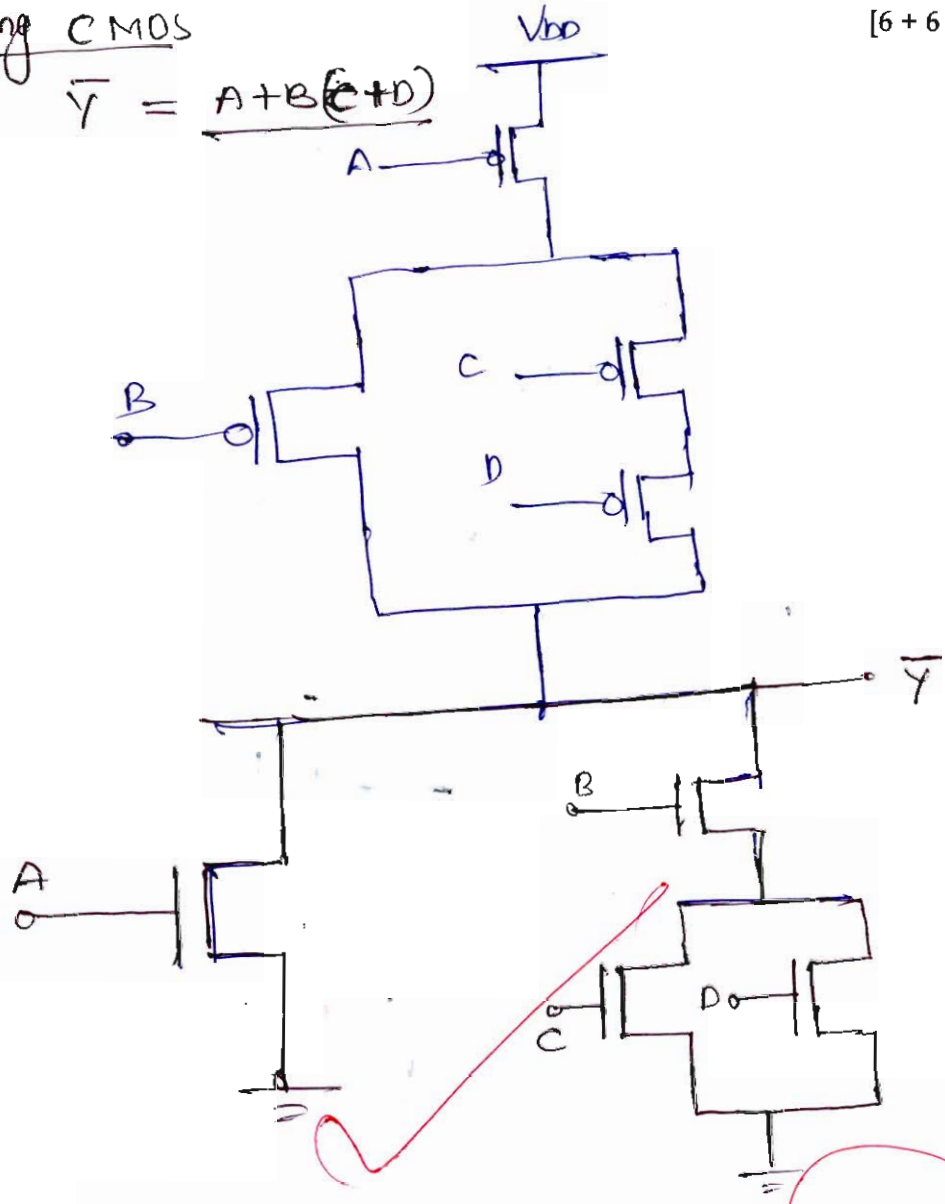
(i) $Y = \overline{A + B(C + D)}$

(ii) $Y = \overline{A} + \overline{B} + \overline{(C + D)}$

[6 + 6 marks]

Using CMOS

(i) $\overline{Y} = A + B(C + D)$



$\overline{A+B} = \overline{A} \cdot \overline{B}$

$\overline{A+B} = \overline{AB}$

(ii) $y = \overline{A} + \overline{B} + \overline{C+D}$

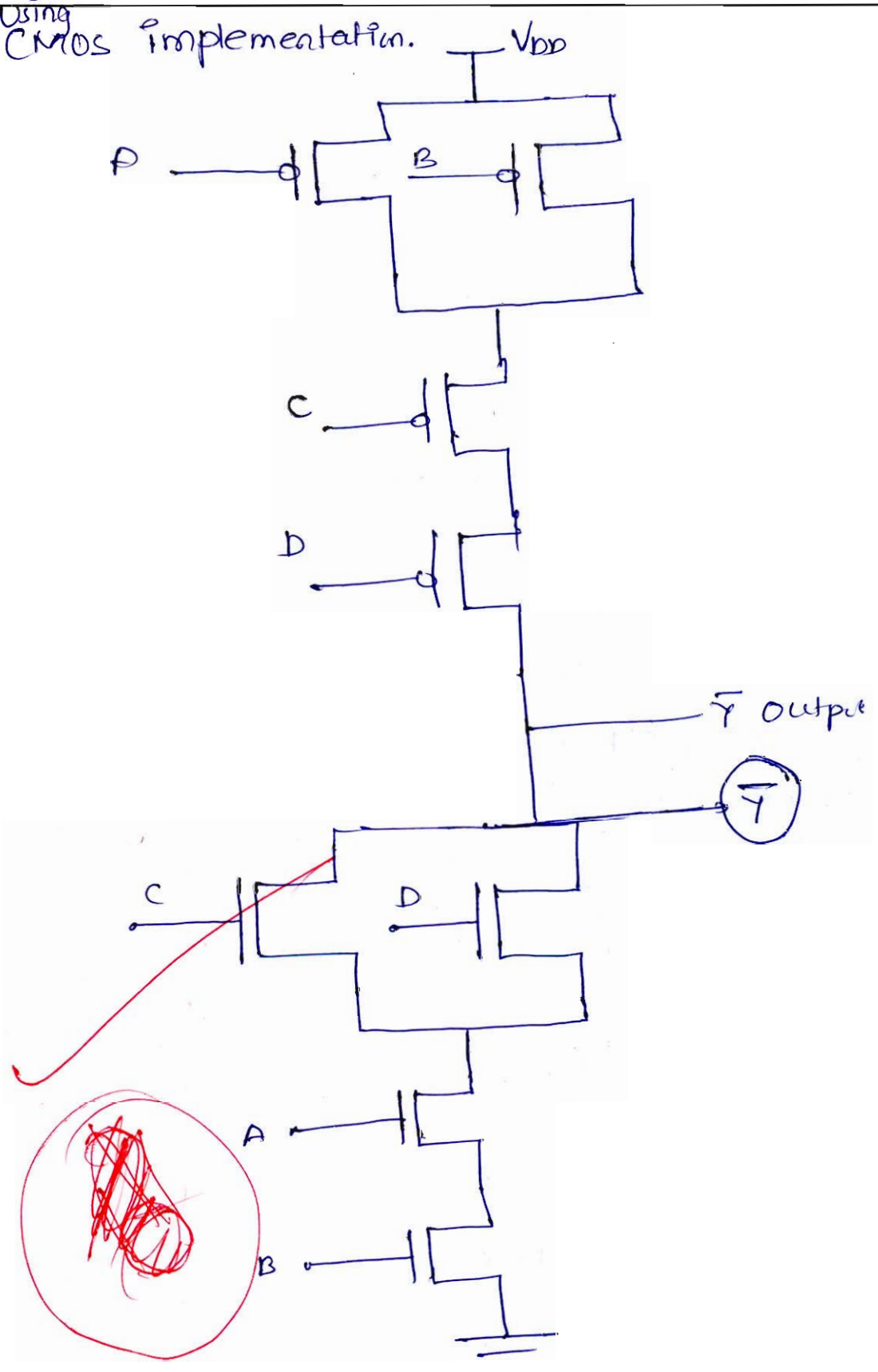
$y = \overline{A+B} + (\overline{C+D})$

$\overline{y} = \overline{\overline{AB} + (\overline{C+D})} = \overline{\overline{AB}} \cdot \overline{\overline{C+D}}$

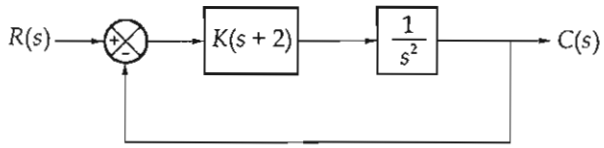
$= AB[C+D]$

$\overline{y} = AB(C+D)$

Using CMOS implementation.



Q.6 (a) **(i)** Consider the block diagram shown below:



Determine the value of K such that the phase margin of the system is 50°.

(ii) A negative feedback control system has open loop transfer function,

$$G(s)H(s)=\frac{K(s+2)}{s(s-1)}$$

Find the value of system gain K so that the damping ratio of the system is $\frac{1}{\sqrt{2}}$.

[12 + 8 marks]

Solution (ii)

From the char. equation

$$1+G(s)H(s)=0$$

$$s(s-1)+K(s+2)=0$$

$$s^2-s+Ks+2K=0$$

$$s^2+s(K-1)+2K=0$$

Compare with $s^2+2\xi\omega_n s+\omega_n^2=0$

$$\omega_n^2=2K$$

$$2\xi\omega_n=K-1$$

$$2\times\frac{1}{\sqrt{2}}\times\sqrt{2K}=(K-1)$$

$$\sqrt{2}\times\sqrt{2K}=(K-1)$$

Square on both side

$$4K=K^2+1-2K$$

$$K^2+1-6K=0$$

$$K^2-6K+1=0$$

$$K=5.828,\ 0.1716$$

So $\boxed{K=5.828,\ 0.171}$

So Gain value $K = 5.828$ and 0.171

(ii) $G H(s) = \dfrac{K(s+2)}{s^2}$

Phase margin $= 50 = 180 + \angle G(j\omega)$

$$\angle G(j\omega) = -130$$

$$G(j\omega) = \frac{K\sqrt{\omega^2+2^2}}{j^2\omega^2} \angle -180^\circ + \tan^{-1}\left(\frac{\omega}{2}\right)$$

$$-180 + \tan^{-1}\left(\frac{\omega}{2}\right) = -130^\circ$$

$$\tan^{-1}\left(\frac{\omega}{2}\right) = 50^\circ$$

$$\frac{\omega}{2} = \tan 50^\circ$$

$$\omega = 2 \times \tan 50^\circ$$

$$\omega = 2.382 \text{ rad/sec}$$

$$\left|\frac{K\sqrt{\omega^2+4}}{\omega^2}\right| = 1 \qquad \omega = 2.382$$

10

$$K = \frac{\omega^2}{\sqrt{\omega^2+4}} = \frac{(2.382)^2}{\sqrt{(2.382)^2+4}} = \frac{5.679}{3.114}$$

$$K = 1.822$$

So $\boxed{K = 1.822}$

we will get phase margin of 50°

Q.6 (b) In a power plant, three digital signals: drum level (D), water flow (W) and steam temperature (S) are used to control a particular system by a feedback signal (F) that comes from the field to the control room.

(i) Find the minimised logic expression that generates a high feedback signal (F) whenever any one of the conditions is satisfied.

C_1 : All the levels are at zero.

C_2 : Level D and S set to zero.

C_3 : Level W and S set to zero.

C_4 : Level D set to zero.

C_5 : All the levels are high.

(ii) Draw the logic circuit using the expression obtained in part (i) that generates a high feedback (F), using only two-input NAND gates.

[15 + 5 marks]

Sol-i

→ from the Given Condition →

$C_1 \rightarrow \bar{D}\,\bar{W}\,\bar{S} \rightarrow 0$

$C_2 \rightarrow \bar{D}\,W\,\bar{S} \rightarrow 2$

$C_3 \rightarrow D\,\bar{W}\,\bar{S} \rightarrow 4$

$C_4 \rightarrow \bar{D}\,W\,S \rightarrow 3$

$C_5 \rightarrow D\,W\,S \rightarrow 7$

Consider

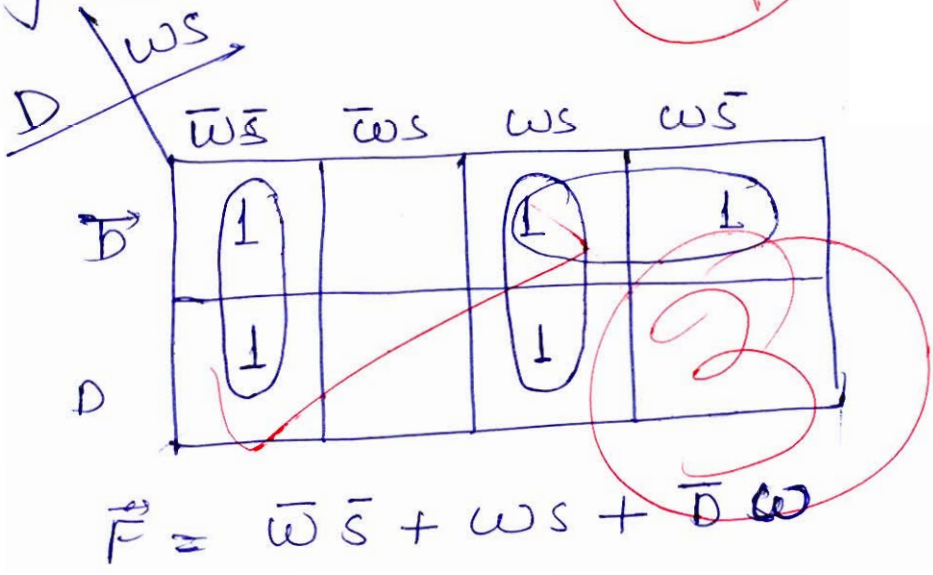
D → MSB

S → LSB

from the Given condition.

$F(D, W, S) = \sum m(0, 2, 3, 4, 7)$

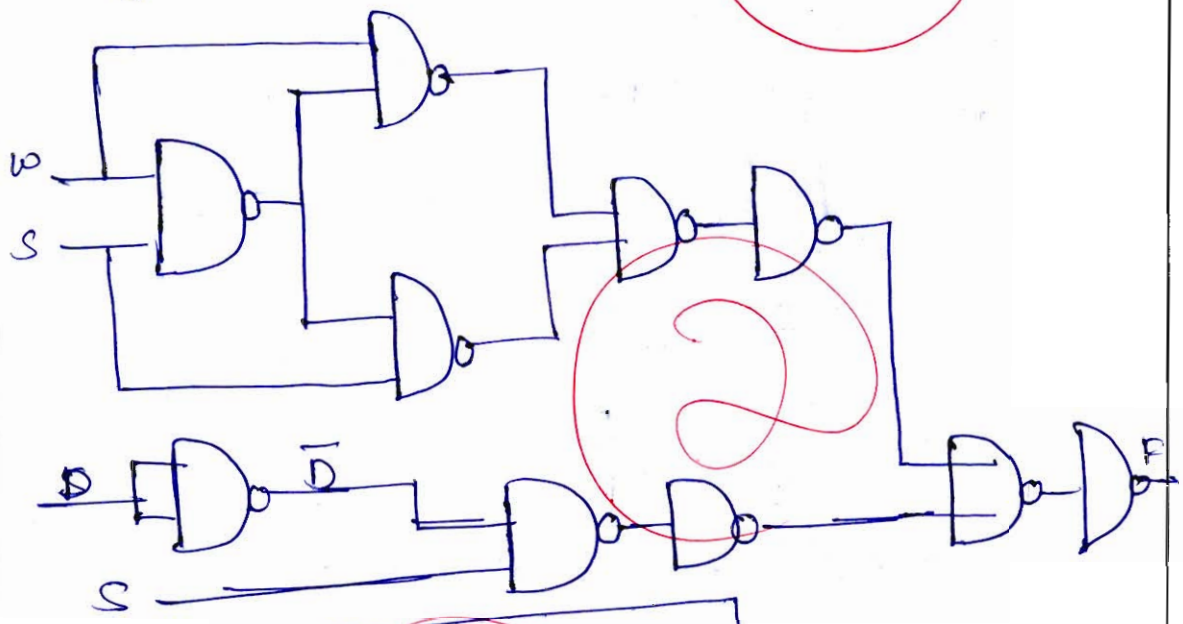
Using K-map Reduction.



$F = \bar{W}\bar{S} + WS + \bar{D}W$

$$F = \bar{W}\bar{S} + WS + \bar{D}S$$

Using NAND Gate



$$F = \bar{W}\bar{S} + WS + \bar{D}S$$

Q.6 (c) Using Nyquist criterion investigate the closed-loop stability of the system whose open-loop transfer function is,

$$G(s)\,H(s) = \frac{K(s+1)}{(s+0.5)(s-2)}$$

For **(i)** $K = 1.25$ and **(ii)** $K = 2.5$

(iii) Also determine the limiting value of K for stability.

[20 marks]

(iii) For limiting value of K we consider

$K = 1.25$

$$G(s)H(s) = \frac{1.25(s+1)}{(s+0.5)(s-2)}$$

$P = 2$

$$G(j\omega)H(j\omega) = \frac{1.25(j\omega+1)}{(j\omega+0.5)(j\omega-2)}$$

$$|G(j\omega)H(j\omega)| = \frac{1.25\sqrt{\omega^2+1}}{\sqrt{\omega^2+0.5^2}\sqrt{\omega^2+4}}$$

$$\angle G(j\omega)H(j\omega) = \tan^{-1}(\omega) - \tan^{-1}(2\omega) - \pi + \tan^{-1}\left(\frac{\omega}{2}\right)$$

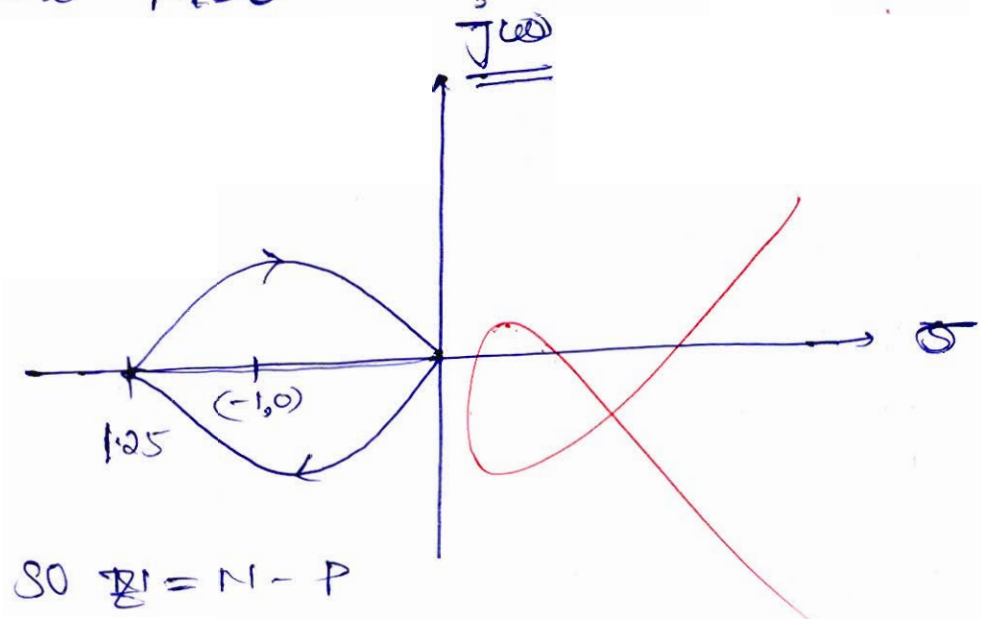
put $\omega = 0$

$M = \frac{1.25}{2 \times 0.5} = 1.25$

$\phi = -\pi$

$\omega = \infty \quad M = 0$

$\phi = -\pi/2$



So $Z = N - P$

So $P = 1$

$N = -1$

then $Z = -2$

So for K=1.25 system is Unstable

System.

(ii) For K=25

$$GH(j\omega) = \frac{2.5\sqrt{\omega^2+1}}{\sqrt{\omega^2+0.5}\sqrt{\omega^2+4}} \Big| \tan^{-1}(\omega) - \tan^{-1}2\omega - \pi + \tan^{-1}(\omega/2)$$

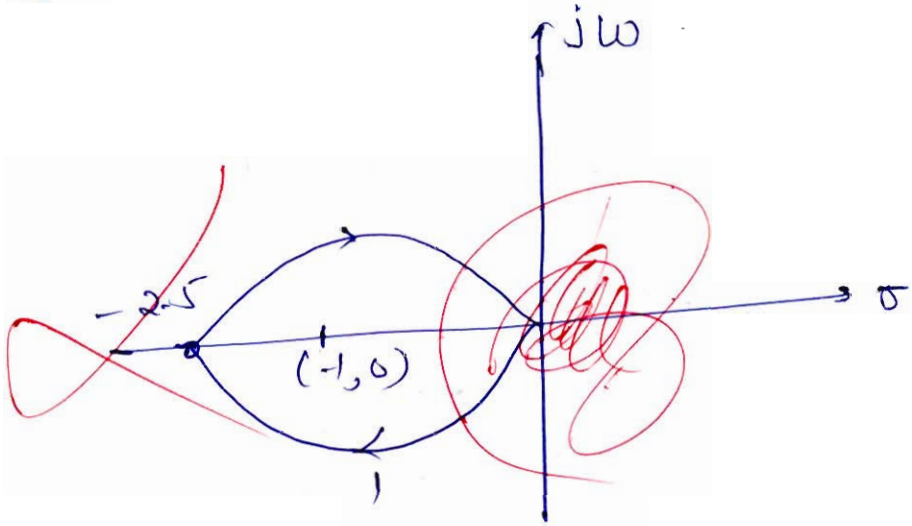
$\omega = 0$

$M = \infty$ $\quad \phi = -\pi$

$\omega = \infty$

$M = 0$ $\quad \phi = -\pi/2$

Using polar part followed by Nyquist plot



So $N = -1$ clockwise

$P = 1$

$Z = 0$

Stable for K=2.5

So Number of encirclement is equal to open loop pole lies on Right side of S-plane.

Stable system.

(iii) For limiting value of 'K'

$$1 + G(s)H(s) = 0$$

$$(s+0.5)(s-2) + K(s+1) = 0$$

$$s^2 - 2s + 0.5s - 1 + Ks + K = 0$$

$$s^2 - 1.5s + Ks + (K-1) = 0$$

$$s^2 - 1.5s + Ks + (K-1) = 0$$

$$s^2 + s(K-1.5)s + (K-1) = 0$$

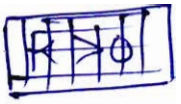
Using R-H Table

s^2	1	$K-1$
s^1	$(K-1.5)$	0
s^0	$(K-1)$	

So for stable $K > 1$

$K - 1.5 > 0$

$K > 1.5$



So if $K > 1.5$ then system is stable.

Q.7 (a) A unity feedback control system has an open loop transfer function,

$$G(s)=\frac{K\left(s+\frac{4}{3}\right)}{s^2(s+12)}$$

Sketch the complete root locus. Also, find the value of K for which all roots are equal, what is the value of these roots?

[20 marks]

Q.7 (b) A switching circuit has two control inputs (C_1 and C_2), two data inputs (X_1 and X_2) and one output (Z). The circuit performs one of the logic functions AND, OR, XOR, XNOR depending upon the control inputs. The output is equal to $X_1 + X_2$ for $C_1C_2 = 00$; $X_1 \oplus X_2$ for $C_1C_2 = 01$; X_1X_2 for $C_1C_2 = 10$; and $X_1 \odot X_2$ for $C_1C_2 = 11$. Find all the possible minimal expressions for logic function Z.

[20 marks]

Q.7 (c) Design combinational circuits for the following Boolean functions as instructed.

(i) Implement $F = \bar{A}\bar{B}\bar{D} + \bar{A}BD + ABC\bar{D} + A\bar{B}CD$ using 8 × 1 MUX and a NOT gate.

(ii) Implement $F = (A_0 \oplus A_2) + (A_1 \odot A_3)$ using only 2 × 1 MUX circuits and basic inputs A_0, A_1, A_2, A_3, 0 and 1.

[10 + 10 marks]

Q.8 (a) A control system with unity negative feedback has an open loop transfer function, $G(s) = \frac{K}{s(s+1)(0.1s+1)}$ and input, $r(t) = 10tu(t)$.

(i) Determine the steady state error (e_{ss}) for $K = 2$.

(ii) Find the minimum value of K for which, $e_{ss} \le 0.1$ for a unit ramp input.

(iii) For the value of K obtained in part (ii), obtain the closed loop transfer function of the system and thereby find the stability of system using *R-H* criteria.

[8 + 4 + 8 marks]

Solution (i) $G(s)H(s) = \frac{K}{s(s+1)(0.1s+1)}$ for Ramp input

$$K_v = \lim_{s\to 0} s \cdot G(s)H(s) = \lim_{s\to 0} \frac{K}{(s+1)(0.1s+1)} = K$$

$\boxed{K_v = 2}$

Input $r(t) = 10t\, u(t)$

$$e_{ss} = \frac{A}{K_v} = \frac{10}{2}$$

$\boxed{e_{ss} = 5}$

(ii) For Ramp input

$$K_v = \lim_{s\to 0} sG(s)H(s) = \lim_{s\to 0} \frac{K}{(s+1)(1\cdot s+1)} = K$$

$\boxed{e_{ss} = \frac{1}{K}}$

As Given $e_{ss} \le 0.1$

$$\frac{1}{K} \le 0.1$$

$1 \le 0.1K$ $\quad K \ge \frac{1}{0.1}$

$\boxed{K \ge 10}$ $\quad \boxed{K_{min} = 10}$

(iii) $G(s) = \dfrac{K}{s(s+1)(0.1s+1)}$

$K = 10$

$G(s) = \dfrac{10}{s(s+1)(0.1s+1)}$

$CLTF = \dfrac{G}{1+GH}$

$CLTF = \dfrac{\dfrac{10}{s(s+1)(0.1s+1)}}{1 + \dfrac{10}{s(s+1)(0.1s+1)}}$

$CLTF\ T(s) = \dfrac{10 \rightarrow K}{s(s+1)(0.1s+1) + 10 \leftarrow K}$

$T(s) = \dfrac{10}{(s^2+s)(0.1s+1)+10}$

$= \dfrac{10}{0.1s^3+s^2+0.1s^2+s+10}$

$$\boxed{T(s) = \frac{10}{0.1s^3+1.1s^2+s+10}}$$

For stability condition → Using RH method

$q(s) = 1 + GH(s) = 0$

$= 1 + \dfrac{10}{s(s+1)(0.1s+1)} = 0$

$q(s) = s(s+1)(0.1s+1) + 10 = 0$

$q(s) = (s^2+s)(0.1s+1) + 10 = 0$

$q(s) = 0.1s^3 + s^2 + 0.1s^2 + s + 10 = 0$

$q(s) = 0.1s^3 + 1.1s^2 + 1s + 10 = 0$

Using R-H method.

s^3	0.1	1
s^2	1.1	10
s^1	$\frac{1.1 - 1}{1.1} = \frac{0.1}{1.1} = 1/11$	
s	10	

So first column in the matrix is positive and having a same sign. so this system is stable. System.

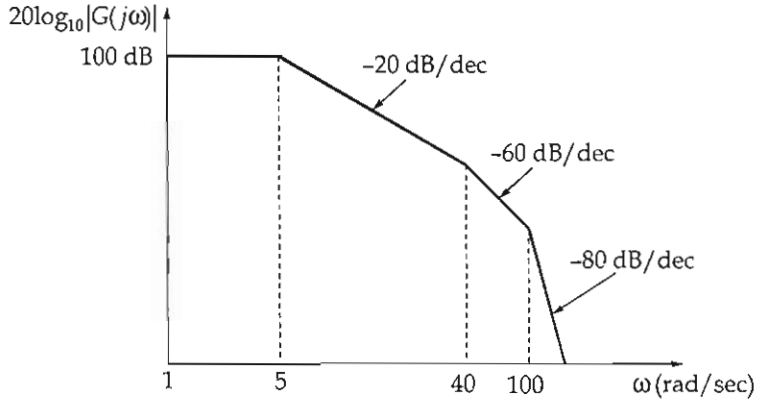
(F)

Q.8 (b) Define the terms: Minimum-phase system, Non-minimum phase system and all-pass system.

The magnitude plot of the open loop transfer function $G(s)$ of a certain system is shown in the figure below:

(i) Determine $G(s)$ if it is known that the system is of Minimum phase type.

(ii) Estimate the phase of $G(j\omega)$ at each of the corner frequencies.



[20 marks]

Minimum Phase System →

The system is said to be minimum phase system if the all poles and zero lies left side of s-plane is called minimum phase system

Example - $G(H(S) = \frac{K(S+1)}{(S+2)(S+3)}$

Non minimum phase system →

The system is said to be Non minimum phase system if either pole or zeros lies Right half of s-plane is called Non minimum phase system.

Example $G(H(S) = \frac{K(S-1)}{(S+2)(S+3)}$ → Right side of s-plane.

All pass System :- A system is said to All pass system if it exists the conjugate pair of pole zero pattern.

Example $\boxed{TF = \dfrac{1 - SRC}{1 + SRC}}$

(i) G(s) ⇒ determine

From the Given Plot we can write.

$$G(s) = \frac{K.}{\left(\frac{s}{5}+1\right)\left(\frac{s}{40}+1\right)^2\left(\frac{s}{100}+1\right)^2}$$

to determin the value of K

$M = -20 \times 2 \times \log\omega + 20\log K$

$\omega = 1 \quad M = 100$

$100 = 20\log K$

$5 = \log K \quad \boxed{K = 10^5}$

put the value of 'K' in G(s) system

$$G(s) = \frac{10^5 . 5 \times 40^2 \times 100}{(s+5)(s+40)^2(s+100)}$$

$$\boxed{G(s) = \frac{8 \times 10^8}{(s+5)(s+40)^2(s+100)}}$$

(ii) Phase of $G(j\omega)$ put $s = j\omega$

$$\angle G(j\omega) = -\tan^{-1}\left[\frac{\omega}{5}\right] - 2\tan^{-1}\left[\frac{\omega}{40}\right] - \tan^{-1}\left[\frac{\omega}{100}\right]$$

corner frequency $\omega = 5$ rad/sec

$$\angle G(j\omega) = -\tan^{-1}(1) - 2\tan^{-1}\left(\frac{5}{40}\right) - \tan^{-1}\left[\frac{5}{100}\right]$$

$$\angle G(j\omega) = -62.11^\circ$$

$\omega = 40$ rad/sec

$$\angle G(j\omega) = -\tan^{-1}\left(\frac{40}{5}\right] - 2\tan^{-1}\left[\frac{40}{40}\right] - \tan^{-1}\left[\frac{40}{100}\right]$$

$$\angle G(j\omega) = -194.67^\circ$$

$\omega = 100$ rad/sec

$$\angle G(j\omega) = -\tan^{-1}\left(\frac{100}{5}\right) - 2\tan^{-1}\left[\frac{100}{40}\right] - \tan^{-1}(1)$$

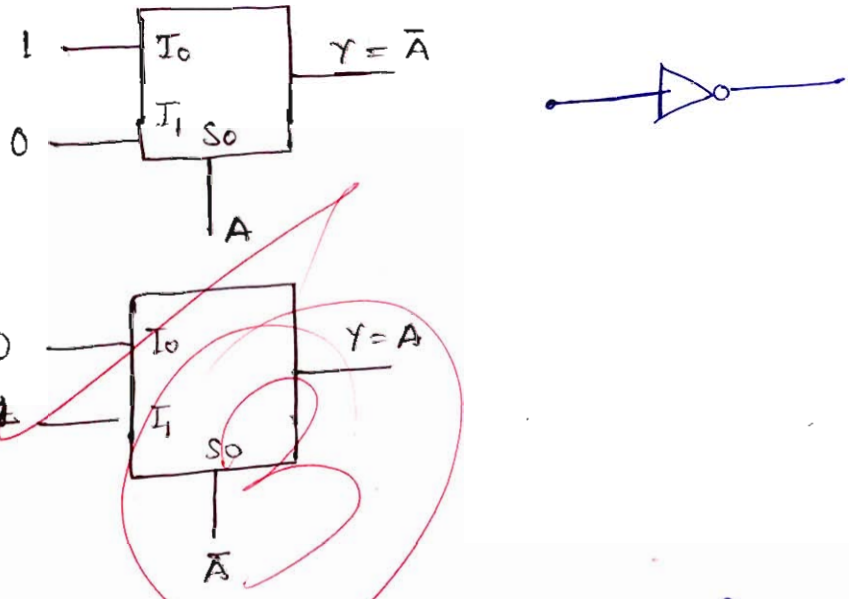
$$\angle G(j\omega) = -268.53^\circ$$

Q.8 (c) (i) What are the Hazards that occur while designing a combinational circuit? Discuss different types of Hazards.

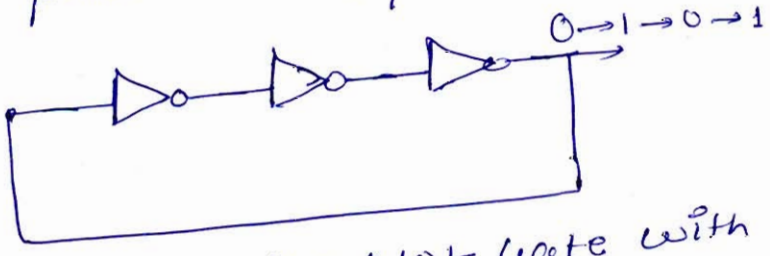
(ii) Design a square wave generator of output frequency (f_s) using a single 2 × 1 MUX circuit which suffers from a propagation delay of 10 ns. Also draw its output waveform and calculate the value of frequency (f_s).

[10 + 10 marks]

(ii) Square wave generator :-



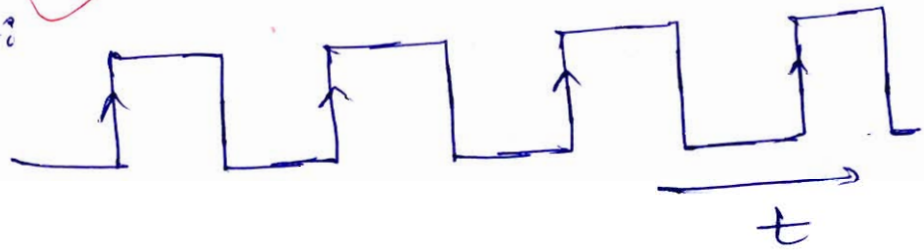
So as simple NOT Gate will be able to produce a square wave generator



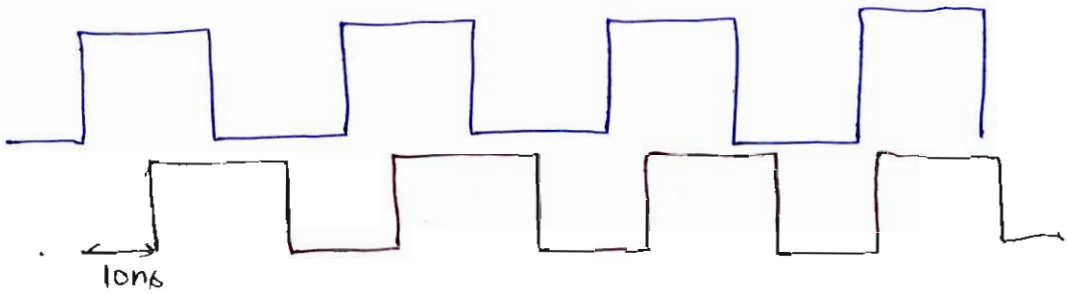
So we can replace the NOT Gate with 2x1 mux as shown in the above.

So we will be able to Generate the Square wave output

Output :-



So due to propagation delay = 10 nsec.



So Calculation of fs-:

$T_{squ} = 2 \times N \times t_{pd}$

$N = 1$

$T_{sq} = 2 \times 1 \times 10$

$T_{sq} = 20\,nsec$

So $f_s = \frac{1}{T_{sq}} = \frac{1}{20\,nsec} = 50\,MHz$

(i) Hazards—:

There are somany types of Hazards which are leads to unexcentented change in the output.

Some time we wanted to some type of Hazards to make the circuit simple.

There are various types of Hazards pres

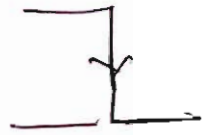
① Static - 0 type

② Static - 1 type

③ Dynamic type Hazards.

Static -0 types -: this type of Hazards basically present in combination circuit. mostly. it will be due to as we get long sequence of '0'.

Exp- AND - OR.



Static-1 types -:

It is one type of Hazards which Basically dominant in combinational circuit which leads to change the sudden output.

Example- OR - AND

Dynamic Hazards -:

It is one type of Hazards which is present in Sequential circuit, which leads to sudden spikes in the clocks signal or output signal. It is one of the Unwanted signal which may leads to damage the circuit also

Example

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Space for Rough Work

Space for Rough Work

Space for Rough Work

2	49
2	24 — 1
2	12 — 0
2	6 — 0
2	3 — 0
	1 — 1

110001

2	25
2	12 — 1
2	6 — 0
2	3 — 0
	1 — 1

11001

2	36
2	18 — 0
2	9 — 0
2	4 — 1
2	2 — 0
	1 — 0

100100