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Detailed Solutions

ESE-2026 Mains Test Series

E & T Engineering Test No : 2

Section A : Digital Circuits + Microprocessors & Microcontroller

Q.1 (a) Solution:

(i) For the given 8 × 1 MUX,

$S_2 = a$, $S_1 = b$, $S_0 = c$ are select lines and output is Z.

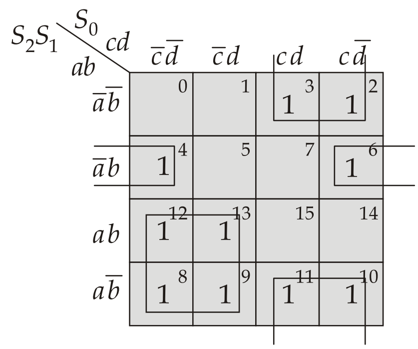
Truth table:

S_2 (a)	S_1 (b)	S_0 (c)	(d)	Z
0	0	0	0	$I_0 = 0$
0	0	0	1	$I_0 = 0$
0	0	1	0	$I_1 = 1$
0	0	1	1	$I_1 = 1$
0	1	0	0	$I_2 = \bar{d} = 1$
0	1	0	1	$I_2 = \bar{d} = 0$
0	1	1	0	$I_3 = \bar{d} = 1$
0	1	1	1	$I_3 = \bar{d} = 0$
1	0	0	0	$I_4 = 1$
1	0	0	1	$I_4 = 1$
1	0	1	0	$I_5 = 1$
1	0	1	1	$I_5 = 1$
1	1	0	0	$I_6 = 1$
1	1	0	1	$I_6 = 1$
1	1	1	0	$I_7 = 0$
1	1	1	1	$I_7 = 0$

(ii) The minimized output logic expression,

$$Z = f(a, b, c, d)$$
$$= \Sigma m(2, 3, 4, 6, 8, 9, 10, 11, 12\ 13)$$

By using 4-variable K-map



$$Z = f(a, b, c, d) = \bar{b}\,c + a\,\bar{c} + \bar{a}\,b\,\bar{d}$$

Q.1 (b) Solution:

(i) Let the n-bit base-3 number is,

$(X_{n-1}\ X_{n-2}\ ......\ X_3\ X_2\ X_1X_0)_3$

The corresponding decimal equivalent is,

$$= 3^{n-1} \cdot X_{n-1} + 3^{n-2} \cdot X_{n-2} + ...+ 3^3 \cdot X_3 + 3^2 \cdot X_2 + 3^1 \cdot X_1 + 3^0 \cdot X_0$$

$$= (3^2)^{\frac{n-1}{2}} X_{n-1} + (3^2)^{\frac{(n-2)}{2}} X_{n-2} + ... + 3^2 \cdot 3X_3 + 3^2X_2 + 3X_1 + X_0$$

$$= \left(9^{\frac{n-1}{2}}\right) X_{n-1} + \left(9^{\frac{n-2}{2}}\right) X_{n-2} + ... + 9.3X_3 + 9X_2 + 3X_1 + X_0$$

$$= 9^{\frac{(n-2)}{2}}\left[3X_{n-1} + X_{n-2}\right] + ... + 9^1(3X_3 + X_2) + 9^0(3X_1 + X_0)$$

So, we take every two digits of base-3 number from LSB side and find their decimal equivalent then it will be the corresponding base-9 digit.

(ii) Given base-3 number,

$(211101222211122)_3$

$$= (2\ 11\ 10\ 12\ 22\ 21\ 11\ 22)_3$$

Based on the result obtained in part (i), the decimal equivalent of the given number can be obtained as,

$$= 9^7(3 \times 0 + 2) + 9^6(3 \times 1 + 1) + 9^5(3 \times 1 + 0) + 9^4(3 \times 1 + 2) + 9^3(3 \times 2 + 2) + 9^2(3 \times 2 + 1) + 9^1(3 \times 1 + 1) + 9^0(3 \times 2 + 2)$$

$$= 9^7(2) + 9^6(4) + 9^5(3) + 9^4(5) + 9^3(8) + 9^2(7) + 9^1(4) + 9^0(8)$$

$\therefore$ base-9 equivalent is $(2\,4\,3\,5\,8\,7\,4\,8)_9$

Q.1 (c) Solution:

```
     MOV  CL, 00 H  ; Initialize CL register to 0 (used to store carry flag)
     MOV  SI, 0200 H ; Load source index register with memory address 0200 H
     MOV  AX, [SI]  ; Load first 16-bit number from memory location 0200 H into AX
     INC  SI        ; Increment SI to point to next memory location (0201 H)
     INC  SI        ; Increment SI to point to next memory location (0202 H)
     MOV  BX, [SI]  ; Load second 16-bit number from memory location 0202 H
                      into BX
     ADD  AX, BX    ; Add BX to AX
     JNC  L1        ; Jump to label L1 if no carry is generated
     INC  CL        ; If carry is generated, increment CL
L1;  MOV  DI, 0204 H ; Load destination index register with memory address 0204 H
     MOV  [DI], AX  ; Store the result (sum) at memory location 0204 H
     INC  DI        ; Increment DI to point to next memory location (0205 H)
     INC  DI        ; Increment DI to point to next memory location (0206 H)
     MOV  [DI], CL  ; Store carry flag (0 or 1) at memory location 0206 H
     HLT            ; Halt the program execution
```

Q.1 (d) Solution:

The 9's complement of a decimal digit d(0 to 9) is defined to be 9-d. Given, decimal digit (0-9) is stored at memory location 2050 H and assume result will be stored in 2051 H.

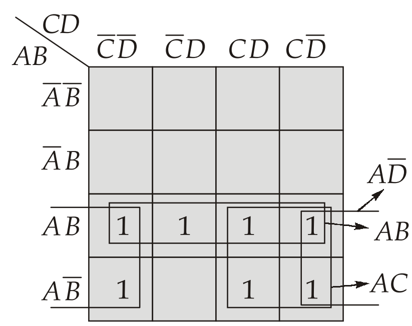
```
MVI  C, 09 H  ;  Load 09 H into register
LDA  2050 H   ;  Load decimal digit into Accumulator
MOV  B, A     ;  Store original digit in B
MOV  A, C     ;  Move 09 H into A
SUB  B        ;  A = 09 H – original digit to obtain 9's complement
STA  2051 H   ;  Store result
HLT           ;  Stop program
```

Q.1 (e) Solution:

(i) Given logic function,

$$F = ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C + AB$$

By using 4-variable K-map,



We get the simplified expression as,

$$F = AB + A\bar{D} + AC \quad \Rightarrow \quad \text{SOP form}$$

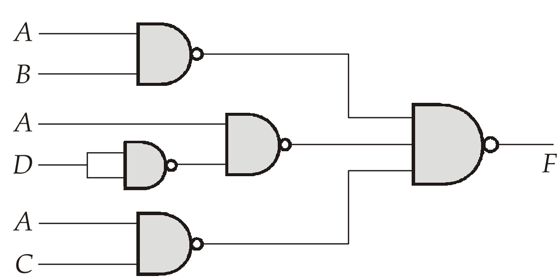
$\therefore$
$$F = A\left[B + C + \bar{D}\right] \quad \Rightarrow \quad \text{POS form}$$

(ii) Realizing the logic function using only NAND gates

$$F = AB + A\bar{D} + AC$$

$$\bar{\bar{F}} = \overline{\overline{AB + A\bar{D} + AC}}$$

$$F = \overline{\overline{AB} \cdot \overline{A\bar{D}} \cdot \overline{AC}}$$

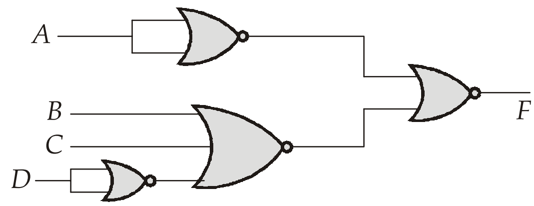


(iii) Realization the logic function using only NOR gates:

$$F = A(B + C + \bar{D})$$

$$\bar{\bar{F}} = \overline{\overline{A(B + C + \bar{D})}}$$

$$F = \overline{\bar{A} + \overline{(B + C + \bar{D})}}$$



Q.2 (a) Solution:

Given,

Generation of 100 kHz square wave (70% duty cycle) using 8051 Timer-1, Mode-2 with 12 MHz crystal.

∴ The time period of square wave,

$$T = \frac{1}{f}$$

$$= \frac{1}{100\text{ kHz}}$$

$$T = 10\ \mu\text{sec}$$

For 70% duty cycle:

$$\text{High time} = 70\% \text{ of } 10\ \mu\text{sec} = 7\ \mu\text{sec}$$

$$\text{Low time} = 30\% \text{ of } 10\ \mu\text{sec} = 3\ \mu\text{sec}$$

Timer frequency of 8051 is $1/12^{th}$ of the frequency of the crystal oscillator,

$$= \frac{12\text{ MHz}}{12} = 1\text{ MHz}$$

∴ 1 timer count = 1 μsec

We are using Mode-2 (Timer mode) which is 8-bit auto reload mode.

i.e., Timer overflows at 256. The counter counts from the loaded value TH_1 to FF H.

∴ $$TH_1 = 256 - \text{delay counts}$$

For HIGH time (7 μsec)

$$TH_1 = 256 - 7 = 249 = \text{F9 H}$$

For LOW time (3 μsec)

$$TH_1 = 256 - 3 = 253 = \text{FD H}$$

The timers' mode is adjusted using TMOD register given below:

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				Timer 0			

To configure Timer 1 in Mode 2, we have M0 = 0 and M1 = 1, $C/\overline{T} = 0$ for operating as a timer and GATE = 0 . Thus, we load TMOD with 20 H.

The program toggles P2.0 HIGH for 7 μs and LOW for 3 μs, continuously generating a 100 kHz square wave with 70% duty cycle.

Assembly language program:

```
                ORG 0000H
                MOV TMOD, #20 H   ;  Timer 1 Mode 2 (8-bit auto reload)
LOOP       :    MOV TH1, #0F9H    ;  Load for 7 μs delay
                SET B P2.0        ;  Make P2.0 high
                ACALL   DELAY 1
                MOV TH1, #0FDH    ;  Load for 3 μs delay
                CLR P2.0          ;  Make P2.0 Low
                ACALL DELAY1
                SJMP LOOP
DELAY 1    :    SETB TR1          ;  Start Timer 1
AGAIN 1    :    JNB TF1, AGAIN1   ;  Wait for overflow
                CLR TR1           ;  Stop Timer
                CLR TF1           ;  Clear overflow flag
                RET
                END
```

Q.2 (b) Solution:

In the given logic circuit, for 4 × 2 priority encoder,

inputs are $D_3 = X$ (Highest priority)

$D_2 = Y$

$D_1 = Z$

$D_0 = 0$ (Lowesst priority)

outputs are, B_1 (MSB)

B_0 (LSB)

V (Valid)

In priority encoder, the highest priority input (logic 1) determines the output.

Truth table

$D_3 = X$	$D_2 = Y$	$D_1 = Z$	$D_0 = 0$	B_1	B_0	V
0	0	0	0	X	X	0
1	X	X	0	1	1	1
0	1	X	0	1	0	1
0	0	1	0	0	1	1
0	0	0	0	0	0	0

From the given logic diagram,

Selection lines to 4 × 1 MUX are,

$$S_1 = B_1 V$$
$$S_0 = B_0 V$$

Truth table:

X	Y	Z	B_1	B_0	V	$S_1 (B_1 \cdot V)$	$S_0 (B_0 \cdot V)$
1	X	X	1	1	1	1	1
0	1	X	1	0	1	1	0
0	0	1	0	1	1	0	1
0	0	0	0	0	0	0	0

Given MUX inputs, $I_0 = 1; I_1 = 0, I_2 = Z, I_3 = \overline{Z}$

MUX output, $F = \overline{S_1}\,\overline{S_0}\,I_0 + \overline{S_1}\,S_0\,I_1 + S_1\,\overline{S_0}\,I_2 + S_1\,S_0\,I_3$

For $S_1S_0 = 11 \Rightarrow I_3 = \overline{Z}$ is propagated to the output.

$\therefore$ $F = \overline{Z}$

For $S_1S_0 = 10 \Rightarrow I_2 = Z$ is propagated to the output.

$\therefore$ $F = Z$

For $S_1S_0 = 01 \Rightarrow I_1 = 0$ is propagated to the output.

$\therefore$ $F = 0$

For $S_1S_0 = 00 \Rightarrow I_0 = 1$ is propagated to the output.

$\therefore$ $F = 1$

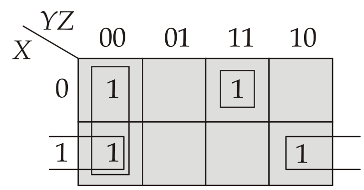
$\therefore$ The truth table for whole combinational logic is as follows:

X	Y	Z	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1

1	0	1	0
1	1	0	1
1	1	1	0

$\therefore$ Output, $F = \Sigma m(0, 3, 4, 6)$

By using 3-variable *k*-map,



$$\therefore \quad F = \overline{Y}\,\overline{Z} + \overline{X}YZ + X\overline{Z}$$

$$F = \overline{X}YZ + \overline{Z}(X + \overline{Y})$$

Q.2 (c) Solution:

The 8237 operates in two cycles, viz. idle or passive cycle and active cycle. Each cycle contains a fixed number of states. The 8237 can assume six states, when it is in active cycle. During idle cycle, it is in state SI (Idle State).

The 8237 is in the idle cycle if there is no pending request or the 8237 is waiting for a request from one of the DMA channels. Once a channel requests a DMA service, the 8237 sends the HOLD request to the CPU using the HRQ pin. If the CPU acknowledges the hold request on HLDA, the 8237 enters an active cycle. In the active cycle, the actual data transfer takes place in one of the following transfer modes, as is programmed.

Single Transfer Mode : In this mode, the device transfers only one byte per request. The word count is decremented and the address is decremented or incremented (depending on programming) after each such transfer. The Terminal Count (TC) state is reached, when the count becomes zero. For each transfer, the DREQ must be active until the DACK is activated, in order to get recognized. After TC, the bus will be relinquished for the CPU. For a new DREQ to 8237, it will again activate the HRQ signal to the CPU and the HLDA signal from the CPU will push the 8237 again into the single transfer mode. This mode is also called as “cycle stealing”.

Block Transfer Mode : In this mode, the 8237 is activated by DREQ to continue the transfer until a TC is reached, i.e. a block of data is transferred. The transfer cycle may be terminated due to an external end-of-process $\overline{\text{EOP}}$ (either internal or external) which forces Terminal Count (TC). The DREQ needs to be activated only till the DACK signal is activated by the DMA controller. Auto-initialization may be programmed in this mode.

Demand Transfer Mode : In this mode, the device continues transfers until a TC is reached or an external $\overline{\text{EOP}}$ is detected or the DREQ signal goes inactive. Thus a transfer may exhaust the capacity of data transfer of an I/O device. After the I/O device is able to catch up, the service may be re-established activating the DREQ signal again. Only the EOP generated by TC or external EOP can cause the auto-initialization, and only if it is programmed for.

Cascade Mode : In this mode, more than one 8237 can be connected together to provide more than four DMA channels. The HRQ and HLDA signals from additional 8237s are connected with DREQ and DACK pins of a channel of the host 8237 respectively. The priorities of the DMA requests may be preserved at each level. The first device is only used for prioritizing the additional devices (slave 8237s), and it does not generate any address or control signal of its own. The host 8237 responds to DREQ generated by slaves and generates the DACK and the HRQ signals to co-ordinate all the slaves. All other outputs of the host 8237 are disabled.

Memory to Memory Transfer Mode : To perform the transfer of a block of data from one set of memory address to another one, this transfer mode is used. Programming the corresponding mode bit in the command word, sets the channel 0 and 1 to operate as source and destination channels, respectively. The transfer is initialized by setting the $DREQ_0$ using software commands. The 8237 sends HRQ (Hold Request) signal to the CPU as usual and when the HLDA signal is activated by the CPU, the device starts operating in block transfer mode to read the data from memory. The channel 0 current address register acts as a source pointer. The byte read from the memory is stored in an internal temporary register of 8237. The channel 1 current address register acts as a destination pointer to write the data from the temporary register to the destination memory location. The pointers are automatically incremented or decremented, depending upon the programming. The channel 1 word count register is used as a counter and is decremented after each transfer. When it reaches zero, a TC is generated, causing $\overline{EOP}$ to terminate the service.

The 8237 also responds to external $\overline{EOP}$ signals to terminate the service. This feature may be used to scan a block of data for a byte. When a match is found the process may be terminated using the external $\overline{EOP}$.

Under all these transfer modes, the 8237 carries out three basic transfers namely, write transfer, read transfer and verify transfer. In write transfer, the 8237 reads from an I/O device and writes to memory under the control of $\overline{IOR}$ and $\overline{MEMW}$ signals. In read transfer, the 8237 reads from memory and writes to an I/O device by activating the $\overline{MEMR}$ and $\overline{IOW}$ signals. In verify transfer, the 8237 works in the same way as the read or write transfer but does not generate any control signal.

Q.3 (a) Solution:

(i) 1. From the given circuit,

Output of flip-flops,

$$F1 = X_1 = Q_1$$
$$F2 = X_2 = Q_2$$
$$F3 = X_3 = Q_3$$

$\therefore$ The input logic X is transferred to the output of the next stage flip-flop on the active edge of the clock pulse as

$$X \to X_1 \to X_2 \to X_3$$

$\therefore$ It is a shift register behaviour.

The output logic, $Z = Y \cdot X_3$

where, $Y = X_1 + X_2$

$\therefore$ $Z = (X_1 + X_2) \cdot X_3$

2.

Inputs			Output
X_3	X_2	X_1	$Z = (X_1 + X_2) \cdot X_3$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Since, output logic, $Z = 1$ only for certain 3-bit input patterns which are 011, 101 and 111.

$\therefore$ The functionality of the given circuit is 3-bit serial-in shift register with combinational detection logic.

(ii) For the given logic circuit,

inputs are: X, Y

output, $Q = A$

input of FF,

$$D = (X + Y) \oplus A$$
$$D = \overline{A}(X+Y) + A(\overline{X+Y})$$

∴ For D-FF, Next state, $A^+ = D$

∴ $$A^+ = \bar{A}(X+Y) + A(\overline{X+Y})$$

if $A = 1$ ⇒ $$A^+ = \bar{1}(X+Y) + 1\cdot(\overline{X+Y})$$

∴ $$A^+ = 0(X+Y) + (\overline{X+Y})$$

∴ $$A^+ = \overline{X+Y}$$

if $A = 0$ ⇒ $$A^+ = \bar{0}(X+Y) + 0\cdot(\overline{X+Y})$$

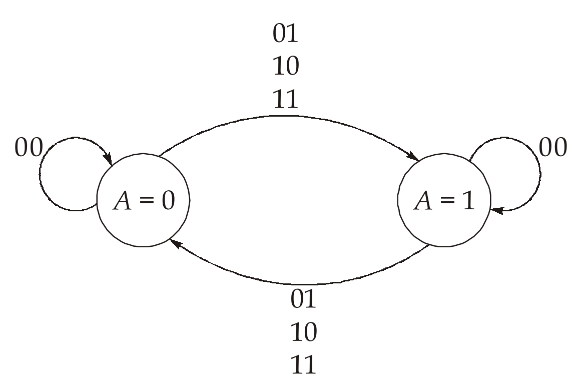
∴ $$A^+ = (X + Y)$$

State table of the given circuit;

Present state	**Inputs**		**Next state**
(*A*)	***X***	***Y***	**(A^+)**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

State diagram:

There are only two states, $A = 0$ and $A = 1$. State transition happens only when inputs XY are 01, 10, 11 and the state is not changed when input $XY = 00$.



Q.3 (b) Solution:

```
        ORG 0000H
START :
        MOV P2, #00 H   ;   Clear Port 2
MAIN_LOOP :
        ; RED Light ON
        SETB P2.0  ;   Turn ON RED LED
        CLR P2.1   ;   Turn OFF YELLOW LED
        CLR P2.2   ;   Turn OFF GREEN LED
        ACALL DELAY_5S; Wait 5 seconds
        ; GREEN Light ON
        CLR P2.0
        CLR P2.1
        SETB P2.2
        ACALL DELAY_5S; Wait 5 seconds
        ; YELLOW Light ON
        CLR P2.0
        SETB P2.1
        CLR P2.2
        ACALL DELAY_2S; Wait 2 seconds
        SJMP MAIN_LOOP; Repeat forever
        ; Delay Subroutines
        ; Delay ~5 seconds (Given (2 MHz clock))
DELAY_5S:
        MOV R7, #5; Repeat 1-sec delay 5 times
D5_Loop:
        ACALL DELAY_1S
        DJNZ R7, D5_Loop
        RET
        ; Delay ~2 seconds
```

```
DELAY_2S:
        MOV R7, #2
D2_Loop:
        ACALL DELAY_1S
        DJNZ R7, D2_Loop
        RET
        ; Delay ~1 second
DELAY_1S:
        MOV R6, #10
        D1_Loop 1:
        MOV R5, #200
        D1_Loop2:
        MOV R4, #250
        D1_Loop3:
        DJNZ R4, D1_Loop3
        DJNZ R5, D1_Loop2
        DJNZ R6, D1_Loop1
        RET
        END
```

Delay Calculation: For 8051, operating frequency is $(1/12)^{th}$ of the crystal frequency. At 12 MHz, one machine cycle takes

$$T = \frac{12}{\text{Clock frequency}} = \frac{12}{12\times10^6} = 1\ \mu\text{s}$$

Number of machine cycles required to generate delay of 1 sec is

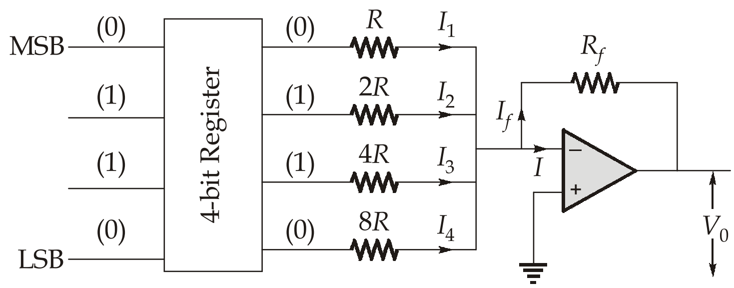
$$N = \frac{1}{1\times10^{-6}} = 1\times10^6$$

Each DJNZ instruction requires 2 machine cycles. Since the required number of cycles is 10^6, three registers are therefore used for, allowing the delay routine to accumulate the required number of machine cycles. Choosing the register counts as: $R6=10$, $R5=200$ and $R4=250$, we get the total delay generated as

$$250 \times 200 \times 10 \times 2\ \mu\text{s} = 1\ \text{sec}$$

Q.3 (c) Solution:

(i) Given, input code is 0110.



Using the concept of virtual short, $V^- = V^+ = 0$.

$$\therefore \quad I_1 = \frac{V_R}{R}(0) = 0 \text{ A}$$

$$I_2 = \frac{V_R}{2R}(1) = \frac{10}{2\times 1\text{ k}}(1) = 5 \text{ mA}$$

$$I_3 = \frac{V_R}{4R}(1) = \frac{10}{4\times 1\text{ k}}(1) = 2.5 \text{ mA}$$

$$I_4 = \frac{V_R}{8R}(0) = 0 \text{ A}$$

Output voltage, $V_0 = -I_f \times R_f$

where, $I_f = I_1 + I_2 + I_3 + I_4 = 7.5$ mA

$$\therefore \quad V_0 = -7.5 \times 10^{-3} \times 10^3$$

$$\therefore \quad V_0 = -7.5 \text{ V}$$

(ii) 1. In the given sequential circuit,

the input logic functions of each flip-flop is

$$D_1 = Q_3$$

$$D_2 = Q_1 \oplus X$$

$$D_3 = Q_2 \oplus Y$$

Since for the D-flip-flop, the next state is $Q^+ = D$.

$$\therefore \quad Q_1^+ = Q_3$$

$$Q_2^+ = Q_1 \oplus X$$

$$Q_3^+ = Q_2 \oplus Y$$

(a) For the given outputs $Q_1 = 0$; $Q_2 = 0$; $Q_3 = 0$ and inputs to XOR gate $X = 0$; $Y = 1$.

$$Q_1^+ = Q_3 = 0$$
$$Q_2^+ = Q_1 \oplus X = 0 \oplus 0 = 0$$
$$Q_3^+ = Q_2 \oplus Y = 0 \oplus 1 = 1$$

(b) For the given outputs $Q_1 = 1$; $Q_2 = 1$; $Q_3 = 0$, and inputs to XOR gate $X = 1$; $Y = 1$

$$Q_1^+ = Q_3 = 0$$
$$Q_2^+ = Q_1 \oplus X = 1 \oplus 1 = 0$$
$$Q_3^+ = Q_2 \oplus Y = 1 \oplus 1 = 0$$

(c) For the given outputs $Q_1 = 0$; $Q_2 = 0$; $Q_3 = 1$ and inputs to XOR gate $X = 1$; $Y = 0$

$$Q_1^+ = Q_3 = 1$$
$$Q_2^+ = Q_1 \oplus X = 0 \oplus 1 = 1$$
$$Q_3^+ = Q_2 \oplus Y = 0 \oplus 0 = 0$$

∴ The complete table is

Q_1	Q_2	Q_3	X	Y	Q_1^+	Q_2^+	Q_3^+
0	0	0	0	1	0	0	1
1	1	0	1	1	0	0	0
0	0	1	1	0	1	1	0

2. From the given timing diagram, just before the negative edge of clock before the dashed line, $X = 0$; $Y = 1$.

∴ For given, $Q_1Q_2Q_3 = 001$

the next state $Q_1^+Q_2^+Q_3^+$ is obtained as below:

$$Q_1^+ = Q_3 = 1$$
$$Q_2^+ = Q_1 \oplus X = 0 \oplus 0 = 0$$
$$Q_3^+ = Q_2 \oplus Y = 0 \oplus 1 = 1$$

∴ The next state is $Q_1^+ Q_2^+ Q_3^+ = 101$.

Q.4 (a) Solution:

(i) Let the inputs (Excess-3 code) are: E_3, E_2, E_1, E_0

Outputs (BCD-code) are: B_3, B_2, B_1, B_0

Truth table:

	Excess-3 input				BCD-output			
Decimal	E_3	E_2	E_1	E_0	B_3	B_2	B_1	B_0
0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	0
3	0	1	1	0	0	0	1	1
4	0	1	1	1	0	1	0	0
5	1	0	0	0	0	1	0	1
6	1	0	0	1	0	1	1	0
7	1	0	1	0	0	1	1	1
8	1	0	1	1	1	0	0	0
9	1	1	0	0	1	0	0	1

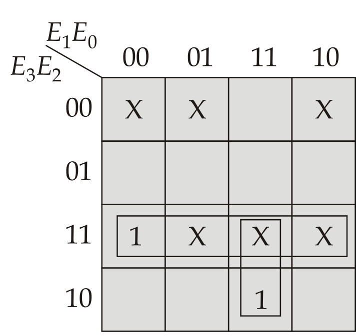
All other input combinations are don't care

i.e., (0000, 0001, 0010, 1101, 1110, 1111)

By using 4-variable K-map:

Output B_3:

$$B_3 = \Sigma m(11, 12)$$



$$\therefore \quad B_3 = E_3E_2 + E_3E_1E_0$$
$$= [(E_1\,E_0) + E_2]E_3$$

Output B_2:

$$B_2 = \Sigma m(7, 8, 9, 10)$$

E_3E_2 \ E_1E_0	00	01	11	10
00	X	X		X
01			1	
11		X	X	X
10	1	1		1

$$B_2 = \overline{E_2}\,\overline{E_1} + \overline{E_2}\,\overline{E_0} + E_2E_1E_0$$

$$= \overline{E_2}(\overline{E_1} + \overline{E_0}) + E_2(E_1E_0)$$

$$= \overline{E_2}(\overline{E_1} + \overline{E_0}) + E_2(\overline{\overline{E_1} + \overline{E_0}})$$

$$= E_2 \oplus (\overline{E_1} + \overline{E_0})$$

Output B_1:

$$B_1 = \Sigma m(5, 6, 9, 10)$$

E_3E_2 \ E_1E_0	00	01	11	10
00	X	X		X
01		1		1
11		X	X	X
10		1		1

$$B_1 = \overline{E_1}E_0 + E_1\overline{E_0} = E_1 \oplus E_0$$

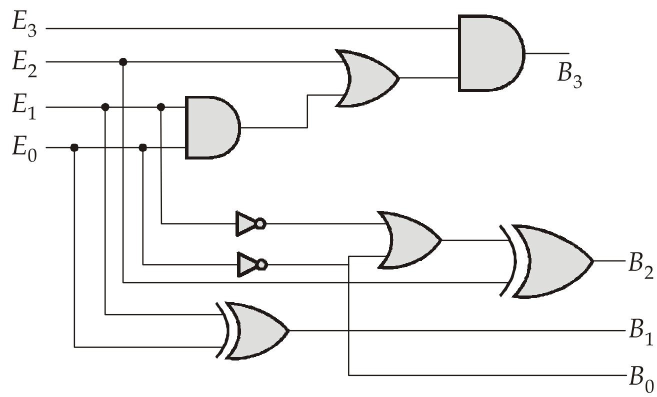
Output B_0:

$$B_0 = \Sigma m(4, 6, 8, 10, 12)$$

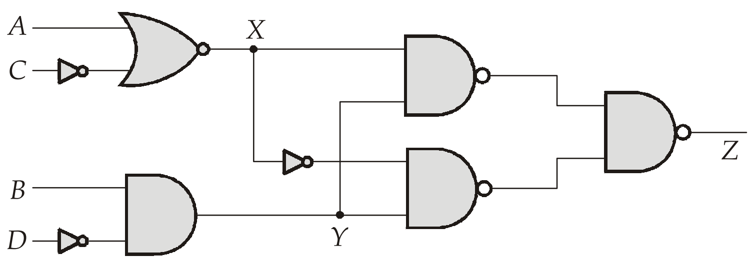
E_3E_2 \ E_1E_0	00	01	11	10
00	X	X		X
01	1			1
11	1	X	X	X
10	1			1

$$B_0 = \overline{E_0}$$

The logic diagram:



(ii)



Let X and Y be the outputs of intermediate circuit.

$$\therefore \quad X = \overline{A+\overline{C}} = \overline{A}\cdot C$$

$$Y = B\cdot\overline{D}$$

$$\text{output, } Z = \overline{\overline{XY}\cdot\overline{\overline{X}Y}}$$

$$= XY + \overline{\overline{\overline{X}Y}}$$

$$= XY + \overline{X}Y$$

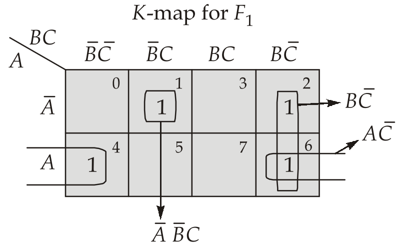
$$\therefore \quad Z = Y(X+\overline{X})$$

$$Z = Y = B\overline{D}$$

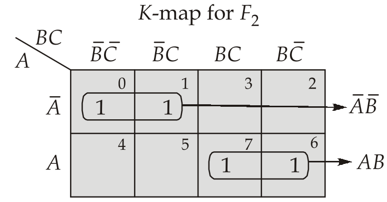
Q.4 (b) Solution

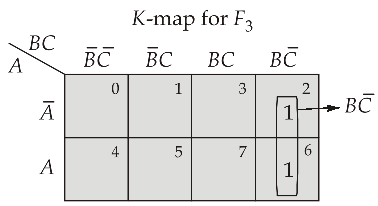
By minimizing the given functions using K-map, we get,

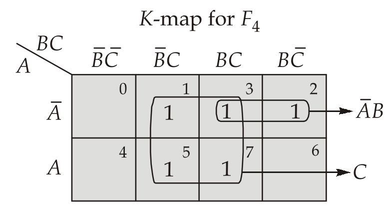
K-map for F_1



K-map for F_2







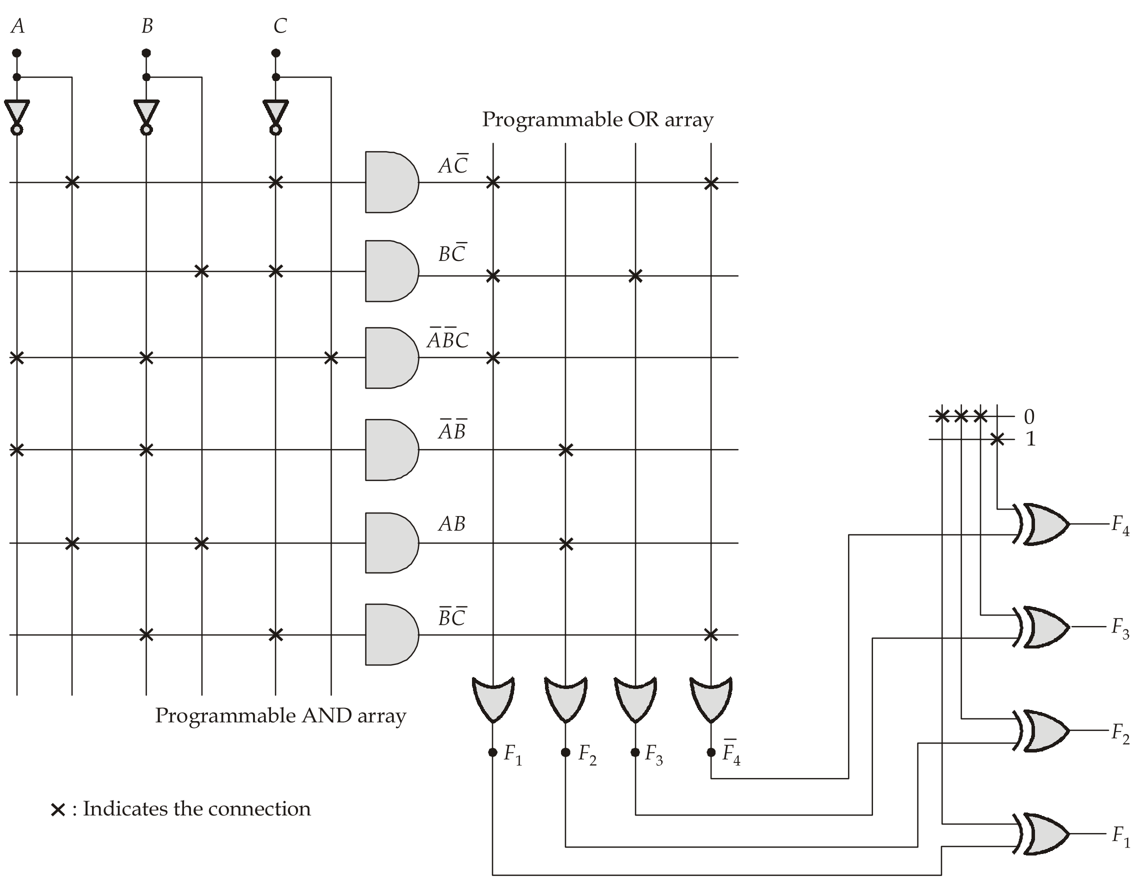
$$\left.\begin{aligned} F_1 &= A\bar{C} + B\bar{C} + \bar{A}\bar{B}C \\ F_2 &= \bar{A}\bar{B} + AB \\ F_3 &= B\bar{C} \\ F_4 &= C + \bar{A}B \end{aligned}\right\} \text{7 unique product terms} \Rightarrow$$

Design is not possible because, with the given (3 × 6 × 4) PLA IC, only 6 unique minterms are possible to form

$$\bar{F}_4 = (\overline{C + \bar{A}B}) = \bar{C}\cdot(\overline{\bar{A}B}) = \bar{C}\cdot(A + \bar{B}) = A\bar{C} + \bar{B}\bar{C}$$

$F_1, F_2, F_3, \bar{F}_4 \Rightarrow$ 6 unique product terms $\Rightarrow$ design is possible.

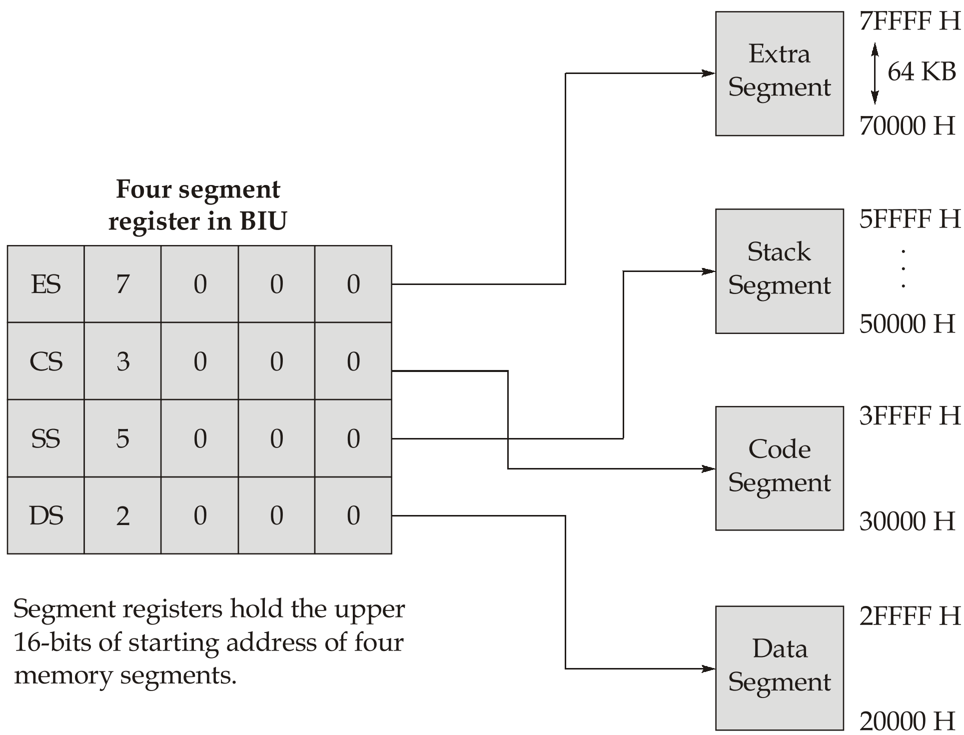
Implementation:



Q.4 (c) Solution:

(i) Segmentation is a process in which the main memory of the computer is logically divided into different segments and each segment has its base address. It is basically used to enhance the speed of execution of the computer system, so that the processor is able to fetch and execute the data from the memory easily and fast.

The Bus Interface Unit (BIU) contains four 16 bit special purpose registers (mentioned below) called as Segment Registers.



Code Segment Register : It is used for addressing memory location in the code segment of the memory where executable program is stored.

Data Segment Register : Points to the data segment of the memory where the data is stored.

Extra Segment Register : Also refers to a segment in the memory where the data is stored.

Stack Segment Register : It is used for addressing stack segment of the memory.

The number of address lines in 8086 is 20, 8086 BIU will send 20 bit address, so as to access one of the 1 MB memory locations. The four segment registers actually contain the upper 16-bits of the starting addresses of the four memory segments of 64 kB each.

In memory segmentation, each segment consists of two main components which are—

- **Segment Address** — It is a 16-bit address which points to the first location of the segment.
- **Offset Address** — It is also a 16-bit address which specifies the location within the memory segment, with respect to its starting address.

When the microprocessor accesses the memory, it combines the segment and offset addresses to calculate the physical address of the memory location. It is done by using the following formula:

$$\text{Physical Address} = (\text{Segment Address} * 10H) + \text{Offset Address}$$

8086 does not work the whole 1 MB memory at any given time. However it works only with four 64 kB segments within the whole 1 MB memory.

(ii) In 8051, there are six types of addressing modes :

1. Immediate addressing mode :

The data is provided in the instruction itself. The data is provided immediately after the opcode.

e.g. →
```
MOV A, #0AFH ;
MOV R3, #45H ;
MOV DPTR, #FF00H ;
```

In these instructions, the # symbol is used for immediate data.

2. Register addressing mode :

In the register addressing mode the source or destination data should be present in a register (R0 to R7).

e.g. →
```
MOV A, R5 ;
MOV R0, A ;
```

3. Direct addressing mode :

The source or destination address is specified by using 8-bit data in the instruction. Only the internal data memory can be used in this mode.

e.g. →
```
MOV 80H, R6 ;
MOV R2, 45H ;
MOV R0, 05H ;
```

4. Register indirect addressing mode :

The source or destination address is given in the register. By using register indirect addressing mode, the internal or external addresses can be accessed.

e.g. →
```
MOV 0E5H, @R0 ;
MOV @R1, 80H ;
```

In the instructions, the @ symbol is used for register indirect addressing. If the content of R0 is 40H, then that instruction will take the data which is located at location 40H of the internal RAM. In the second one, if the content of R1 is 30H, then it indicates that the content of port P0 will be stored at location 30H in the internal RAM.

5. **Indexed addressing mode :**
In Indexed addressing mode, the effective address is obtained by adding an 8-bit offset from the Accumulator (A) to a 16-bit base address held in the Data Pointer (DPTR) or Program Counter (PC),
e.g. → MOVC A, @A + PC ;
MOVC A, @A + DPTR ;
The C in MOVC instruction refers to code byte. For the first instruction, let us consider A holds 30H. And the PC value is 1125H. The contents of program memory location 1155H (30H + 1125H) are moved to register A.

6. **Implied addressing mode :**
In implied addressing mode, the operand is inherently defined within the opcode itself, rather than being explicitly stated. The instruction acts on specific registers (like the Accumulator or Carry flag) by default, requiring no operand address field.
e.g. → RLA ;
SWAP A ;

Section B : Network Theory-1 + Signals and Systems-1

Q.5 (a) Solution:

Applying Kirchhoff's voltage law, we get the time domain equation as

$$Ri(t) + L\frac{di(t)}{dt} = v(t)$$

Taking Laplace transform, we have

$$RI(s) + LsI(s) - Li(0^+) = V(s)$$

$$[R + Ls]I(s) = V(s) \qquad [\text{since } i(0^+) = i(0) = 0]$$

Substituting $R = 2\ \Omega$ and $L = 2$ H, we get

$$(2 + 2s)I(s) = V(s)$$

$$I(s) = \frac{V(s)}{2+2s} = \frac{V(s)}{2(s+1)}$$

The Laplace transform of the given triangular wave is obtained as,

$$v(t) = r(t) - 2r(t-1) + r(t-2)$$

$$\Rightarrow \qquad V(s) = \frac{1-2e^{-s}+e^{-2s}}{s^2}$$

Therefore,
$$I(s) = \frac{1-2e^{-s}+e^{-2s}}{2s^2(s+1)}$$

By partial fraction expansion,

$$F(s) = \frac{1}{s^2(s+1)} = \frac{A_0}{s^2}+\frac{A_1}{s}+\frac{A_2}{(s+1)}$$

where,
$$A_0 = F(s)s^2\Big|_{s=0} = \frac{1}{s+1}\Big|_{s=0} = 1$$

$$A_1 = \frac{d}{ds}\frac{1}{s+1}\Big|_{s=0} = -\frac{1}{(s+1)^2}\Big|_{s=0} = -1$$

$$A_2 = (s+1)F(s)\Big|_{s=-1} = \frac{1}{s^2}\Big|_{s=-1} = 1$$

Therefore,
$$\frac{1}{s^2(s+1)} = \frac{1}{s^2}-\frac{1}{s}+\frac{1}{(s+1)}$$

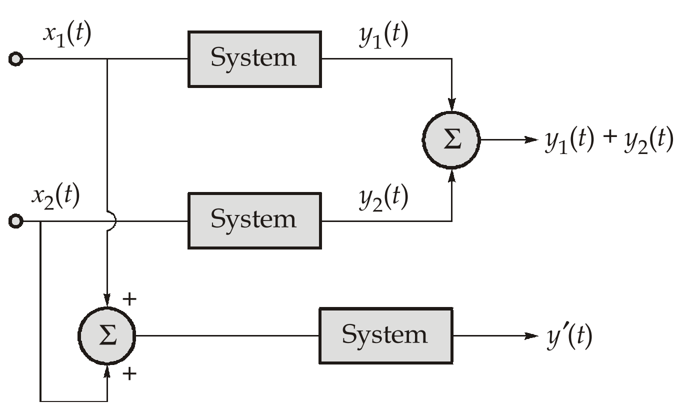
$$L^{-1}\left\{\frac{1}{s^2(s+1)}\right\} = t-1+e^{-t}$$

Therefore,
$$i(t) = L^{-1}[I(s)] = L^{-1}\left\{\frac{1-2e^{-s}+e^{-2s}}{2s^2(s+1)}\right\}$$

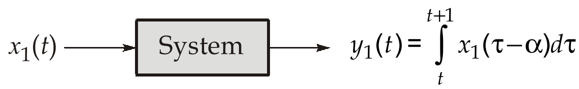
$$= \frac{1}{2}\left[t-1+e^{-t}\right][u(t)-2u(t-1)+u(t-2)]$$

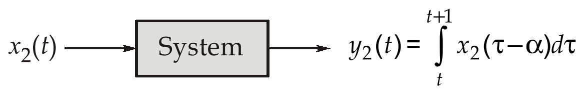
Q.5 (b) Solution:

(i) 1. Linearity :



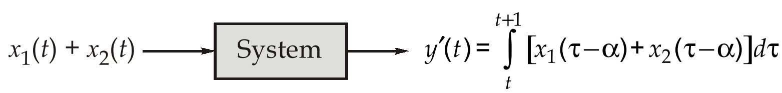
For a system to be linear, $y'(t) = y_1(t) + y_2(t)$





$$\therefore \quad y_1(t) + y_2(t) = \int_t^{t+1} [x_1(\tau-\alpha)+x_2(\tau-\alpha)]d\tau \quad ...(i)$$

and when



$$y'(t) = \int_t^{t+1} [x_1(\tau-\alpha)+x_2(\tau-\alpha)]d\tau \quad ...(ii)$$

From equation (i) and (ii),

$$y'(t) = y_1(t) + y_2(t)$$

$\therefore$ The system is linear,

2. Shift the input by t_0,

$$y_1(t) = \int_t^{t+1} x(\tau-\alpha-t_0)d\tau$$

Let, $\tau - t_0 = \lambda$

$d\tau = d\lambda$

$\therefore$ When $\tau = t$ then, $\lambda = t - t_0$

When $\tau = t + 1$ then $\lambda = t + 1 - t_0$

$$\therefore \quad y_1(t) = \int_{t-t_0}^{t+1-t_0} x(\lambda-\alpha)d\lambda \quad ...(i)$$

Shift in output by t_0,

$$y_2(t) = \int_{t-t_0}^{t-t_0+1} x(\tau-\alpha)d\tau \quad ...(ii)$$

as τ is a dummy variable we can replace it by any variable.

Let replace τ by λ.

$$\therefore \quad y_2(t) = \int_{t-t_0}^{t-t_0+1} x(\lambda - \alpha) d\lambda \quad \text{...(iii)}$$

From equation (i) and (iii),

$$y_1(t) = y_2(t)$$

The system is time invariant.

3. Now,
$$y(t) = \int_{t}^{t+1} x(\tau - \alpha) d\tau$$

Let, $\tau - \alpha = \lambda$

$\therefore$ $d\tau = d\lambda$

When $\tau = t$ then $\lambda = t - \alpha$

$\tau = t + 1$ then $\lambda = t + 1 - \alpha$

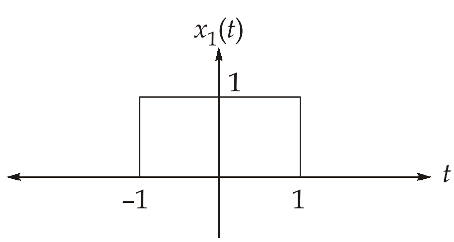
$$\therefore \quad y(t) = \int_{t-\alpha}^{t+1-\alpha} x(\lambda) d\lambda$$

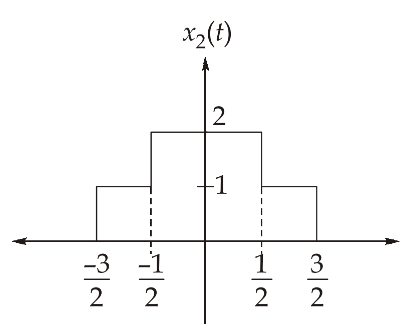
So, the present output depends upon future input when $\alpha \le 0$.

The system is non-causal as well as dynamic.

4. As it is an integration operation it will produce a different output for different input, so the system is invertible.

(ii)

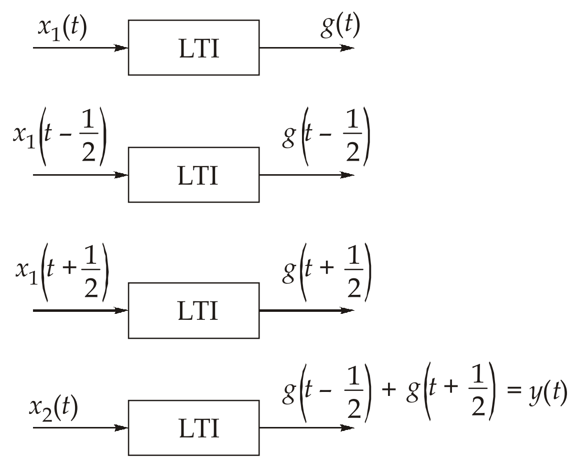




We can write,

$$x_2(t) = x_1\left(t - \frac{1}{2}\right) + x_1\left(t + \frac{1}{2}\right)$$

Since the system is LTI, we have



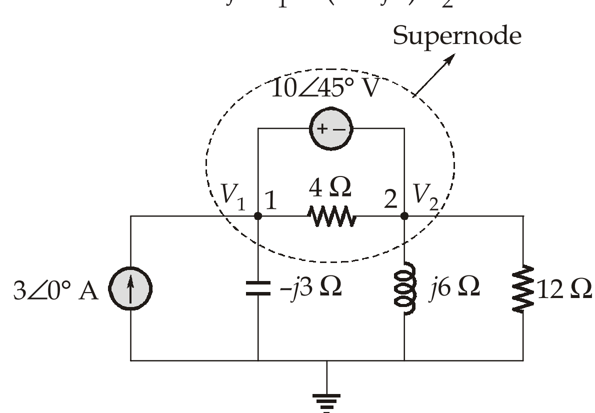
$$y(0) = g\left(-\frac{1}{2}\right)+g\left(\frac{1}{2}\right) = 3.25 + 3.25 = 6.50$$

Q.5 (c) Solution:

Nodes 1 and 2 form a supernode as shown in figure below. Applying KCL at the supernode gives

$$3 = \frac{V_1}{-j3}+\frac{V_2}{j6}+\frac{V_2}{12}$$

or $$36 = j4V_1 + (1-j2)V_2 \quad ...(1)$$



But a voltage source is connected between nodes 1 and 2, so that

$$V_1 = V_2 + 10\angle 45° \quad ...(2)$$

Substituting Eq. (2) in Eq. (1) results in

$$36 - 40\angle 135° = (1+j2)V_2 \quad \Rightarrow \quad V_2 = 31.41\angle{-87.18°}\text{V}$$

From Eq. (2),

$$V_1 = V_2 + 10\angle 45° = 25.78\angle{-70.48°}\text{ V}$$

Q.5 (d) Solution:

(i) Eigen function : If for a system, the response output is defined as scalar multiple of the input itself then the input function is defined as the eigen function of that system.

i.e., for a static LTI system having impulse response $h(t) = Af(t)$, any general signal $f(t)$ can be defined as eigen function.

(ii)
$$\sin t = \frac{e^{jt} - e^{-jt}}{j2}$$

and
$$\cos 2t = \frac{e^{j2t} + e^{-j2t}}{2}$$

$\therefore$
$$\sin t + \cos 2t = \frac{e^{jt}}{2j} - \frac{1}{2j}e^{-jt} + \frac{1}{2}e^{j2t} + \frac{1}{2}e^{-j2t}$$

(ii) Now the system difference equation is,
$$\frac{d^2y}{dt^2} + 6\frac{dy}{dt} + y(t) = 5\frac{dx}{dt} + x(t)$$

$\therefore$
$$H(j\omega_0) = \frac{5(j\omega_0)+1}{(j\omega_0)^2 + 6(j\omega_0)+1}$$

For a LTI system with impulse response $H(j\omega)$, the input $Ae^{j\omega_0 t}$ is an eigen function and the output is given by $A\left|H(j\omega_0)\right|e^{j\{at + \angle H(j\omega_0)\}}$

Now let's consider 4 different terms in the expression sin t + cos $2t$ as 4 different inputs,

$\omega_0 = 1$

$$\frac{1}{2j}e^{j1t} \longrightarrow \boxed{\text{System}} \longrightarrow \frac{1}{2j}\cdot\frac{5j+1}{(j)^2+(6j)+1}\cdot e^{j1t} = \frac{1}{2j}\left(\frac{5}{6} - j\frac{1}{6}\right)e^{j1t} = \frac{1}{2j}0.85e^{j(1t-11.31°)}$$

$\omega_0 = 1$

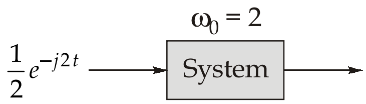
$$\frac{-1}{2j}e^{-j1t} \longrightarrow \boxed{\text{System}} \longrightarrow \frac{1}{2j}\cdot\frac{5(-j)+1}{(-j)^2+(-6j)+1}\cdot e^{-j1t} = -\frac{1}{2j}\left(\frac{5}{6} + j\frac{1}{6}\right)e^{-j1t}$$

$$= -\frac{1}{2j}0.85e^{-j(1t-11.31°)}$$

$\omega_0 = 2$

$$\frac{1}{2}e^{j2t} \longrightarrow \boxed{\text{System}} \longrightarrow \frac{1}{2}\times\frac{5(2j)+1}{(2j)^2+(12j)+1}\cdot e^{j2t} = \frac{1}{2}\left(\frac{1+10j}{-3+12j}\right)e^{j2t}$$

$$= \frac{1}{2}0.81e^{j(2t-19.75°)}$$



$$\frac{1}{2}\times\frac{5(-2j)+1}{(-2j)^2+(-12j)+1}\cdot e^{-j2t} = \frac{1}{2}\left(\frac{1-10j}{-3-12j}\right)e^{-j2t}$$

$$= \frac{1}{2}0.81e^{-j(2t-19.75°)}$$

∴ Adding 4 outputs we get,

$$y(t) = 0.85\left(\frac{e^{j(1t-11.31°)}-e^{-j(1t-11.31°)}}{2j}\right)+0.81\left(\frac{e^{j(2t-19.75°)}-e^{-j(2t-19.75°)}}{2}\right)$$

$$y(t) = 0.85\sin(t - 11.31°) + 0.81\cos(2t - 19.75°)$$

Q.5 (e) Solution:

We have,

secondary side impedance,

$$Z_{sec} = j40 + Z_2 + Z_L$$

$$Z_{sec} = j40 + (30 + j40) + (80 - j60)$$

$$Z_{sec} = (110 + j20)\ \Omega$$

Now,

secondary side impedance reflected to primary side is given by

$$Z_{ref} = \frac{(\omega M)^2}{(100+j20)} = \frac{25}{110+j20}$$

$$Z_{ref} = \left(\frac{11}{50}-\frac{1}{25}j\right)\Omega$$

Now, $Z_{in} = Z_1 + j20 + Z_{ref}$

$$= (60-j100)+j20+\frac{11}{50}-\frac{1}{25}j$$

$$= (60.22 - 80.04j)\ \Omega$$

$$= (100.16\ \angle -53.04°)\ \Omega$$

∴ current, $I_1 = \frac{V_1}{Z_{in}} = \frac{50\angle 60°}{100.16\angle -53.04°} = 0.5\angle 113.1°(A)$

Q.6 (a) Solution:

(i) The discrete time convolution of two signals $x[n]$ and $h[n]$ is given by

$$y[n] = x[n] + h[n] = \sum_{k=-\infty}^{\infty} x[k]h[n-k]$$

Following are the steps to perform discrete-time graphical convolution:

(a) Represent graphically if signals are given in form of equation.

(b) Obtain the limits of $y[n]$.

Sum of lower limits of $x[n]$ and $h[n] \leq n \leq$ sum of upper limits of $x[n]$ and $h[n]$.

(c) Change the axis from 'n' to 'k'.

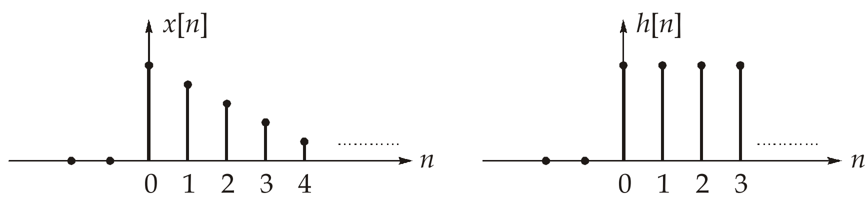
(d) Folding ($x[-k]$ or $h[-k]$).

(e) Shifting (either use $x[-k]$ or $h[-k]$ to get $x[n-k]$ or $h[n-k]$).

(f) Evaluation : Evaluate $x[k]\,h[n-k]$ by varying 'k' and summarize all the results and sketch the resultant.

Given: $$x[n] = a^n u[n],\; 0 < a < 1$$
$$h[n] = u[n]$$

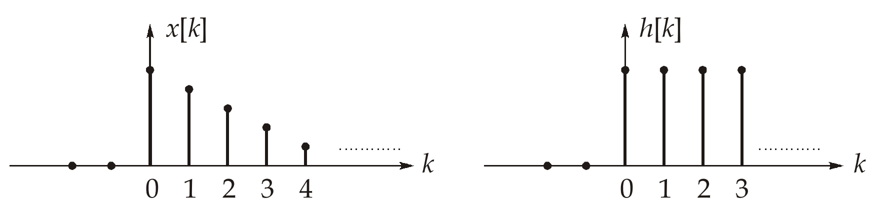
1. Represent $x[n]$ and $h[n]$ graphically



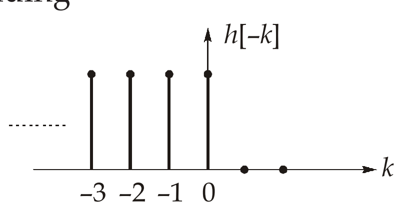
2. Limits of output

$$0 \leq n \leq \infty$$

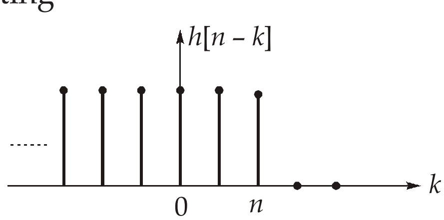
3. Change of axis from 'n' to 'k'



4. Folding

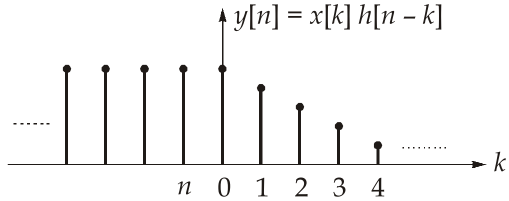


5. Shifting



6. Evaluation

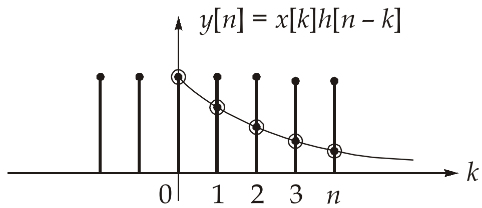
- **For $n < 0$**



Since there is no overlap.

Hence $y[n] = 0; n < 0$

- **For $n > 0$**



$$y[n] = \sum_{k=0}^{n} x[k]h[n-k]$$

$$y[n] = \sum_{k=0}^{n} a^n \cdot 1$$

$$y[n] = \frac{1-a^{n+1}}{1-a}, n \geq 0$$

- Hence the analytical expression for $y[n]$ is

$$y[n] = \begin{cases} 0 & ; \quad n < 0 \\ \dfrac{1-a^{n+1}}{1-a} & ; \quad n \geq 0 \end{cases}$$

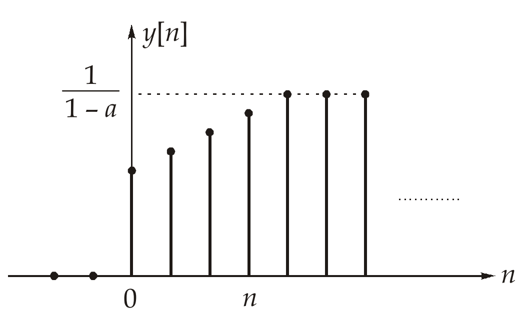
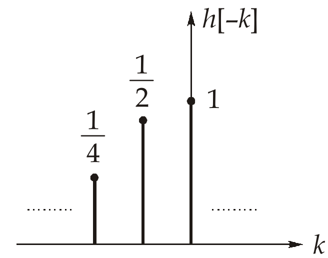


Fig.: Sketch of output signal $y[n]$

(ii) Given,

$$h[n] = \left(\frac{1}{2}\right)^n u[n]$$

The discrete time convolution of $h[n]$ and $g[n]$ is given by



$$y[n] = \sum_{k=-\infty}^{\infty} h[n-k]\, g[k]$$

$$y[0] = \sum_{k=-\infty}^{\infty} h[-k]\, g[k]$$

Since $g[n]$ is a causal sequence, meaning $g[k] = 0$ for $k < 0$

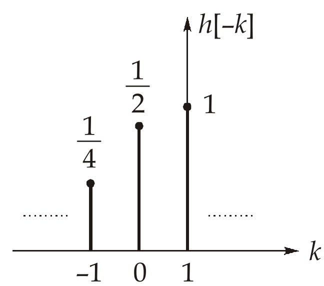
Hence, $\quad y[0] = h[0]\, g[0]$

$1 = 1\, g[0] \qquad$ {Given: $h[0] = 1$; and $y[0] = 1$}

$\therefore \quad g[0] = 1$

Now, $\quad y[1] = \sum_{k=-\infty}^{\infty} h[1-k] g[k]$

Since $h[1 - k]$ will be zero for $k > 1$ and $g[k]$ will be zero for $k < 0$ as it is a causal sequence.



$$y[1] = h[1] \cdot g[0] + h[0] \cdot g[1] \qquad \text{...(i)}$$

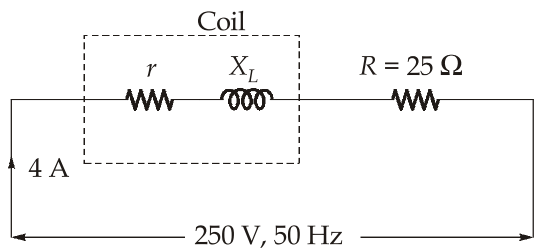
$$\frac{1}{2} = \frac{1}{2} \cdot 1 + 1 \cdot g[1] \qquad \left\{\text{Given } y[1] = \frac{1}{2}; h[1] = \frac{1}{2}\right\}$$

$$g[1] = 0$$

Hence, the obtained value for $g[1] = 0$

Q.6 (b) Solution:

(i) We have,



$$\text{Total impedance, } |Z| = \frac{250}{4} = 62.5\ \Omega$$

Hence, $Z_{equivalent} = |Z|\angle\phi$

∵ As current lag behind the voltage by 65°. Hence, $\phi = 65°$

$$Z_{eq} = 62.5\angle 65°\ \Omega = (26.41 + 56.64i)\Omega \quad \text{...(i)}$$

Now, from the circuit we get

$$Z_{eq} = (R + r) + j\omega L \quad \text{...(ii)}$$

On comparing (ii) with (i), we get

$$R + r = 26.41$$
$$25 + r = 26.41$$
$$r = 1.41\ \Omega$$

and $\omega L = 56.64$

$$L = \frac{56.64}{2\pi \times 50}$$
$$L = 0.18 \text{ Henry}$$

- Total power, $S(VA) = VI\cos\theta - jVI\sin\theta$ ...as circuit is lagging
$$= 250 \times 4\cos 65° - j250 \times 4\sin 65°$$
$$= (422.62 - j906.31)\text{VA}$$

- Power consumed by resistance ($R = 25\ \Omega$) = I^2R
$$= 4^2 \times 25$$
$$= 400 \text{ W}$$

- Power consumed by choke coil, ($r = 1.41\ \Omega$) = I^2r
$$= 4^2 \times 1.41$$
$$= 22.56 \text{ Watt}$$

- Resistance and inductance of the coil,

$$r = 1.41\ \Omega \text{ and } L = 0.18\text{ H}$$

(ii) As shown in figure below, meshes 3 and 4 form a supermesh due to the current source between the meshes. For mesh 1, KVL gives

$$-10 + (8 - j2)I_1 - (-j2)I_2 - 8I_3 = 0$$

or

$$(8 - j2)I_1 + j2I_2 - 8I_3 = 10 \quad ...(1)$$

For mesh 2, $$I_2 = -3\text{A} \quad ...(2)$$

For the supermesh,

$$(8 - j4)I_3 - 8I_1 + (6 + j5)I_4 - j5I_2 = 0 \quad ...(3)$$

Due to the current source between meshes 3 and 4, at node A,

$$I_4 = I_3 + 4 \quad ...(4)$$

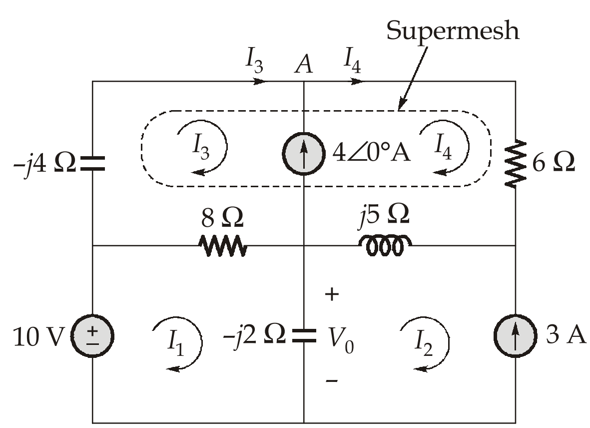
Instead of solving the above four equations, we reduce them to two by elimination.

Combining eqs. (1) and (2),

$$(8 - j2)I_1 - 8I_3 = 10 + j6 \quad ...(5)$$

Combining Eqs. (2), (3) and (4),

$$-8I_1 + (14 + j)I_3 = -24 - j35 \quad ...(6)$$



From eqs. (5) and (6), we obtain the matrix equation

$$\begin{bmatrix} 8 - j2 & -8 \\ -8 & 14 + j \end{bmatrix} \begin{bmatrix} I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} 10 + j6 \\ -24 - j35 \end{bmatrix}$$

We obtain the following determinants

$$\Delta = \begin{vmatrix} 8 - j2 & -8 \\ -8 & 14 + j \end{vmatrix} = 112 + j8 - j28 + 2 - 64 = 50 - j20$$

$$\Delta_1 = \begin{vmatrix} 10+j6 & -8 \\ -24-j35 & 14+j \end{vmatrix} = 140 + j10 + j84 - 6 - 192 - j280$$

$$= -58 - j186$$

Current I_1 is obtained as

$$I_1 = \frac{\Delta_1}{\Delta} = \frac{-58-j186}{50-j20} = 3.618\angle 274.5°\text{A}$$

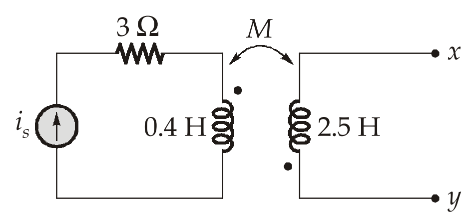
The required voltage V_0 is

$$V_0 = -j2(I_1 - I_2) = -j2(3.618\angle 274.5° + 3)$$

$$= -7.2134 - j6.568 = 9.756\angle 222.32°\text{ V}$$

Q.6 (c) Solution:

(i) When x and y are open-circuited



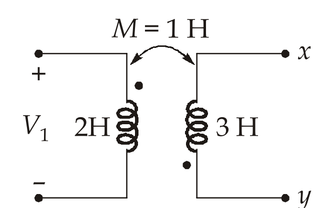
The current in the second coil $I_2 = 0$.

The energy stored is

$$W = \frac{1}{2}L_1 I_1^2 + \frac{1}{2}L_2 I_2^2 \pm M I_1 I_2$$

$$= \frac{1}{2} \times 0.4 \times 2^2 = 0.8\text{ J} \qquad [\because I_1 = i_s]$$

(ii) When x and y are short-circuited

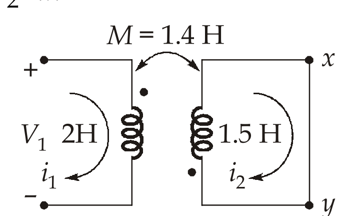


Applying KVL for the two meshes

For the mesh 1: $$V_1 = L_1\frac{di_1}{dt} - M\frac{di_2}{dt}$$

For the mesh 2: $$0 = -M\frac{di_1}{dt} + L_2\frac{di_2}{dt} \Rightarrow \frac{di_2}{dt} = \frac{M}{L_2}\frac{di_1}{dt}$$

Substituting this in the first equation,



$$V_1 = L_1\frac{di_1}{dt} - M\frac{M}{L_2}\frac{di_1}{dt}$$

$$= \left(\frac{L_1 L_2 - M^2}{L_2}\right)\frac{di_1}{dt} = L_{eq}\frac{di_1}{dt}$$

where $$L_{eq} = \frac{L_1L_2 - M^2}{L_2} = \frac{2\times3-1^2}{3} = \frac{5}{3} = 1.67$$

or, $$15 = 1.67\frac{di_1}{dt} \quad \text{or,} \quad \frac{di_1}{dt} = 9 \quad \Rightarrow \quad i_1 = 9t$$

At $t = 0.5$s, $i_1 = 9t = 9 \times 0.5 = 4.5$ A

Thus, the total energy stored in the system,

$$W = \frac{1}{2}L_{eq}i_1^2 = \frac{1}{2}\times\frac{5}{3}\times(4.5)^2 = 16.875 \text{ J}$$

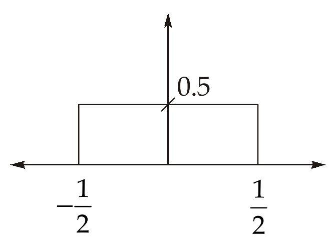
Q.7 (a) Solution:

(i) Given:

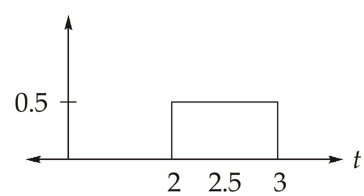
$$X(j\omega) = e^{-j5\omega/2}\left[\frac{\sin\left(\frac{\omega}{2}\right)+2\sin\left(\frac{3\omega}{2}\right)}{\omega}\right]$$

We have,

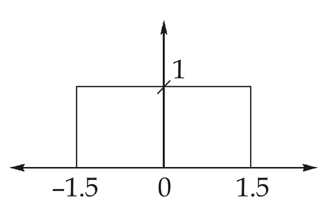
$$\frac{\sin(\omega/2)}{\omega} \xleftrightarrow{\text{IFT}}$$



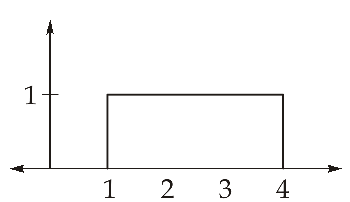
$$e^{-j(5\omega/2)}\frac{\sin(\omega/2)}{\omega} \xleftrightarrow{\text{IFT}}$$



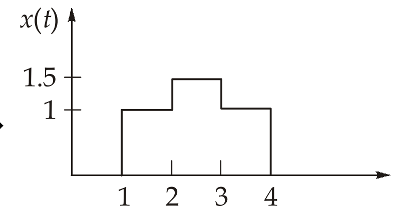
$$\frac{2\sin(3\omega/2)}{\omega} \xleftrightarrow{\text{IFT}}$$



$$2e^{-j(5\omega/2)}\frac{\sin(3\omega/2)}{\omega} \xleftrightarrow{\text{IFT}}$$



$$e^{-j(5\omega/2)}\left[\frac{\sin(\omega/2)+2\sin(3\omega/2)}{\omega}\right] \xleftrightarrow{\text{IFT}}$$



(ii) Given:

$$I = \int_{-\infty}^{2} \cos\frac{\pi}{2}t\left[\delta'(2t-1)+\delta(t-4)\right]dt$$

$$I = \int_{-\infty}^{2} \cos\frac{\pi}{2}t\cdot\delta'(2t-1)dt + \underbrace{\int_{-\infty}^{2} \cos\frac{\pi}{2}t\cdot\delta(t-4)dt}_{\Downarrow\ 0}$$

$$= \int_{-\infty}^{2} \cos\frac{\pi}{2}t\cdot\delta'(2t-1)dt$$

$$= \int_{-\infty}^{2} \cos\frac{\pi}{2}t\cdot\frac{1}{2}\delta'\left(t-\frac{1}{2}\right)dt \qquad \left[\because \delta(2t-1)=\frac{1}{2}\delta\left(t-\frac{1}{2}\right)\right]$$

$$= \frac{1}{2}\cdot\int_{-\infty}^{2} \cos\frac{\pi}{2}t\cdot\delta'\left(t-\frac{1}{2}\right)dt$$

$$= \frac{1}{2}\times(-1)\frac{d}{dt}\left(\cos\frac{\pi}{2}t\right)\bigg|_{t=1/2} \qquad \left\{\because \int_{-\infty}^{\infty} f(t)\cdot\delta'(t-a) = -f'(a)\right\}$$

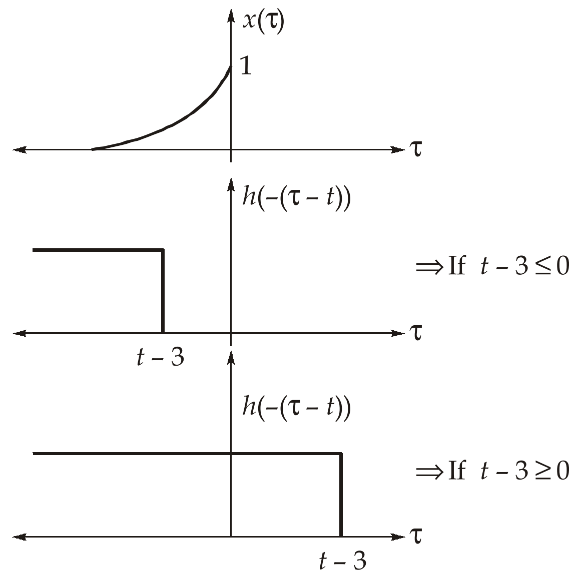
$$= \frac{-1}{2}\cdot\left(-\frac{\pi}{2}\sin\frac{\pi}{2}t\right)\bigg|_{t=1/2} = \frac{\pi}{4}\sin\frac{\pi}{4} = \frac{\pi}{4}\times\frac{1}{\sqrt{2}} = \frac{\pi}{4\sqrt{2}}$$

Q.7 (b) Solution:

(i) The output $y(t)$ of an LTI system with impulse response $h(t)$ is given by

$$y(t) = x(t) * h(t)$$

$$= \int_{-\infty}^{\infty} x(\tau)\cdot h(t-\tau)d\tau$$



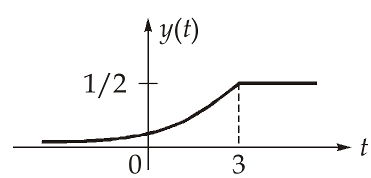
When $t - 3 \leq 0$, product of $x(\tau)\, h(t - \tau)$ is non zero for $-\infty < \tau < t - 3$

So,
$$y(t) = \int_{-\infty}^{t-3} e^{2\tau} d\tau = \frac{1}{2} e^{2(t-3)}$$

For $t - 3 \geq 0$, product of $x(\tau)\, h(t - \tau)$ is non zero for $-\infty < \tau < 0$, so $y(t)$ will be

$$y(t) = \int_{-\infty}^{0} x(\tau) h(t-\tau) d\tau = \int_{-\infty}^{0} e^{2\tau} d\tau = \frac{1}{2}$$

∴ The output $y(t)$ is



(ii)
$$y(n) = h(n) * x(n) = \sum_{k=-\infty}^{\infty} h(k) \cdot x(n-k)$$

If $x(n)$ is a unit step,

$$y(n) = \sum_{k=-\infty}^{\infty} h(k) \cdot u(n-k) = \sum_{k=-\infty}^{n} h(k)$$

The steady state value of the output is given by

$$\lim_{n \to \infty} y(n) = \sum_{k=-\infty}^{\infty} h(k)$$

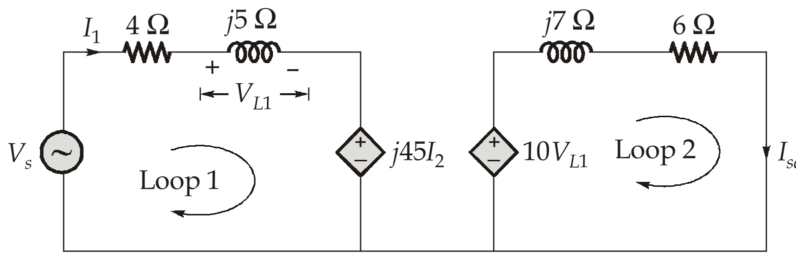
$$\therefore \quad \lim_{n\to\infty} y(n) = 3\sum_{k=0}^{\infty}\left(\frac{1}{2}\right)^k - 2\sum_{k=0}^{\infty}\left(\frac{1}{3}\right)^{k-1}$$

$$= \frac{3}{1-\frac{1}{2}} - \frac{6}{1-\frac{1}{3}} = 6 - 9 = -3$$

Q.7 (c) Solution:

Short circuit current across load 'R_L'. (I_{sc})

Short Circuiting the output terminal, we get



On applying KVL in loop 1, we get

$$-V_s + (4 + j5)I_1 + j45I_{sc} = 0 \qquad [\because I_2 = I_{sc}]$$

$$(4 + j5)I_1 + j45I_{sc} = 110\angle 53.13°\text{V} \qquad \text{...(i)}$$

Similarly from loop 2, we get

$$-10\, V_{L1} + (6 + j7)I_{sc} = 0$$

We have, $\quad V_{L1} = j65I_1$

$$-j50I_1 + (6 + j7)I_{sc} = 0$$

$$I_1 = \frac{(6+j7)I_{sc}}{j50} \qquad \text{...(ii)}$$

Using equation (ii) in (i), we get

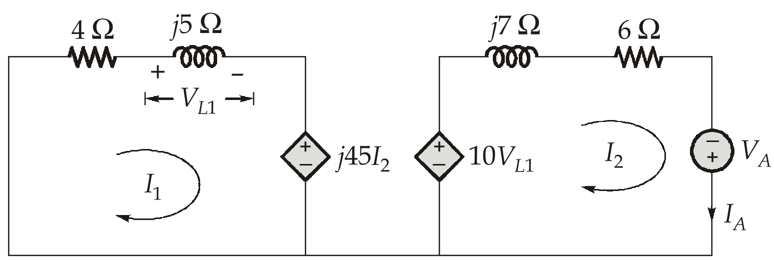
$$\frac{(4+j5)(6+j7)I_{sc}}{j50} + j45I_{sc} = 110\angle 53.13°$$

$$I_{sc} = \frac{110\angle 53.13°}{\frac{(4+j5)(6+j7)}{j50} + j45}$$

$$= 2.43 \angle -35.4°\text{A}$$

Norton equivalent impedance (Z_{th}):

Let us use a voltage source across load impedance as shown below:



On applying KVL in loop 1, we get

$$(4 + j5)I_1 + j45I_A = 0 \qquad \because I_2 = I_A$$

$$I_1 = \frac{0 - j45I_A}{(4 + j5)} \qquad \text{...(i)}$$

$$I_1 = \frac{-j45I_A}{(4 + j5)}$$

Similarly applying KVL in loop 2, we get

$$-10\,V_{L1} + (6 + 7j)I_A - V_A = 0$$

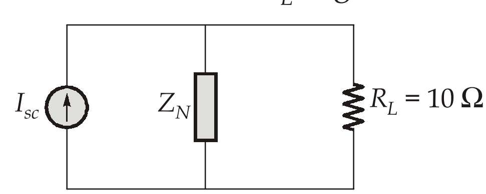
$$-10(j5I_1) + (6 + 7j)I_A = V_A$$

$$-j50\left(\frac{-j45I_A}{(4 + j5)}\right) + (6 + 7j)I_A = V_A$$

$$\frac{V_A}{I_A} = \frac{+j50(j45)}{(4 + j5)} + (6 + 7j)$$

$$Z_N = \frac{V_A}{I_A} = [353.23\angle 127.2°]\Omega = (-213.56 + j281.35)\ \Omega$$

Now, Norton equivalent circuit across load R_L is given as below



Now,

Maximum Power transfer theorem:

The maximum power transfer theorem states that the maximum power is delivered from a source to its load when the load resistance is equal to the source resistance.

Here, load resistance is not equal to the norton equivalent resistance $(R_L \neq \sqrt{R_{th}^2 + X_{th}^2})$.

Hence, it will not deliver the maximum power.

The power delivered to load is $P_L = I_L^2 R_L$

$$P_L = \left(\frac{I_{sc} \cdot Z_L}{Z_L + R_L}\right)^2 \cdot R_L$$

$$P_L = \left\{\frac{(2.43\angle -35.4°)(353.23\angle 127.2)°}{353.23\angle 127.2° + 10}\right\}^2 \times 10$$

$$P_L = \left(\frac{858.35\angle 91.8°}{347.3\angle 125.89°}\right)^2 \times 10 = 61.08 \angle -68.18° \text{ VA}$$

$$P_L = (22.7 - j56.7)\text{VA}$$

Q.8 (a) Solution:

(i) If the pf = 0.8, then

$$\cos\theta_1 = 0.8 \quad \Rightarrow \quad \theta_1 = 36.87°$$

where θ_1 is the phase difference between voltage and current. We obtain the apparent power from the real power and the pf as

$$S_1 = \frac{P}{\cos\theta_1} = \frac{4000}{0.8} = 5000 \text{ VA}$$

The reactive power is

$$Q_1 = S_1 \sin\theta = 5000 \sin 36.87° = 3000 \text{ VAR}$$

When the pf is raised to 0.95,

$$\cos\theta_2 = 0.95 \quad \Rightarrow \quad \theta_2 = 18.19°$$

The real power P has not changed. But the apparent power has changed; its new value is

$$S_2 = \frac{P}{\cos\theta_2} = \frac{4000}{0.95} = 4210.5 \text{ VA}$$

The new reactive power is

$$Q_2 = S_2 \sin\theta_2 = 4210.5 \sin 18.19° = 1314.4 \text{ VAR}$$

The difference between the new and old reactive powers is due to the parallel addition of the capacitor to the load. The reactive power due to the capacitor is

$$Q_C = Q_1 - Q_2 = 3000 - 1314.4 = 1685.6 \text{ VAR}$$

and $$C = \frac{Q_C}{\omega V_{rms}^2} = \frac{1685.6}{2\pi \times 60 \times 120^2} = 310.5\,\mu\text{F}$$

(ii) Here $R = 4\ \Omega$, $L = 25$ mH $= 0.025$ H, $Q = 50$, $V_m = 100$ V

1. $\because$ $$Q = \frac{\omega_0 L}{R} = \frac{1}{\sqrt{LC}} \times \frac{L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

$\therefore$ $$C = \frac{L}{Q^2 R^2} = \frac{0.025}{50^2 \times 4^2} = 0.625\,\mu\text{F}$$

2. $$\omega_1 = -\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}$$

$$= -\frac{4}{2 \times 0.025} + \sqrt{\left(\frac{4}{2 \times 0.025}\right)^2 + \frac{1}{0.025 \times 0.625 \times 10^{-6}}}$$

$$= -80 + 8000 = 7920 \text{ rad/s}$$

$$\omega_2 = \frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}$$

$$= \frac{4}{2 \times 0.025} + \sqrt{\left(\frac{4}{2 \times 0.025}\right)^2 + \frac{1}{0.025 \times 0.625 \times 10^{-6}}}$$

$$= 80 + 8000 = 8080 \text{ rad/s}$$

3. Average power dissipated at resonant frequency,

$$|P_{av}|_{\omega = \omega_0} = \frac{V_{rms}^2}{R} = \frac{\left(\frac{100}{\sqrt{2}}\right)^2}{2} = 1.250 \text{ kW}$$

Average power dissipated at half-power frequencies,

$$|P_{av}|_{\omega = \omega_1 = \omega_2} = \frac{|P_{av}|_{\omega = \omega_0}}{2} = \frac{1.25}{2} = 0.625 \text{ kW}$$

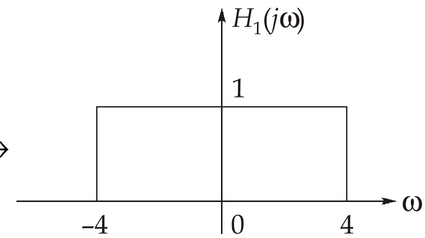
Q.8 (b) Solution:

(i) Given, impulse response $h(t) = \dfrac{\sin(4(t-1))}{\pi(t-1)}$

Let $$h(t) = h_1(t-1)$$

where, $$h_1(t) = \frac{\sin 4t}{\pi t}$$

$$h_1(t) = \frac{\sin 4t}{\pi t} \xleftrightarrow{\text{FT}}$$



Using the time-shifting property of Fourier Transform, we get

$$\therefore \qquad H(j\omega) = \begin{cases} e^{-j\omega}\ ; & |\omega| < 4 \\ 0\ ; & \text{otherwise} \end{cases}$$

given input, $$x(t) = \cos\left(6t + \frac{\pi}{2}\right)$$

By taking Fourier transform,

$$X(j\omega) = \pi e^{j\frac{\pi}{12}}\delta(\omega - 6) + \pi e^{j\frac{\pi}{12}}\delta(\omega + 6)$$

∴ The input has two frequency components at $\omega = \pm 6$

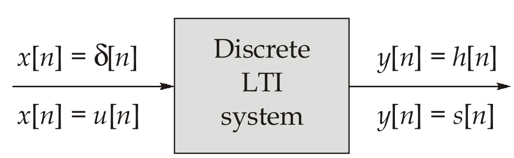
i.e., we can say that $X(j\omega)$ is zero in the passband of $H(j\omega)$.

$$\therefore \qquad Y(j\omega) = X(j\omega)H(j\omega) = 0 \quad \Rightarrow \quad y(t) = 0$$

(ii) Given, impulse response,

$$h[n] = a^n u[n]$$

For discrete LTI system,



where, $$u[n] = \sum_{K=0}^{\infty} \delta[n - K]$$

Similarly, $$s[n] = h[n] * u[n] = \sum_{K=0}^{\infty} h[n - K]$$

$$= \sum_{K=0}^{\infty} a^{n-K} u[n - K]$$

$$\because \qquad u[n - K] = \begin{Bmatrix} 1;\ n - K \geq 0 \\ \text{(or)} \\ n \geq K \end{Bmatrix}$$

Thus, $$s[n] = \sum_{K=0}^{n} a^{n-K}(1) = a^n \sum_{K=0}^{n} a^{-K}$$

$$s[n] = a^n \sum_{K=0}^{n} \left(\frac{1}{a}\right)^K = a^n \left[\frac{1-\left(\frac{1}{a}\right)^{n+1}}{1-\frac{1}{a}}\right]$$

$$= a^{n+1}\left[\frac{1-\left(\frac{1}{a}\right)^{n+1}}{a-1}\right]$$

$$s[n] = \frac{1}{a-1}\left[a^{n+1}-1\right] \text{ for; } n \geq 0$$

given, $$s[2] = 7$$

$$7 = \frac{1}{a-1}\left[a^3-1\right]$$

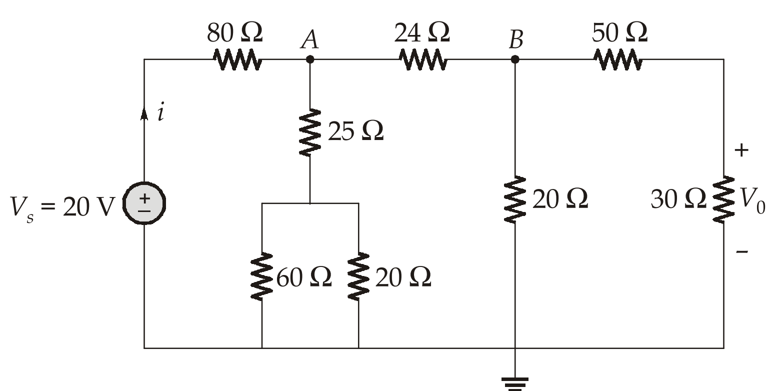
$$7 = \frac{1}{(a-1)}(a-1)(a^2+a+1)$$

$\therefore$ $$a^2 + a - 6 = 0 \Rightarrow (a+3)(a-2) = 0 \Rightarrow a = -3$$

Since $a > 0$, thus $$a = 2$$

Q.8 (c) Solution:

(i) **1.** We have,



On applying KCL at each node, we get
At node A,

$$\frac{V_A - 20}{80} + \frac{V_A - V_B}{24} + \frac{V_A}{(25 + 60 \parallel 20)} = 0$$

$$V_A\left[\frac{1}{80}+\frac{1}{24}+\frac{1}{25+60\,||\,20}\right]-\frac{V_B}{24} = \frac{1}{4}$$

$$\frac{19V_A}{240}-\frac{V_B}{24} = \frac{1}{4} \quad \text{...(i)}$$

At node B,

$$\frac{V_B-V_A}{24}+\frac{V_B}{20}+\frac{V_B}{80} = 0$$

$$\frac{-V_A}{24}+\frac{5V_B}{48} = 0 \quad \text{...(ii)}$$

From equation (i) and (ii), we get

$$V_A = 4 \text{ volt}; V_B = 1.6 \text{ volt}$$

Now, Input current, $i = \dfrac{20-V_A}{80}$

$$i = \frac{20-4}{80}$$

$$i = 0.2 \text{ A}$$

2. Output voltage, V_0

$$V_0 = \frac{V_B\times 30}{50+30} \quad \text{...(using voltage division rule)}$$

$$V_0 = \frac{1.6\times 30}{50+30}$$

$$V_0 = 0.6 \text{ Volt}$$

3. Power efficiency:

$$\text{Input power} = V_s \times i$$

$$P_i = 20 \times 0.2$$

$$P_i = 4 \text{ Watts}$$

$$\text{Output power, } P_0 = \frac{V_0^2}{R}$$

$$P_0 = \frac{(0.6)^2}{30}$$

$$P_0 = 0.012 \text{ W}$$

Thus, $$\eta = \frac{\text{Output power}}{\text{Input power}} \times 100\%$$

$$\eta = \frac{0.012}{4} \times 100$$

$$\eta = 0.3\%$$

(ii) The convolution of two continuous time signals is given by

$$y(t) = x(t) * h(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$

Thus, we have

$$z(t) = u(t+1) * r(t-2)$$

$$z(t) = \int_{-\infty}^{\infty} r(\tau-2)u(t+1-\tau)d\tau$$

$$z(t) = \int_{-\infty}^{t+1} r(\tau-2)d\tau = \int_{2}^{t+1} (\tau-2)d\tau \quad \text{...for } (t+1) \geq 2 \Rightarrow t \geq 1$$

$$z(t) = \left[\frac{\tau^2}{2} - 2\tau\right]_2^{t+1}$$

$$= \frac{1}{2}\left[\tau^2 - 4\tau\right]_2^{t+1}$$

$$= \frac{1}{2}\left[(t+1)^2 - 4(t+1) - 4 + 8\right]$$

$$= \frac{1}{2}\left[t^2 + 2t + 1 - 4t - 4 + 4\right]$$

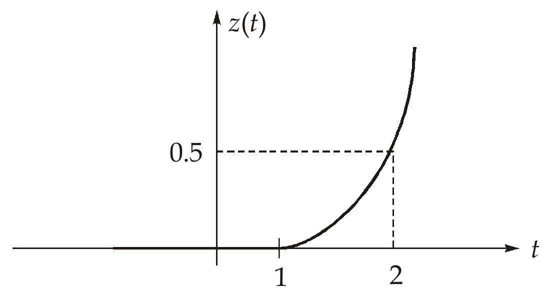
$$z(t) = \frac{1}{2}(t-1)^2 \; ; t \geq 1$$

$$z(t) = \frac{1}{2}(t-1)^2 u(t-1)$$

The function can be defined piece-wise as:

$$z(t) = \begin{cases} 0 & ; \; t < 1 \\ \frac{1}{2}(t-1)^2 & ; \; t \geq 1 \end{cases}$$

The waveform of $z(t)$ is obtained as below:



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