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Detailed Solutions

ESE-2026 Mains Test Series

Electrical Engineering Test No : 2

Section A : Digital Electronics + Microprocessors

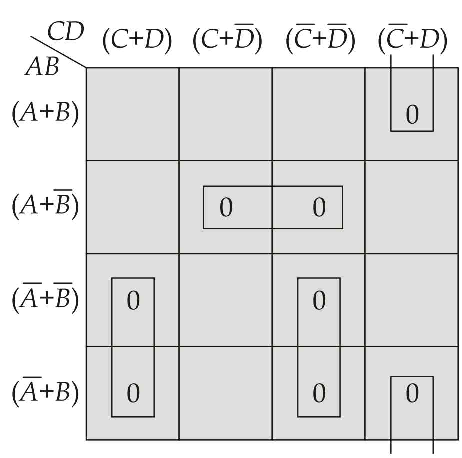
Q.1 (a) Solution:

Given : $$F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 6, 9, 13, 14)$$

For POS expression :

$$F(A, B, C, D) = \pi M(2, 5, 7, 8, 10, 11, 12, 15)$$

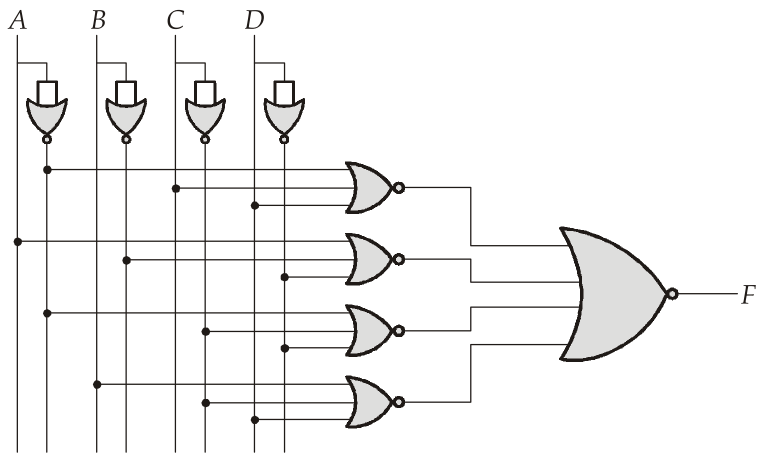
K-Map :



$$F(A, B, C, D) = (\bar{A}+C+D)(A+\bar{B}+\bar{D})(\bar{A}+\bar{C}+\bar{D})(B+\bar{C}+D)$$

$$\overline{F(A,B,C,D)} = \overline{(\bar{A}+C+D)(A+\bar{B}+\bar{D})(\bar{A}+\bar{C}+\bar{D})(B+\bar{C}+D)}$$

$$F(A, B, C, D) = \overline{\overline{(\bar{A}+C+D)}+\overline{(A+\bar{B}+\bar{D})}+\overline{(\bar{A}+\bar{C}+\bar{D})}+\overline{(B+\bar{C}+D)}}$$



Q.1 (b) Solution

An odd parity bit generator gives the output 1 when the number of 1's in the data bits is even, so that the total number of 1's in the data bits and the parity bit together is odd. Thus the truth table for this condition using four bit input is

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

K-map

$AB \backslash CD$	00	01	11	10
00	1		1	
01		1		1
11	1		1	
10		1		1

From the K-map, the output is

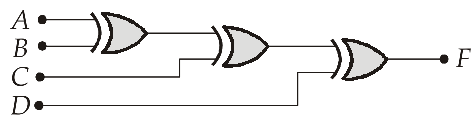
$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + AB\bar{C}\bar{D} + ABCD + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} + \bar{A}BC\bar{D}$$

$$= \bar{A}\bar{B}(\overline{C \oplus D}) + AB(\overline{C \oplus D}) + \bar{A}B(C \oplus D) + A\bar{B}(C \oplus D)$$

$$= (\overline{C \oplus D})\,(\overline{A \oplus B}) + (C \oplus D)(A \oplus B)$$

$$\therefore \quad F = \overline{A \oplus B \oplus C \oplus D}$$

Logic diagram :



Q.1 (c) Solution

(i) $$\text{Step size} = \text{Weight of } A_0 = \frac{\text{Weight of } A_1}{10} = \frac{2}{10} = 0.2 \text{ V}$$

(ii) There are 99 steps since there are two BCD digits. Thus, the full scale output is

$$V_{FS} = 99 \times \text{Step size} = 99 \times 0.2 = 19.8 \text{ V}$$

(iii) The percentage resolution is,

$$\frac{\text{Step size}}{\text{Full scale output}} \times 100\% = \frac{0.2}{19.8} \times 100\% \approx 1\%$$

(iv) The exact weights of various bits are,

MSD $\Rightarrow D_1 = 16, C_1 = 8, B_1 = 4, A_1 = 2$

LSD $\Rightarrow D_0 = 1.6, C_0 = 0.8, B_0 = 0.4, A_0 = 0.2$

One way to find V_{out} for a given input is to add the weights of all the bits that are 1's.

Therefore for an input of "0110 0100",

$$V_{out} = 8 \text{ V} + 4 \text{ V} + 0.8 \text{ V} = 12.8 \text{ V}$$

Q.1 (d) Solution:

Functional classification of 8085 instructions:

An instruction is a binary pattern designed inside a microprocessor to perform a specific function. The entire group of instructions, called the instruction set, determines what functions the microprocessor can perform.

These instructions can be classified into the following five functional categories: data transfer (copy) operations, arithmetic operations, logical operations, branching operations, and machine-control operations.

1. **Data Transfer instructions:** These instructions move (or copy) data from source to destination. The source and destination are registers and memory. Memory to memory transfer is not possible. After the data transfer, the content of the source is not modified, and the earlier content of the destination is altered.

   Example: LDA: Load Accumulator Directly from Memory

2. **Arithmetic instructions:** Arithmetic operations like addition, subtraction, increment, and decrement are performed by this category of instructions. One of the operands is taken from the Accumulator and the other operand may be from registers or memory. The result of the arithmetic operations is stored in the Accumulator.

Example: ADC: Add to Accumulator Using Carry Flag

Logical instructions: This group performs logical (Boolean) operations on data in registers and memory and on condition flags. The logical AND, OR, and Exclusive OR instructions enable you to set specific bits in the accumulator ON or OFF.

Example: XRA: Exclusive Logical OR with Accumulator

3. **Branch instructions:** Branch instructions change the sequence of the program execution unconditionally or conditionally. The condition of flags is used to take the decision for conditional branches. No flags are affected.

   JMP: Jump

4. **Stack Instructions, I/O instructions & Machine Control instructions:** The instructions dealing with interrupt handling and system operations are classified into this category. No flags are affected.

   Examples:

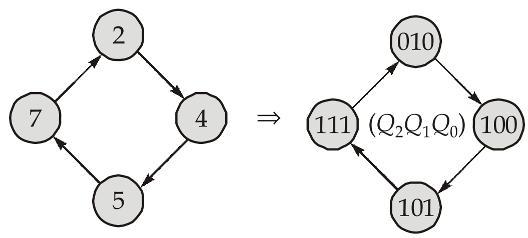
   PUSH: Push Two bytes of Data onto the Stack IN: Initiate Input Operation EI: Enable Interrupt System

Q.1 (e) Solution:

```
            LXI H, 2050H;       // memory pointer
            MVI B, 00H;         // counter
            MVI C, A3H;         // value for comparison
COMPARE:    MOV   A, M;         // this block sees if a particular TV in 19" or not
            ORA   A;
            JZ    END;
            SUB   C;
            JZ    COUNT;
            INX   H;
            JMP   COMPARE;
COUNT:      INR   B;            // this block increments the counter for a 19" TV
            INX   H;
            JMP   COMPARE;
END         MOV   A, B;         // this block provides output at port 01 H
            OUT   01H;
            HLT
```

Q.2 (a) Solution

The sequence diagram of the counter to be designed is,



Excitation table:

	Present state			Next state			Excitations		
	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
*	0	0	0	×	×	×	×	×	×
*	0	0	1	×	×	×	×	×	×
	0	1	0	1	0	0	1	1	0
*	0	1	1	×	×	×	×	×	×
	1	0	0	1	0	1	0	0	1
	1	0	1	1	1	1	0	1	0
*	1	1	0	×	×	×	×	×	×
	1	1	1	0	1	0	1	0	1

"*" indicates unused states of the counter

Minimization:

K-map for T_2

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	×	×	×	1
1			1	×

$$T_2 = Q_1$$

K-map for T_1

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	×	×	×	1
1	0	1		×

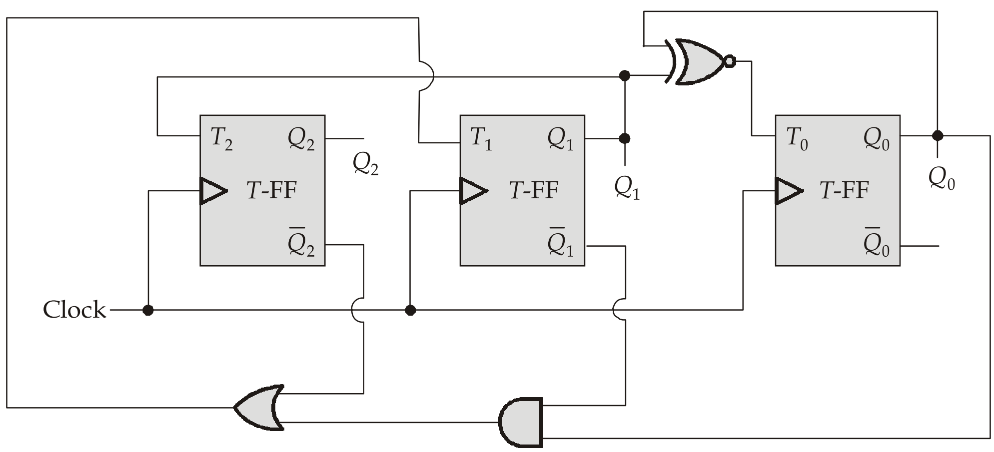
$$T_1 = \bar{Q}_2 + \bar{Q}_1Q_0$$

K-map for T_0

Q_2 \ Q_1Q_0	00	01	11	10
0	×	×	×	
1	1		1	×

$$T_0 = \bar{Q}_1\bar{Q}_0 + Q_1Q_0 = Q_1 \odot Q_0$$

Logic circuit:

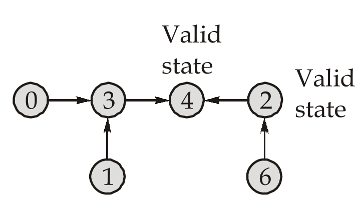


Checking for self starting:

- A counter is said to be self starting when it enters into a used or valid state from an unused state within finite number of clock cycles.
- In the above designed counter, there are four unused states (0, 1, 3, 6). In order to determine the self starting capability of the counter, the next states of the unused states are to be examined, which can be done as shown below.

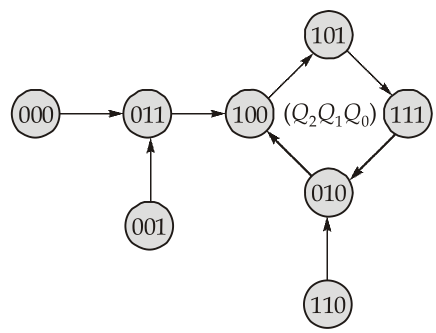
$$T_2 = Q_1$$
$$T_1 = \bar{Q}_2 + \bar{Q}_1Q_0$$
$$T_0 = Q_1 \odot Q_0$$

Present state			Excitations			Next state		
Q_2	Q_1	Q_0	T_2	T_1	T_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	1	1	0	1	1
0	0	1	0	1	0	0	1	1
0	1	1	1	1	1	1	0	0
1	1	0	1	0	0	0	1	0



- From the above sequence diagram, it is clear that, from all the unused states, the counter will enter into a valid state within finite number of clock cycles. So, the designed counter is said to be self starting.

Complete sequence diagram:



Q.2 (b) (i) Solution

- The total delay produced by the given subroutine program can be calculated by determining the total number of T-states required to execute the program.
- The total number of T-states required to execute the program can be determined by analyzing the given program as shown in the following table:

	Instruction	Number of times executed	Number of T-states for one time execution
Delay :	MVI B, 02H	1	7
LOOP2 :	MVI C, FFH	(1 × 2) = 2	7
LOOP1 :	DCR C	(255 × 2) = 510	4
	JNZ LOOP1	(254 × 2) = 508 ⇒ true (1 × 2) = 2 ⇒ false	10 ⇒ true 7 ⇒ false
	DCR B	2	4
	JNZ LOOP2	1 ⇒ true 1 ⇒ false	10 ⇒ true 7 ⇒ false
	RET	1	10

- The total delay produced by the program in terms of T-states can be given by,

$$\text{Delay} = (1 \times 7T) + (2 \times 7T) + (510 \times 4T) + (508 \times 10T) + (2 \times 7T) + (2 \times 4T) + (10T + 7T) + (10T)$$

$$= 7T + 14T + 2040T + 5080T + 14T + 8T + 17T + 10T = 7190T$$

- The time delay corresponds to one T-state is,

$$T = \frac{1}{f_{clk}} = \frac{1}{2}\,\mu s = 0.5\,\mu s \qquad \because \text{ given that, } f_{clk} = 2 \text{ MHz}$$

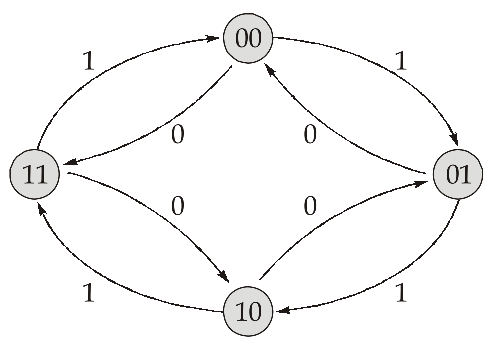
- So, the total delay produced by the program is,

$$\text{Delay} = \frac{7190}{2}\,\mu s = 3595\,\mu s \simeq 3.6\text{ ms}$$

Q.2 (b) (ii) Solution:

1. **Hardware interrupt:** These interrupts occur as signals on the external pins of the microprocessor. 8086 has two pins to accept hardware interrupts, NMI and INTR.
2. **Software interrupt:** These are caused by writing the software interrupt instructions INTn where n can be any value from 0 to 255 (00H to FFH). Hence all 256 interrupts can be invoked by software.
3. **Error conditions:** 8086 is interrupted when some special conditions occur while executing contain instructions in the program. Eg. An error in division automatically causes the INTO interrupt.

Q.2 (c) Solution:



State Diagram

State Table

Present State		Next State			
		X = 0		X = 1	
A	B	A	B	A	B
0	0	1	1	0	1
0	1	0	0	1	0
1	0	0	1	1	1
1	1	1	0	0	0

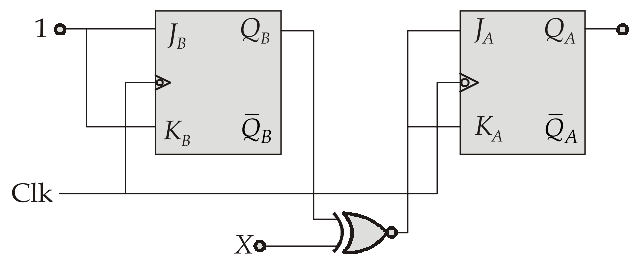
Input Table

Counter State			Flip Flop Inputs			
X	Q_A	Q_B	J_A	K_A	J_B	K_B
0	0	0	1	×	1	×
0	0	1	0	×	×	1
0	1	0	×	1	1	×
0	1	1	×	0	×	1
1	0	0	0	×	1	×
1	0	1	1	×	×	1
1	1	0	×	0	1	×
1	1	1	×	1	×	1

$$J_B = K_B = 1$$

$$J_A = K_A = (Q_B \odot X)$$

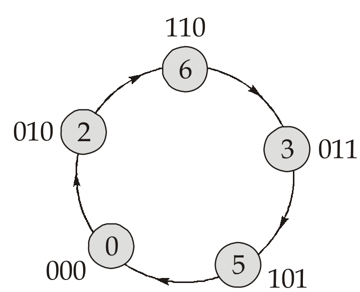
Circuit is



Mudulo-4 UP/DOWN Counter

Q.3 (a) (i) Solution:

The state transition diagram for the given count sequence



The state table for the given count sequence is

State Transition Table		Inputs of flip-flops		
Present state	Next state	*D* flip-flop		
Q_2 Q_1 Q_0	Q_2^+ Q_1^+ Q_0^+	D_2	D_1	D_0
1 1 0	0 1 1	0	1	1
0 1 1	1 0 1	1	0	1
1 0 1	0 0 0	0	0	0
0 0 0	0 1 0	0	1	0
0 1 0	1 1 0	1	1	0

From the state table, the logical expression for the *D* flip-flop inputs as

For D_2, $$D_2 = \bar{Q}_2Q_1Q_0 + \bar{Q}_2Q_1\bar{Q}_0 = \bar{Q}_2Q_1(Q_0 + \bar{Q}_0)$$

$\Rightarrow$ $$D_2 = \bar{Q}_2Q_1$$

For D_1, $$D_1 = Q_2Q_1\bar{Q}_0 + \bar{Q}_2\bar{Q}_1\bar{Q}_0 + \bar{Q}_2Q_1\bar{Q}_0$$

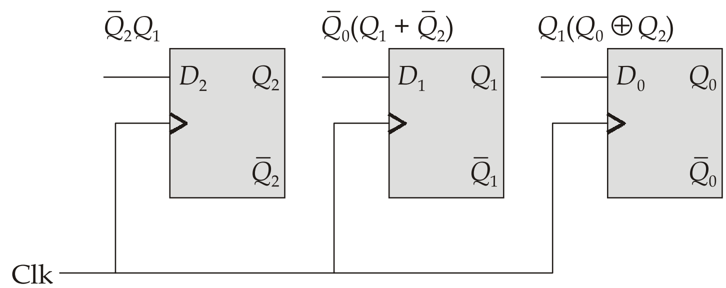
$\Rightarrow$ $$D_1 = Q_1\bar{Q}_0 + \bar{Q}_2\bar{Q}_0 = \bar{Q}_0(Q_1 + \bar{Q}_2)$$

For D_0,

$$D_0 = Q_2Q_1\bar{Q}_0 + \bar{Q}_2Q_1Q_0 = Q_1(Q_2\bar{Q}_0 + \bar{Q}_2Q_0)$$

$$D_0 = Q1(Q_0 \oplus Q_2)$$

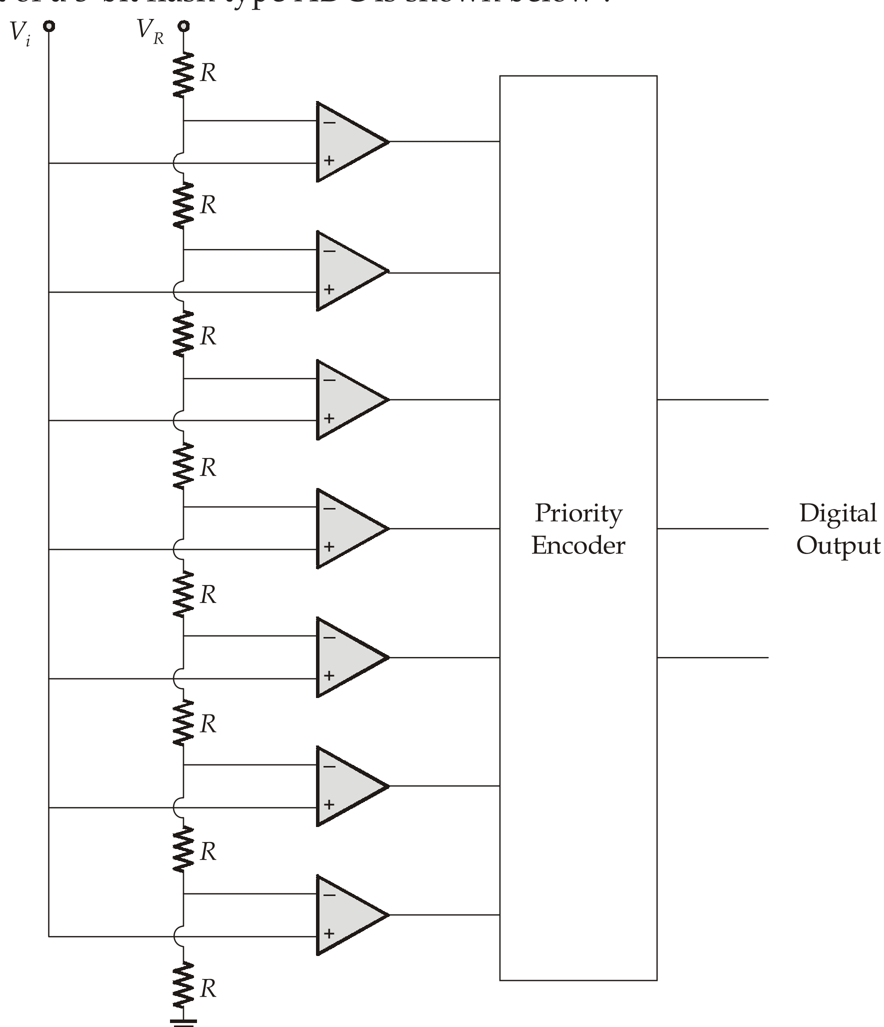
The synchronous counter for the given sequence is designed using inputs D_2, D_1 and D_0 as:



Synchronous counter using *D* flip-flop

Q.3 (a) (ii) Solution:

The circuit of a 3-bit flash type ADC is shown below :



The 3-bit flash type ADC consists of a voltage divider network having 7 comparator and a priority encoder.

The working of 3-bit flash type ADC is as follows :

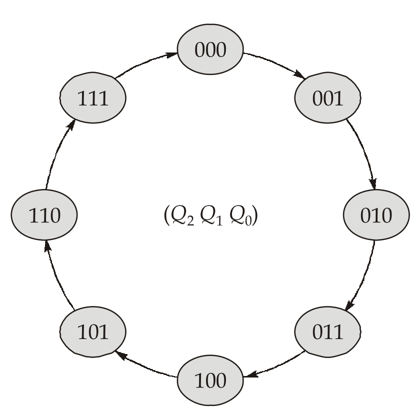
- The voltage divider network contains 8 equal resistors. A reference voltage V_R is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom-to-top with respect to ground will be the integer multiple of $\frac{V_R}{8}$.
- The external input voltage V_i is applied to the non-inverting terminals of all comparators. The voltage drop across each resistor from bottom-to-top is applied to the inverting terminal of the comparator.
- At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminals. That means the comparison operations take place by each comparator parallelly.
- The output of the comparator will be '1' as long as V_i is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when V_i is less than or equal to the voltage drop present at the respective other input terminal.
- All the outputs of comparators are connected as the inputs of priority encoder. This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.
- Therefore, the output of priority encoder is nothing but the binary equivalent (digital output) of external analog input voltage V_i.

Q.3 (b) Solution

(i) Design of a synchronous 3-bit binary up-counter:

Number of flip-flops required = 3

Sequence diagram:

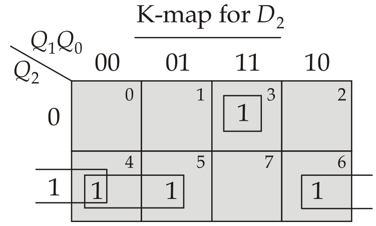


Excitation table:

Present state			Next state			Excitations		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

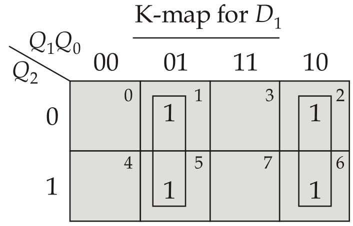
Minimization:

K-map for D_2



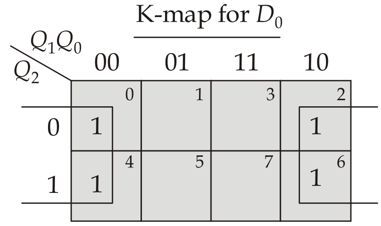
$$D_2 = Q_2\bar{Q}_1 + Q_2\bar{Q}_0 + \bar{Q}_2Q_1Q_0$$

K-map for D_1



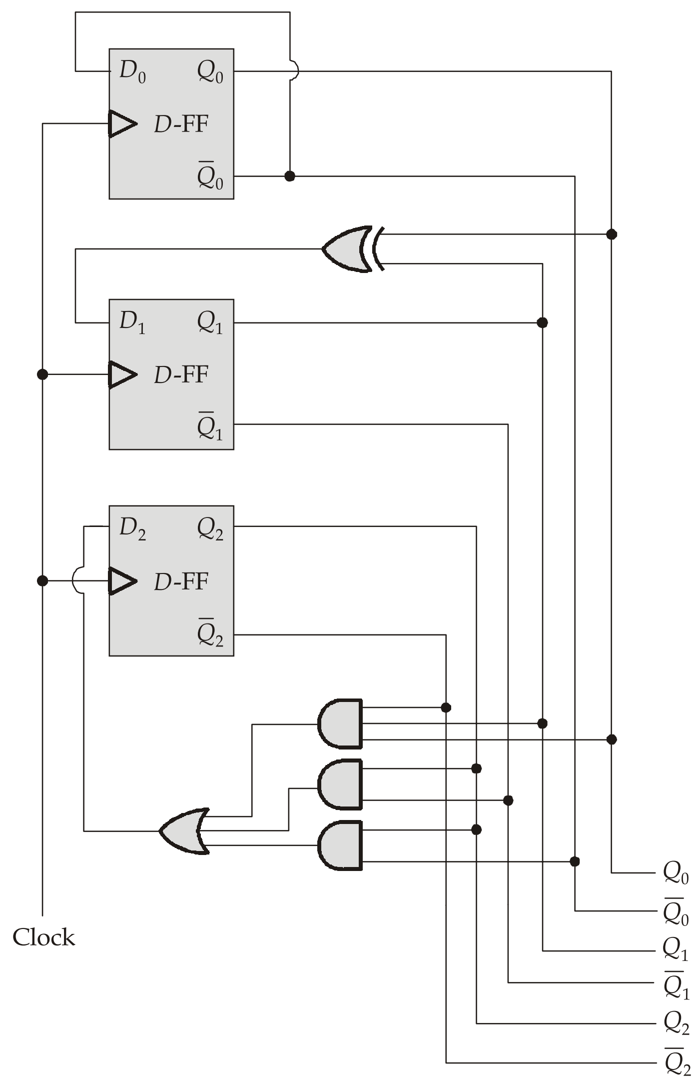
$$D_1 = \bar{Q}_1Q_0 + Q_1\bar{Q}_0 = Q_1 \oplus Q_0$$

K-map for D_0



$$D_0 = \bar{Q}_0$$

Logic circuit:



(ii) To design the necessary signal waveforms for stepper motor:

- Each of the given periodic signal waveforms has a period of 40 ms and the 3-bit binary counter has 8 unique states. So, we have to select the clock frequency such that 8 clock cycles should cover a time period of 40 ms.

So,
$$T_{clock} = \frac{40}{8}\text{ms} = 5 \text{ ms}$$

Required clock frequency,

$$f_{clock} = \frac{1}{T_{clock}} = \frac{1000}{5}\text{Hz} = 200 \text{ Hz}$$

- The additional circuitry, apart from the counter designed in part (i), can be designed by using the following truth table.

Counter outputs			Required signals			
Q_2	Q_1	Q_0	ϕ_1	ϕ_2	ϕ_3	ϕ_4
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

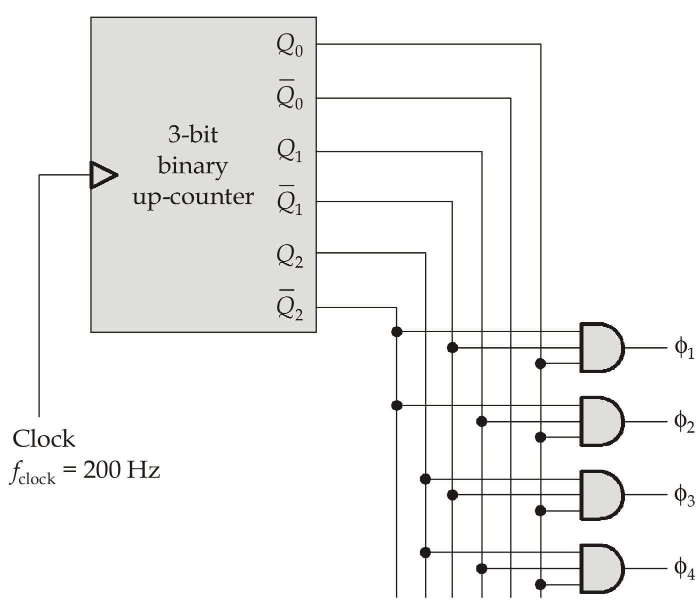
$$\phi_1 = \bar{Q}_2\bar{Q}_1Q_0$$

$$\phi_2 = \bar{Q}_2Q_1Q_0$$

$$\phi_3 = Q_2\bar{Q}_1Q_0$$

$$\phi_4 = Q_2Q_1Q_0$$

Logic circuit:



Q.3 (c) (i) Solution:

8086 has a 16-bit flag register which is divided into two parts, viz. (a) condition code or status flags and (b) machine controls flags. The condition code flag register is the lower byte of the 16-bit flag register along with overflow flag. This part is identical to the 8085 flag register, with an additional overflow flag, which is not present in 8085. This part of the flag register of 8086 reflects the results of the operations performed by ALU. The control flag register is the higher byte of the flag register of 8086. It contains three flags, viz. direction flag (D), interrupt flag (I) and trap flag (T).

The complete bit configuration of 8086 flag register is shown below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	O	D	I	T	S	Z	X	AC	X	P	X	CY

O - Overflow flag
D - Direction flag
I - Interrupt flag
T - Trap flag
S - Sign flag
Z - Zero flag
AC - Auxiliary carry flag
P - Parity flag
CY - Carry flag
X - Not used

The description of each flag bit is as follows:

Sign Flag (S) : This flag is set when the result of any computation is negative. For signed computations, the sign flag equals to the MSB of the result.

Zero Flag (Z) : This flag is set if the result of the computation or comparison performed by the previous instruction/instructions is zero.

Parity Flag (P) : This flag is set to 1 if the lower byte of the result contains even number of 1s.

Carry Flag (CY) : This flag is set when there is a carry out of MSB in case of addition or a borrow in case of subtraction.

Trap Flag (T) : If this flag is set, the processor enters the single step execution mode. In other words, a trap interrupt is generated after execution of each instruction. The processor executes the current instruction and the control is transferred to the Trap interrupt service routine.

Interrut Flag (I) : If this flag is set, the maskable interrupts are recognised by the CPU, otherwise they are ignored.

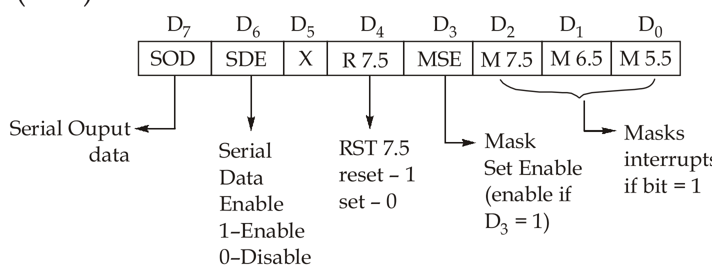
Direction Flag (D) : This is used by string manipulation instructions. If this flag bit is '0', the string is processed beginning from the lowest address to the highest address, i.e. autoincrementing mode. Otherwise, the string is processed from the highest address towards the lowest address, i.e. autodecrementing mode.

Auxiliary Carry Flag (AC) : This is set if there is a carry from the lowest nibble, i.e. bit three, during addition or borrow for the lowest nibble, i.e. bit three, during subtraction.

Overflow Flag (O) : This flag is set if an overflow occurs, i.e. if the result of a signed operation is large enough to be accomodated in a destination register. For example, in case of the addition of two signed numbers, if the result overflows into the sign bit, i.e. the result is of more than 7-bits in size in case of 8-bit signed operations and more than 15-bits in size in case of 16-bit signed operations, then the overflow flag will be set.

Q.3 (c) (ii) Solution:

Set Interrupt Mask (SIM):



Functions of SIM:

1. Used to implement 8085 interrupts.
2. Used to implement serial data output.

Q.4 (a) (i) Solution:

Direct Memory Access (DMA) is a technique used in computer architecture to allow peripherals to communicate directly with memory without involving the CPU. The 8085 microprocessor, however support DMA using HOLD and HLDA signals, but requires an external DMA controller, so DMA operations typically require additional hardware components. Some general steps involved in DMA data transfer are given below :

1. **Initialization :**
   - Configure the DMA controller, if present, to set up the DMA transfer mode and other parameters.
   - Set the source and destination addresses for data transfer.
   - Specify the number of bytes or words to transfer.
2. **Request DMA :**
   - The peripheral device that needs to transfer data initiates a DMA request to the DMA controller.
3. **DMA Controller Acknowledgement :**
   - The DMA controller acknowledges the DMA request and gains control of the system buses.

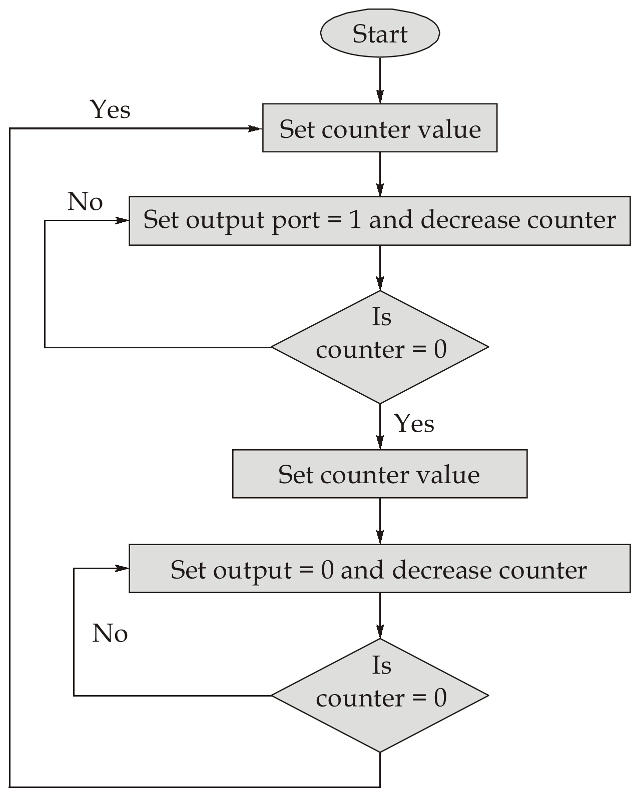
4. **Memory Access :**
   - The DMA controller reads data from the source memory location and writes it to the destination memory location directly, bypassing the CPU.
5. **Transfer Completion :**
   - After the specified amount of data is transferred, the DMA controller releases control of the system buses back to the CPU.

Functions of 8085 pins used in DMA data transfer :

1. **Hold (HOLD) :**
   - When this pin is held high (active), it indicates that the 8085 CPU should enter the hold state. This is used during DMA to allow external DMA controllers to gain control of the system buses.
2. **Hold Acknowledge (HLDA) :**
   - This is the acknowledgement signal from the CPU indicating that it has entered the hold state and released the address, data and control bues.
3. **Memory Read (RD) and Memory Write (WR) :**
   - These pins control the memory read and write cycles. During DMA, the external controller may use these pins to read from or write to memory.
4. **Status (S0, S1, S2) :**
   - These status pins are used to indicate the type of operation being performed. In the case of DMA, they may signal that a memory write cycle is taking place.
5. **Data Bus (AD0-AD7) :**
   - The data bus is used to transfer data between the DMA controller and memory. During DMA, data is moved between these pins.
6. **Address Bus (A0-A15) :**
   - The address bus specifies the memory location to read from or write to. During DMA, the external controller sets the address bus to the desired memory location.

Q.4 (a) (ii) Solution:

This can be done by pulling 1 on the output port and then putting zero on the output port for the same duration. We can change the counter value to change bit rate.



Q.4 (b) Solution

Main Program:

	LXI D, 2050H	;	Point index to readings
	LXI H, 2090H	;	Point index to maximum limits
	MVI C, 05H	;	Set up C as a counter with a count value of 5
NEXT:	CALL SBTRAC	;	Call the subroutine to perform 16-bit subtraction to determine the difference between a reading and its maximum limit.
	INX D	;	Increment the contents of DE pair to point the location of next reading.
	INX H	;	Increment the contents of HL pair to point the location of maximum limit corresponding to the next reading.
	DCR C	;	Decrement the count value after completion of the process corresponding to each reading.

	JNZ NEXT	;	Jump to the location labeled as "NEXT" till the count value of the counter becomes zero, to start the process corresponding to the next reading.
	HLT	;	Halt the execution

Subroutine:

SBTRAC:	MOV A, M	;	Load the accumulator with lower byte of the maximum limit corresponding to the reading.
	XCHG	;	Exchange the contents of HL and DE pairs.
	SUB M	;	Subtract lower byte of the reading from the lower byte of the corresponding maximum limit.
	MOV M, A	;	Store the lower byte of the difference in the location corresponding to the lower byte of the reading.
	XCHG	;	Exchange the contents of HL and DE pairs
	MOV A, M	;	Load the accumulator with higher byte of the maximum limit corresponding to the reading.
	XCHG	;	Exchange the contents of HL and DE pairs.
	SBB M	;	Subtract (with borrow) higher byte of the reading from the higher byte of the corresponding maximum limit.
	MOV M, A	;	Store the higher byte of the difference in the location corresponding to the higher byte of the reading.
	CC INDCTR	;	Call the indicator subroutine if the value of reading is higher than the corresponding maximum limit.
	XCHG	;	Exchange the contents of HL and DE pairs.
	RET	;	Return to the Main Program.

Q.4 (c) Solution:

(i) Let the base be x

Then,
$$292 = (1 \times x^3) + (2 \times x^2) + (0 \times x) + (4 \times 1)$$
$$292 = x^3 + 2x^2 + 4$$
$$x^3 + 2x^2 - 288 = 0$$

On solving we get,
$$x = 6, (-4 + 5.7i), (-4 - 5.7i)$$

As base of the number system must be real hence
$$x = (-4 \pm 5.7i) \text{ are discarded.}$$

Therefore $(292)_{10}$ = 1204 is valid when base of the number system is 6 i.e. $(1204)_6$.

(ii) If 1st number is taken in binary, then it is $(16)_{10}$

$$(121)_3 = (16)_{10}$$
$$(100)_4 = (16)_{10}$$
$$(24)_6 = (16)_{10}$$
$$(22)_7 = (16)_{10}$$
$$(20)_8 = (16)_{10}$$

$\therefore$ The missing number is to be the base 5

$$(x)_5 = (16)_{10}$$

$$\Rightarrow \quad x = 31$$

(iii)

```
 ①①①①  ①①
  1 1 0 1 . 1 0 1
+   1 1 1 . 0 1 1
-----------------
1 0 1 0 1 . 0 0 0  = (21)10
```

(iv) We need to find 46 - 14 using 8-bit 2's complement.

Finding complement of 14:

$$+14 = 00001110$$
$$-14 = 11110010 \text{ (2's complement form)}$$

```
 46 =    0 0 1 0 1 1 1 0
–14 =  +1 1 1 1 0 0 1 0
      ①0 0 1 0 0 0 0 0
```

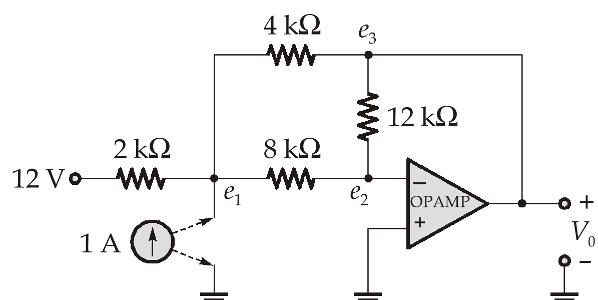
Ignore the carry. MSB is 0, so the result is positive and in normal binary form

$\therefore$ Answer is +00100000 = +32

Section B : Electrical Circuits-1 + Systems and Signal Processing-1

Q.5 (a) Solution:

Open-circuiting the 4-kΩ resistor,



Here, $e_2 = 0, \quad e_3 = V_0$

$$\frac{e_1 - 12}{2\times10^3} + \frac{e_1 - V_0}{4\times10^3} + \frac{e_1}{8\times10^3} = 0$$

$$\Rightarrow \quad 7e_1 = (48 + 2V_0) \quad ...(i)$$

$$\frac{0 - e_1}{8\times10^3} + \frac{0 - V_0}{12\times10^3} = 0$$

$$\Rightarrow \quad V_0 = -\frac{3}{2}e_1 \quad ...(ii)$$

From (i) and (ii),

$$e_1 = 4.8 \text{ V} = e_{oc}$$

Now, we connect a 1-A current source at the place of the 4-kΩ resistor,

By KCL at the node-1,

$$\frac{e_1}{2\times10^3} + \frac{e_1 - V_0}{4\times10^3} + \frac{e_1}{8\times10^3} = 1$$

$$\Rightarrow \quad 7_{e1} = 8000 + 2V_0$$

By KCL at the node-2,

$$V_0 = -\frac{3}{2}e_1$$

$$\Rightarrow \quad 7e_1 = 8000 + 2\left(-\frac{3}{2}e_1\right)$$

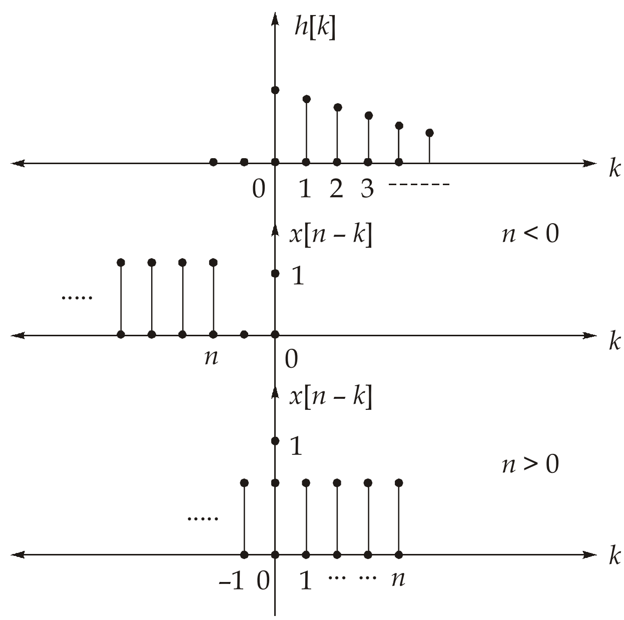
$$\Rightarrow \quad e_1 = 800 \text{ V}$$

$$\therefore \quad R_{th} = \frac{e_1}{1} = 800\ \Omega$$

$$\therefore \quad i = \frac{4.8}{4000 + 800} = \frac{4.8}{4.8\times10^3} = 1 \text{ mA}$$

Q.5 (b) Solution:

$$y[n] = h[n] * x[n] = \sum_{k=-\infty}^{\infty} h[k]\, x[n-k]$$



For $n < 0$; there is no overlap between $h[k]$ and $x[n-k]$.

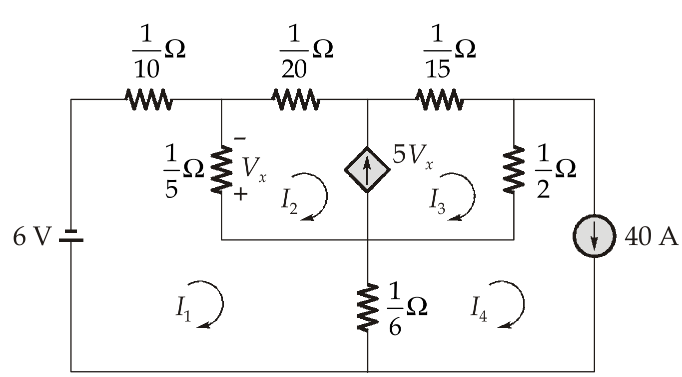
$\therefore \qquad y[n < 0] = 0$

For $n > 0$; overlap of $h[k]$ and $x[n-k]$ is from $k = 0$ to $k = n$.

$$y[n] = \sum_{k=0}^{n} a^k = \frac{1-\alpha^{n+1}}{1-\alpha} \qquad \text{...(sum of G.P.)}$$

$$y[n] = \frac{1-\alpha^{n+1}}{1-\alpha}$$

Q.5 (c) Solution:



$$I_4 = 40 \text{ A} \qquad \text{...(i)}$$

Meshes 2 and 3 form a supermesh, writing current equation for supermesh,

$$I_3 - I_2 = 5V_x$$

$$V_x = \frac{1}{5}(I_2 - I_1)$$

$$I_3 = 2I_2 - I_1 \qquad \text{...(ii)}$$

Applying KVL to supermesh,

$$-\frac{1}{5}(I_2 - I_1) - \frac{1}{20}I_2 - \frac{1}{15}I_3 - \frac{1}{2}(I_3 - I_4) = 0 \qquad \text{...(iii)}$$

$$46I_1 - 83I_2 = -1200$$

Applying KVL to mesh-1,

$$-6 - \frac{1}{10}I_1 - \frac{1}{5}(I_1 - I_2) - \frac{1}{6}(I_1 - I_4) = 0$$

$$-7I_1 + 3I_2 = -10 \qquad \text{...(iv)}$$

Solving equation (iii) and (iv),

$$I_1 = 10 \text{ A}$$

and $$I_2 = 20 \text{ A}$$

$$I_3 = 2(20) - 10$$

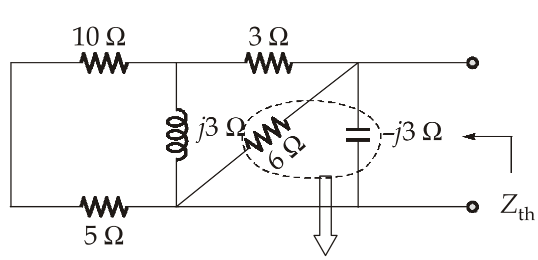
$$= 30 \text{ A}$$

$$I_4 = 40 \text{ A}$$

Q.5 (d) Solution:

Step-I: Calculation of Z_{Th}:

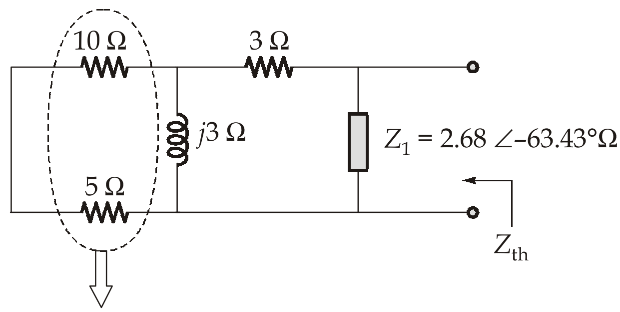
For calculation of equivalent impedance across load impedance, (Z_{Th}) we have to deactivate all the independent voltage and current source i.e., replace voltage source by short circuit and current source by open circuit. We can redraw the circuit as shown below:



6 Ω and $-j3\Omega$ are in parallel. Hence,

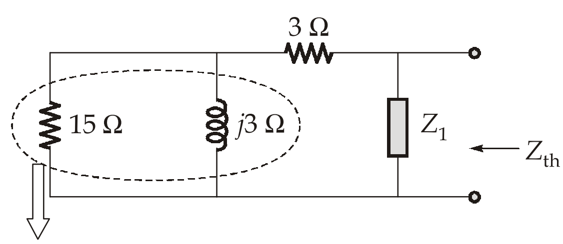
Hence, $$Z_1 = 6\Omega \parallel -j3\Omega = \frac{6 \times (-j3)}{6 - j3} = 2.68\angle -63.43^\circ\ \Omega$$

The simplified circuit can be drawn as below:



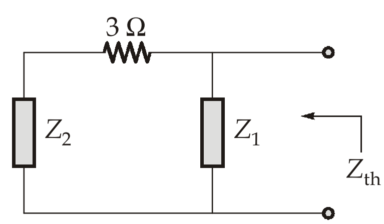
10 Ω and 5Ω are series. Hence,

Hence, $$10 + 5 = 15\ \Omega$$



$$Z_2 = 15 \parallel j3 = \frac{15 \times j3}{15 + j3}$$

$$Z_2 = 2.94\ \angle\ 78.70^\circ\ \Omega$$



$$Z_{th} = (Z_2 + 3) \parallel Z_1$$

$$Z_{th} = (2.94(\angle 78.70^\circ + 3)) \parallel (2.68\ \angle -63.43^\circ)$$

$$Z_{th} = (4.60\ \angle 38.87^\circ) \parallel (2.68\ \angle -63.43^\circ)$$

$$Z_{th} = \frac{(4.60\angle 38.87^\circ)(2.68\angle -63.43^\circ)}{(4.60\angle 38.87^\circ) + (2.68\angle -63.43^\circ)}$$

$$= \frac{12.328\angle -24.56^\circ}{48\angle 5.85^\circ}$$

$$Z_{th} = 2.57\ \angle -30.41^\circ\ \Omega$$

Step-II:

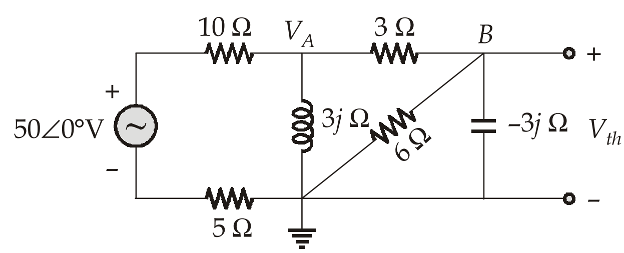
For maximum power transfer, $Z_L = Z^*_{Th}$

$$Z_L = 2.57\angle{+30.41°}\ \Omega = (2.216 + j1.3)\ \Omega$$

Step-III:

Calculation of V_{th}:

For calculation of V_{th}, assume load impedance to be infinite and calculate voltage across it, i.e.,



Apply KCL at node A,

$$\frac{V_A - 50\angle 0°}{15} + \frac{V_A}{3j} + \frac{V_A - V_{th}}{3} = 0$$

$$V_A\left[\frac{1}{15} + \frac{1}{3j} + \frac{1}{3}\right] + V_{th}\left[\frac{-1}{3}\right] = 3.33$$

$$V_A(0.52\angle{-39.81°}) - V_{th}0.33 = 3.33 \qquad \text{...(i)}$$

Similarly, writing KCL at node B,

$$\frac{V_{th} - V_A}{3} + \frac{V_{th}}{(6\,\|\,-3j)} = 0 \qquad \because 6\,\|\,-3j = Z_1 = 2.68\angle{-63.43°}\ \Omega$$

$$V_{th}\left[\frac{1}{3} + \frac{1}{2.68\angle -63.43°}\right] + V_A\left[-\frac{1}{3}\right] = 0$$

$$V_{th}[0.60\angle 33.70°] - V_A 0.33 = 0 \qquad \text{...(ii)}$$

Write equation (i) and (ii) in matrix form,

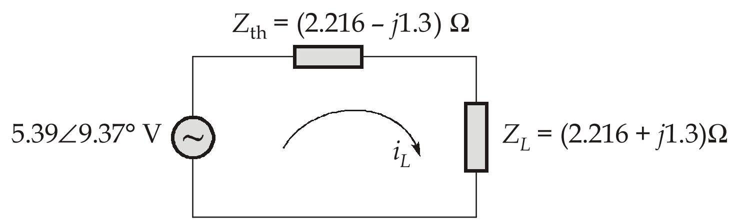
$$\begin{bmatrix} 0.52\angle -39.81° & -0.33 \\ -0.33 & 0.60\angle 33.70° \end{bmatrix}\begin{bmatrix} V_A \\ V_{th} \end{bmatrix} = \begin{bmatrix} 3.33\angle 0° \\ 0 \end{bmatrix}$$

Using Cramer's rule,

$$V_{th} = \frac{\begin{vmatrix} 0.52\angle -39.81° & 3.33\angle 0° \\ -0.33 & 0 \end{vmatrix}}{\begin{vmatrix} 0.52\angle -39.81° & -0.33 \\ -0.33 & 0.60\angle 33.70° \end{vmatrix}} = 5.39\angle 9.37°\ \text{Volt}$$

Step-IV:

Calculation of maximum power, P_{max}



$$P_{max} = I_L^2 R_L \,, \qquad \text{where } I_L = \frac{5.39\angle 9.37°}{4.432}$$

$$P_{max} = (1.22)^2(2.216) \qquad I_L = 1.22\angle 9.37° \text{ A}$$

$$P_{max} = 3.30 \text{ W}$$

Q.5 (e) Solution:

In series RLC circuit,

$$I = \frac{V}{R + j\left(\omega L - \frac{1}{\omega C}\right)}$$

$$|I| = \frac{V}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}$$

At half power points,

$$I = \frac{I_0}{\sqrt{2}}$$

where, $I_0 = \frac{V}{R}$ (Current at resonance)

$$\frac{V}{\sqrt{2}\,R} = \frac{V}{\sqrt{R^2 + \left(\omega L - \frac{1}{C\omega}\right)^2}}$$

$$\omega L - \frac{1}{\omega C} = \pm R$$

At lower half power point,

$$\omega_1 L - \frac{1}{\omega_1 C} = -R$$

$$\omega_1^2 + \frac{R}{L}\omega_1 - \frac{1}{LC} = 0$$

$$\omega_1 = \frac{-R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}$$

At upper half power point,

$$\omega_2 L - \frac{1}{\omega_2 C} = R$$

$$\omega_2^2 - \frac{R}{L}\omega_2 - \frac{1}{LC} = 0$$

$$\omega_2 = \frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}$$

$$\omega_1 \omega_2 = \left[-\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}\right]\left[\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}\right] = \frac{1}{LC}$$

$$\therefore \quad \omega_1 \omega_2 = \omega_0^2$$

$$\therefore \quad \omega_0 = \sqrt{\omega_1 \omega_2}$$

Q.6 (a) Solution:

(i) We have,

Transmission parameter matrix,

$$[T] = \begin{bmatrix} 10^{-2} & 10^2\ \Omega \\ 0\ \mho & 10^{-1} \end{bmatrix}$$

Thus, we can write

$$V_1 = 0.01V_2 - 100I_2$$

$$I_1 = -0.1I_2$$

As the given equivalent circuit is similar to h-parameter equivalent circuit. Hence, *h*-parameter of the circuit is obtained as below:

$$I_2 = -10I_1 \quad \text{...(i)}$$

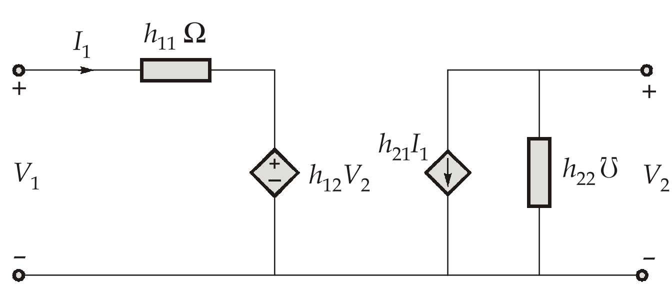
and

$$V_1 = 0.01V_2 + 1000I_1 \quad \text{...(ii)}$$

The *h*-parameter equations and the corresponding equivalent circuit is given by

$$V_1 = h_{11}I_1 + h_{12}V_2$$

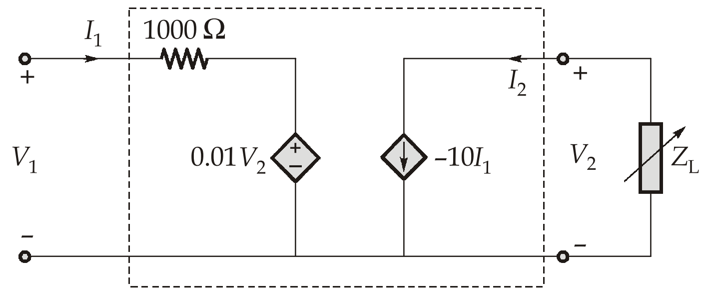
$$I_2 = h_{21}I_1 + h_{22}V_2$$



On comparing, we get

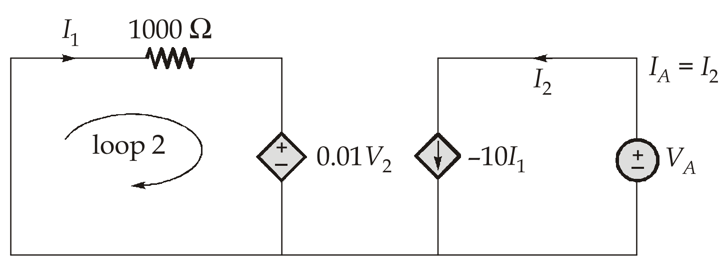
$$h_{11} = R_1 = 1000\ \Omega; \quad h_{12} = x = 0.01$$
$$h_{21} = y = -10; \quad h_{22} = z = 0\ ℧$$

Now, we can redraw circuit as,



(ii) For maximum power transfer, $Z_L = Z_{th}$

***Z**$_{th}$*: Replacing the independent voltage source V_1 with a short-circuit and connecting voltage source V_A across the load terminals to calculate the Thevenin equivalent impedance,



$\because$ $$I_A = I_2 = -10I_1 \quad \text{...(i)}$$

On applying KVL in loop 1, we get

$$1000I_1 + 0.01V_2 = 0$$
$$1000I_1 = -0.01V_2$$

From equation (i), we get

$$I_1 = \frac{-I_A}{10}$$

We get, $$-0.01V_A = -\frac{1000}{10}I_A \quad [\because V_2 = V_A]$$

$$\frac{V_A}{I_A} = Z_{th} = \frac{+1000}{10\times 1}\times 100$$

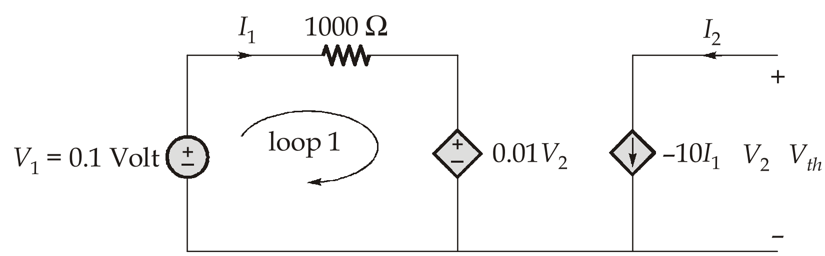
$$Z_{th} = 10\ \text{k}\Omega$$

Hence,

for maximum power transfer, $Z_L = Z_{th} = 10\ \text{k}\Omega$

(iii) Maximum power transfer to the load for $V_1 = 0.1$ V:

V_{th}:



As $I_2 = 0 = 10I_1 \quad \Rightarrow \quad I_1 = 0$

Hence, no current flow in the loop 1. It implies

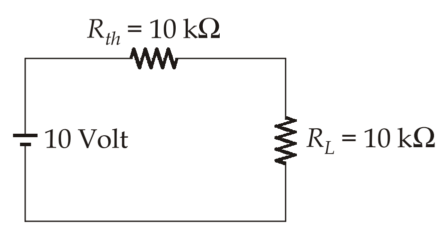
$$V_1 = 0.01\ V_2 = 0.01V_{th}$$

$$V_{th} = 100\ V_1$$

For $V_1 = 0.1$ V

$$V_{th} = 10\ \text{V}$$

Thus, Thevenin equivalent circuit can be drawn as below,



$$P_{L\max} = \frac{V_{th}^2}{4R_L}$$

$$P_{L\max} = \frac{100}{4\times10\times1000}$$

$$P_{L\max} = 2.5\ \text{mW}$$

Q.6 (b) (i) Solution:

The solution can be split into two portions

$$y(t) = y_s(t) + y_n(t)$$

where, $y_s(t)$ = steady state response,

$y_n(t)$ = normal response

∴ To calculate the steady-state response, we will assume initial input to be zero.

$$\therefore \quad G(s) = \frac{1}{s+3}$$

$$\therefore \quad \frac{Y(s)}{X(s)} = \frac{1}{s+3}$$

$$(s+3)Y(s) = X(s)$$

$$sY(s) + 3Y(s) = X(s)$$

Now, given input is a step response

$$\therefore \quad sY(s) + 3Y(s) = \frac{1}{s}$$

$$\therefore \quad Y(s) = \frac{1}{s(s+3)}$$

$$Y(s) = \frac{A}{s} + \frac{B}{s+3} = \frac{1/3}{s} + \frac{-1/3}{s+3}$$

Applying, inverse Laplace transform, we get

$$y_s(t) = \frac{1}{3}u(t) - \frac{1}{3}e^{-3t}u(t)$$

Now, to calculate the natural response, we assume that the input $x(t) = 0$

$$sy(s) - y(0) + 3y(s) = 0$$

$$(s+3)Y(s) = y(0)$$

$$y(s) = \frac{y(0)}{s+3}$$

Given $y(0) = 3$

$$\therefore \quad Y(s) = \frac{3}{s+3}$$

Taking the inverse Laplace transform,

we get $\quad y_n(t) = 3e^{-3t}\,u(t)$

$\therefore$ Total response,

$$y(t) = y_s(t) + y_n(t)$$

$$\therefore \quad y(t) = 3e^{-3t}u(t) + \frac{1}{3}u(t) - \frac{1}{3}e^{-3t}u(t)$$

$$\therefore \quad y(t) = 0.4659 \simeq 0.47$$

Q.6 (b) (ii) Solution:

$$f(t) = 1 + 2\cos(\pi t) + 3\sin\left(\frac{2\pi}{3}t\right) + 4\cos\left(\frac{\pi}{2}t + \frac{\pi}{4}\right)$$

$$\omega_1 = \pi$$

$$\omega_2 = \frac{2\pi}{3}$$

$$\omega_3 = \frac{\pi}{2}$$

$$\omega_0 = \text{GCD}\left(\pi, \frac{2\pi}{3}, \frac{\pi}{2}\right) = \frac{\pi}{6}$$

Fundamental period, $$N = \frac{2\pi}{\omega_o} = \frac{2\pi}{(\pi/6)} = 12\,\text{sec}$$

Q.6 (b) (iii) Solution:

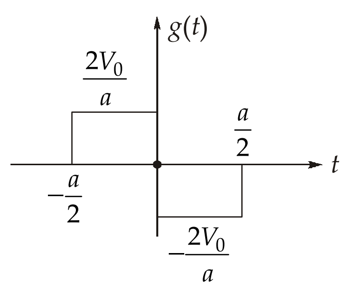
$$\omega_1 = 100$$
$$\omega_2 = 300$$
$$\omega_3 = 500$$
$$\text{H.C.F. of } (\omega_1, \omega_2 \text{ and } \omega_3) = \text{H.C.F. } (100, 300, 500)$$
$$\omega = 100 \text{ rad/sec.}$$

Q.6 (c) (i) Solution:

Let $$g(t) = \frac{d}{dt} f(t)$$

$$\Updownarrow \text{F.T.}$$

$$G(j\omega) = (-j\omega)F(j\omega)$$



$$g(t) = \frac{2V_o}{a}\text{rect}\left[\frac{2t}{a} + \frac{a}{4}\right] - \frac{2V_o}{a}\text{rect}\left[\frac{2t}{a} - \frac{a}{4}\right]$$

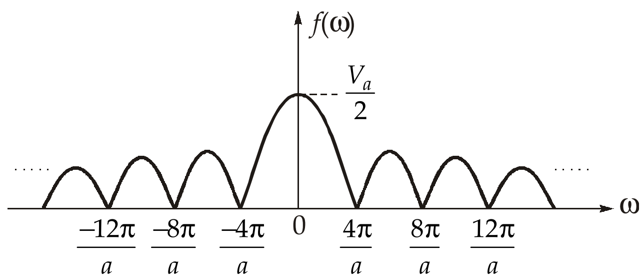
$$\Updownarrow$$

$$G(j\omega) = \frac{2V_o}{a} \cdot \frac{a}{2} Sa\left(\frac{\omega a}{4}\right) e^{j\frac{\omega a}{4}} - \frac{2V_o}{a} \cdot \frac{a}{2} Sa\left(\frac{\omega a}{4}\right) e^{-j\frac{\omega a}{4}}$$

$$F(j\omega) = \frac{1}{(-j\omega)} \times V_o Sa\left(\frac{a\omega}{4}\right)\left[\frac{e^{\frac{j\omega a}{4}} - e^{\frac{-j\omega a}{4}}}{2j}\right] \times 2j$$

$$= \frac{2V_o}{\omega} Sa\left(\frac{a\omega}{4}\right)\sin\left(\frac{a\omega}{4}\right) \times \frac{\left(\frac{a\omega}{4}\right)}{\left(\frac{a\omega}{4}\right)}$$

$$F(j\omega) = \frac{V_o a}{2} Sa^2\left(\frac{a\omega}{4}\right)$$



Q.6 (c) (ii) Solution:

Duality property of the Fourier Transform state that,

If, $$x(t) \xleftrightarrow{FT} X(f)$$

then, $$X(t) \xleftrightarrow{FT} x(-f)$$

Now, we know the standard Fourier transform pair

$$e^{-at}u(t) \xleftrightarrow{FT} \frac{1}{a + j2\pi f}$$

∴ Using the duality property,

$$\frac{1}{a + j2\pi t} \xleftrightarrow{FT} e^{af} u(-f)$$

Put, $a = 1$

$$\frac{1}{1 + j2\pi t} \longleftrightarrow e^{f} u(-f)$$

Q.7 (a) Solution:

From the given description in question, we get

$$P_{CD} = P_{AB}$$

$$I_{CD}^2 R_{CD\text{ equivalent}} = I_{AB}^2 R_{AB\text{ equivalent}}$$

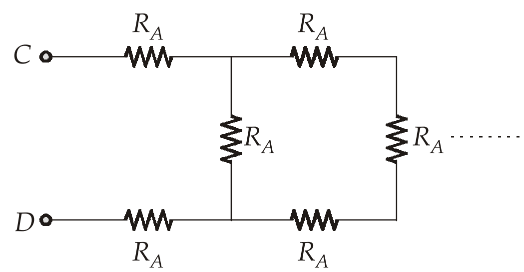
∵ $$I = \frac{V}{R}$$

$$\frac{V_{CD}^2}{R_{CD\text{ equivalent}}} = \frac{V_{AB}^2}{R_{AB\text{ equivalent}}}$$

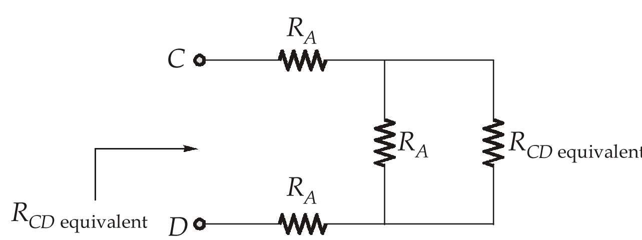
$\because$ $V_{CD} = V_{AB} = 10\text{ V}$

$\therefore$ $R_{CD\text{ equivalent}} = R_{AB\text{ equivalent}}$

Now, Equivalent resistance across CD is given as



or



$$R_{CD\text{ equivalent}} = 2R_A + (R_A \parallel R_{CD\text{ equivalent}})$$

$$R_{CD\text{ equivalent}} = 2R_A + \frac{R_A \cdot R_{CD\text{ equivalent}}}{R_A + R_{CD\text{ equivalent}}}$$

$$R_A R_{CD\text{equivalent}} + R_{CD\text{ equivalent}}^2 = 2R_A^2 + 2R_A \cdot R_{CD\text{equivalent}} + R_A \cdot R_{CD\text{equivalent}}$$

$$R_{CD\text{equivalent}}^2 - 2R_A \cdot R_{CD\text{equivalent}} - 2R_A^2 = 0$$

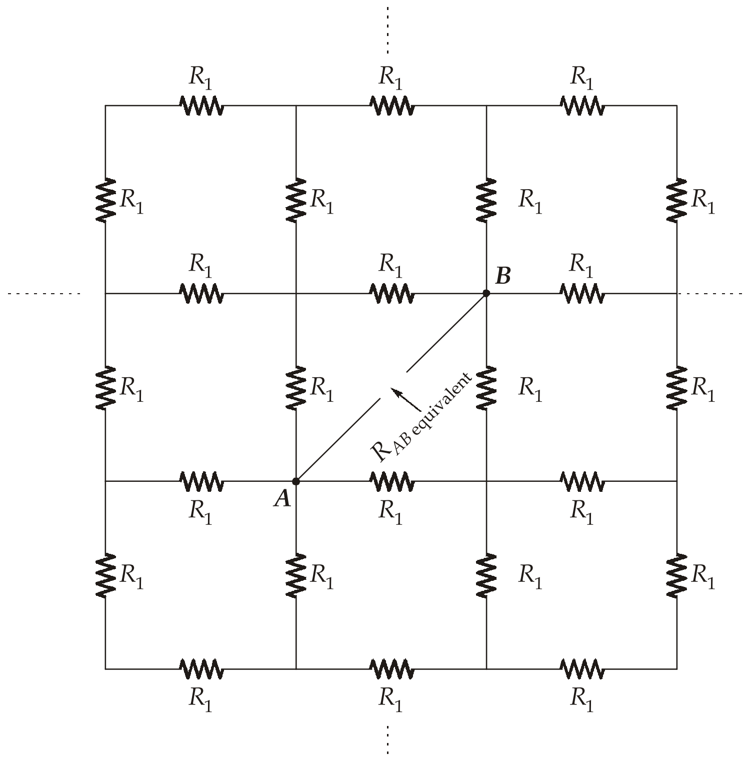
$$R_{CD\text{ equivalent}} = \frac{2R_A \pm \sqrt{4R_A^2 + 8R_A^2}}{2}$$

$$R_{CD\text{ equivalent}} = R_A \pm \sqrt{R_A^2 + 2R_A^2}$$

Since R_A cannot be negative, we get

$$R_{CD\text{ equivalent}} = (R_A + \sqrt{3}R_A)\,\Omega \quad \text{...(i)}$$

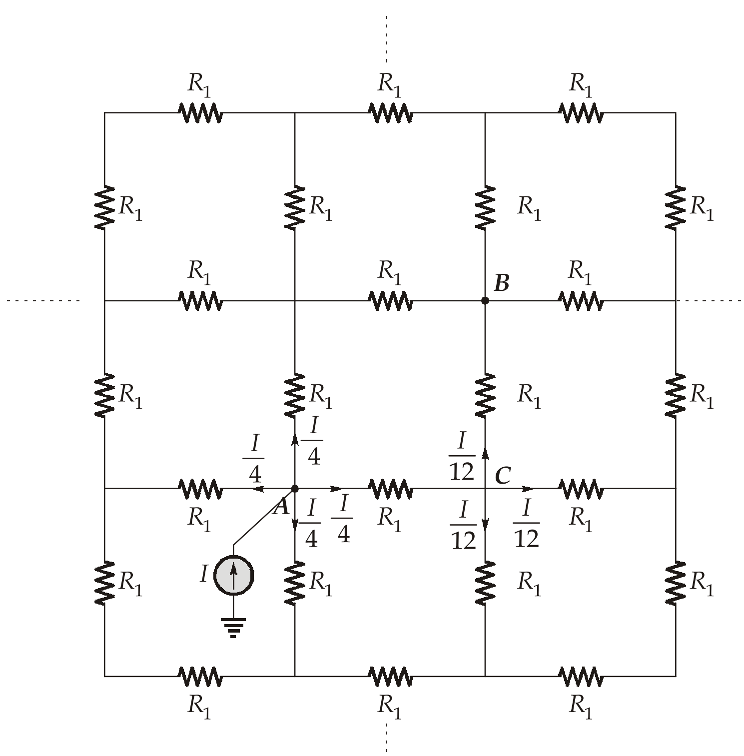
Now, equivalent resistance across A-B in network (ii) is calculated as,



Network (ii)

$R_{AB\ \text{equivalent}}$:

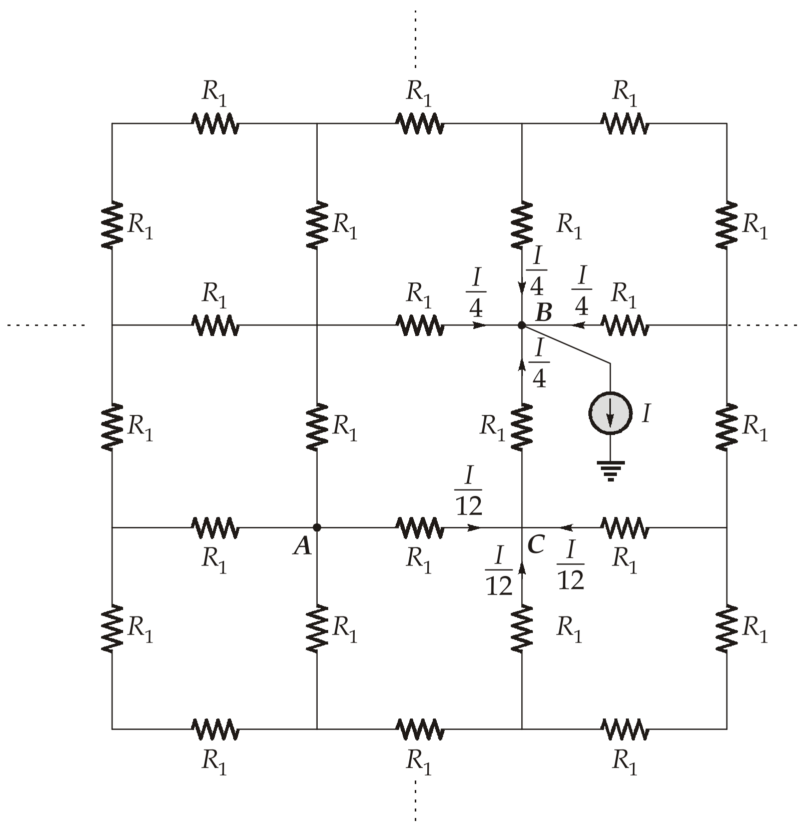
Case 1:



By KVL [$ACBA$]

$$V'_{AB} = R_1\frac{I}{4} + R_1\frac{I}{12} = I\left[\frac{R_1}{3}\right]$$

Case 2:



By KVL [$ACBA$]

$$V''_{AB} = R_1\frac{I}{4} + R_1\frac{I}{12} = I\left[\frac{R_1}{3}\right]$$

By super-position,

$$V_{AB} = V'_{AB} + V''_{AB} = \frac{2}{3}R_1 I$$

$$R_{AB\,\text{equivalent}} = \frac{2R_1}{3} \quad \text{...(ii)}$$

$$\because \quad R_{CD\,\text{equivalent}} = R_{AB\,\text{equivalent}}$$

$$R_A + \sqrt{3}R_A = \frac{2R_1}{3}$$

$$R_1 = \left[\frac{3+3\sqrt{3}}{2}\right]R_A$$

$$R_1 = 4.10\, R_A \quad \text{or}$$
$$R_A = 0.244\, R_1$$

Now, Power delivered by source for $R_A = 10\ \Omega$ is

$$P_{\text{delivered}} = \frac{V^2}{R_{AB\text{equivalent}}}$$

where $$R_{AB\text{ equivalent}} = \frac{2R_1}{3}$$

$$R_{AB\text{ equivalent}} = \frac{2(4.10R_A)}{3} = \frac{2\times 4.10\times 10}{3} = \frac{82}{3}\ \Omega$$

$$P_{\text{delivered}} = \frac{(10)^2\times 3}{82}$$

$$P_{\text{delivered}} = 3.66 \text{ Watt}$$

Q.7 (b) Solution:

Given : From fact (2)

$$F^{-1}\{(1+j\omega)X(j\omega)\} = Ae^{-2t}u(t)$$

Taking fourier transform on both sides,

$$(1+j\omega)X(j\omega) = \frac{A}{2+j\omega}$$

$$X(j\omega) = \frac{A}{(1+j\omega)(2+j\omega)}$$

Taking inverse fourier transform,

$$X(j\omega) = \frac{A_1}{1+j\omega} + \frac{A_2}{1+j\omega}$$

where, $$A_1 = \left.\frac{A}{2+j\omega}\right|_{j\omega=-1} \Rightarrow A_1 = A$$

$$A_2 = \left.\frac{A}{1+j\omega}\right|_{j\omega=-2} \Rightarrow A_2 = -A$$

$$X(j\omega) = A\left[\frac{1}{1+j\omega} - \frac{1}{2+j\omega}\right]$$

Taking inverse fourier transform,

$$x(t) = Ae^{-t}u(t) - Ae^{-2t}u(t) \quad \text{...(1)}$$

Using fact (3),

$$\int_{-\infty}^{\infty} |X(j\omega)|^2 = 2\pi$$

From Parseval's theorem,

$$\int_{-\infty}^{\infty} |X(j\omega)|^2 = 2\pi \int_{-\infty}^{\infty} |x(t)|^2 \, dt$$

i.e.,

$$\int_{-\infty}^{\infty} |x(t)|^2 \, dt = 1$$

$$\int_{-\infty}^{\infty} [Ae^{-t}u(t) - Ae^{-2t}u(t)]^2 \, dt = 1$$

$$A^2 \int_{0}^{\infty} (e^{-2t} - 2e^{-3t} + e^{-4t}) dt = 1$$

$$A^2 \left[\frac{e^{-2t}}{(-2)} - \frac{2e^{-3t}}{(-3)} + \frac{e^{-4t}}{(-4)} \right]_0^{\infty} = 1$$

$$A^2 \left[\frac{1}{2} - \frac{2}{3} + \frac{1}{4} \right] = 1$$

$$\frac{A^2}{12} = 1$$

$$A = \pm\sqrt{12}$$

Since, $x(t)$ is a non-negaitve.

So,

$$A = +\sqrt{12}$$

$$x(t) = \left[\sqrt{12}e^{-t} - \sqrt{12}e^{-2t} \right] u(t)$$

Q.7 (c) (i) Solution:

Given that,

$$h_1(t) = 2\delta(t + 2) - 3\delta(t + 1)$$

$$h_2(t) = \delta(t - 2)$$

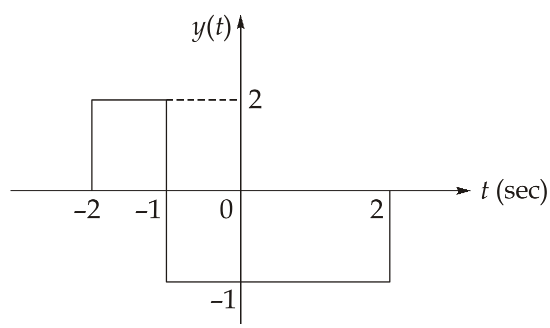
Overall impulse response is,

$$h(t) = h_1(t) + h_2(t)$$
$$= 2\delta(t+2) - 3\delta(t+1) + \delta(t-2)$$

If input, $x(t) = u(t)$, then the output will be,

$$y(t) = x(t) * h(t)$$
$$= u(t) * [2\delta(t+2) - 3\delta(t+1) + \delta(t-2)]$$
$$= 2u(t+2) - 3u(t+1) + u(t-2)$$

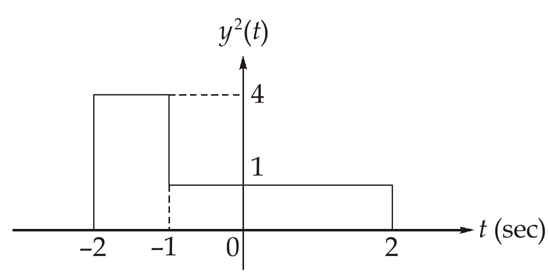
By plotting $y(t)$, we get,



The energy of $y(t)$ can be given as,

$$E_y = \int_{-\infty}^{\infty} y^2(t)\,dt$$

By plotting $y^2(t)$, we get,



$$E_y = \text{Area under the plot of } y^2(t)$$
$$= (4 \times 1) + (3 \times 1) = 7\text{ J}$$

Q.7 (c) (ii) Solution:

1. $x(t)$ is real and even so a_k is also real and even $a_k = a_{-k}$
2. Average of $x(t)$ is 2 i.e., $a_0 = 2$.
3. $x(t) \rightarrow a_k = k$ $\quad 1 \le k \le 3 \quad a_1 = a_{-1} = 1$

$0k > 3 \quad a_2 = a_{-2} = 2$

$a_3 = a_{-3} = 3$

4. $T_0 = 6$

Parseval's Power Theorem

$$\frac{1}{T}\int_0^T \left|x(t)^2\right| dt = \sum_{n=-\infty}^{+\infty} |a_k|^2$$

$$P_{x(t)} = \sum_{n=-\infty}^{+\infty} |a_k|^2$$

$$= |a_{-3}|^2 + |a_{-2}|^2 + |a_{-1}|^2 + |a_0|^2 + |a_1|^2 + |a_2|^2 + |a_3|^2$$

$$= 2|a_1|^2 + 2|a_2|^2 + 2|a_3|^2 + |a_0|^2$$

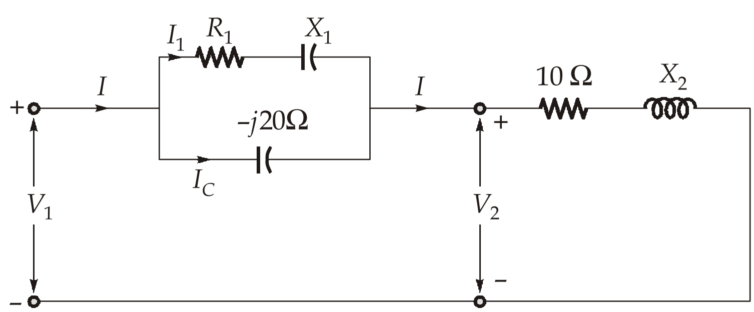
$$= 2 \times 1^2 + 2 \times (2)^2 + 2(3)^2 + (2)^2$$

$$= 2 + 8 + 18 + 4$$

$$P_{x(t)} = 32$$

Q.8 (a) Solution:

The given circuit is,

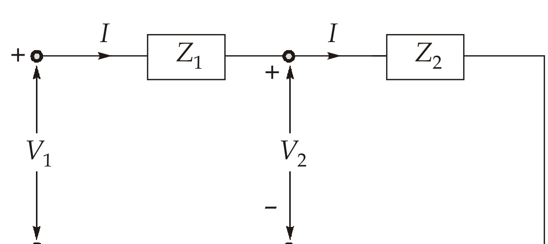


Given: $|V_1| = 200$ V and $V_2 = 200 \angle 0°$ V

also, $|I| = 12$ A

$P_T = 1.8$ kW

Now, the circuit can be redrawn as



where, $\dfrac{1}{Z_1} = \dfrac{1}{Z} + \dfrac{1}{-j20\Omega}$ with $Z = R_1 - jX_1$

and, $Z_2 = R_2 + jX_2$

$= 10 + jX_2 = Z_2\angle\theta_2$

$\therefore \quad I = \frac{V_2}{Z_2} = \frac{200\angle 0°}{Z_2\angle\theta_2}$

Thus, $|I| = \frac{200}{Z_2} = 12$

Hence, $Z_2 = \frac{200}{12} = 16.67\Omega$

$\because \quad |Z_2| = \sqrt{10^2 + X_2^2}$

$\therefore \quad (16.67)^2 = 100 + X_2^2$

or $X_2^2 = 177.77$

or $X_2 = \sqrt{177.77} = 13.33\Omega$

and $\theta_2 = \tan^{-1}\left(\frac{X_2}{10}\right) = \tan^{-1}\left(\frac{13.33}{10}\right) = 53.13°$

$\theta_2 = 53.13°$

Thus, angle between I and V_2 is 53.13°

$\therefore \quad I = 12\angle -53.13° A$

Now, $P_T = V_1 \times I \cos\theta_T$

where, $\cos\theta_T = \frac{P_T}{V_1 \times I} = \frac{1800}{200 \times 12}$ (given)

$\cos\theta_T = 0.75$

or $\theta_T = 41.4°$

$\because$ This is the angle between current I and voltage V_1

$\therefore \quad V_1 = 200\angle(-53.13 + 41.4)°$

or $V_1 = 200\angle -11.73° \text{ V}$

and $V_{z1} = V_1 - V_2 = 200\angle -11.73° - 200\angle 0°$

$= 195.82 - 40.659j - 200$

$= -4.18 - 40.659j$

$= 40.87\angle -95.86°$

Current through capacitor ($-j20\ \Omega$) is

$$I_C = \frac{V_{z1}}{jX_c} = \frac{40.87\angle -95.86°}{20\angle -90°} = 2.0436\angle -5.86° \text{ A}$$

Now, current through R_1 and X_1 are

$$I_1 = I - I_C = 12\angle -53.13° - 2.0436\angle -5.86°$$

$$I_1 = 10.718\angle{-61.18°}\text{ A}$$

$$\therefore \quad Z_1 = \frac{V_{z1}}{I_1} = \frac{40.87\angle -95.86°}{10.718\angle -61.18°}$$

$$= 3.813\angle{-34.68°}$$

$$= 3.135 - 2.169j = R_1 - jX_1$$

$$\therefore \quad R_1 = 3.135\ \Omega$$

$$X_1 = 2.169\ \Omega$$

Q.8 (b) (i) Solution:

1. Taking the Laplace transform, we have

$$s^2Y(s) + sY(s) - 2Y(s) = X(s)$$

or
$$(s^2 + s - 2)Y(s) = X(s)$$

Hence, the system function $H(s)$ is

$$H(s) = \frac{Y(s)}{X(s)} = \frac{1}{s^2+s-2} = \frac{1}{(s+2)(s-1)}$$

2. Using partial fraction expansions, we get

$$H(s) = \frac{1}{(s+2)(s-1)} = -\frac{1}{3}\frac{1}{s+2} + \frac{1}{3}\frac{1}{s-1}$$

(1) If the system is causal, then $h(t)$ is causal (that is, a right-sided signal) and the ROC of $H(s)$ is Re(s) > 1. Then, we get

$$h(t) = -\frac{1}{3}(e^{-2t} - e^{t})u(t)$$

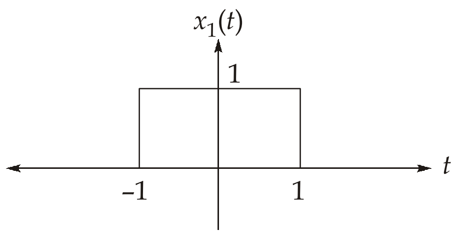
(2) If the system is stable, then the ROC of $H(s)$ must contain the $j\omega$-axis. Consequently, the ROC of $H(s)$ is $-2 < \text{Re}(s) < 1$. Thus, $h(t)$ is two-sided and we get

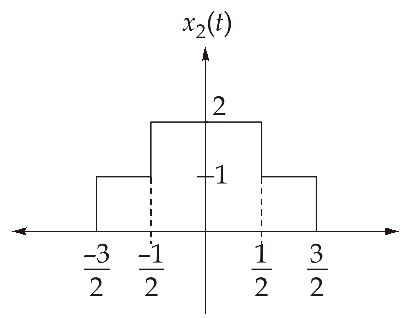
$$h(t) = -\frac{1}{3}e^{-2t}u(t) - \frac{1}{3}e^{t}u(-t)$$

(3) If the system is neither causal nor stable, then the ROC of $H(s)$ is $\text{Re}(s) < -2$. Then, $h(t)$ is non-causal (that is, a left-sided signal) and we get

$$h(t) = \frac{1}{3}e^{-2t}u(-t) - \frac{1}{3}e^{t}u(-t)$$

Q.8 (b) (ii) Solution:

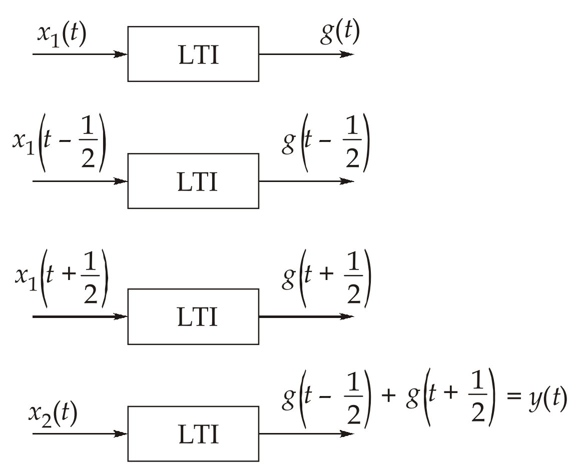




We can write,

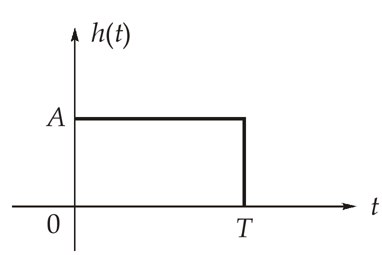
$$x_2(t) = x_1\left(t-\frac{1}{2}\right)+x_1\left(t+\frac{1}{2}\right)$$

Since the system is LTI, we have



$$y(0) = g\left(-\frac{1}{2}\right)+g\left(\frac{1}{2}\right) = 3.25 + 3.25 = 6.50$$

Q.8 (c) Solution:



By using convolution property,

$$y_1(t) = \int_{-\infty}^{\infty} x_1(\tau)h(t-\tau)d\tau$$

From the given first fact,

at $$t = 5$$

$$y_1(5) = \int_{-\infty}^{\infty} x_1(\tau)h(5-\tau)d\tau$$

$$y_1(5) = A\int_{5-T}^{5} x_1(\tau)d\tau = 0$$

if the lower limit is equal to 1, then the area of the triangle between $\tau = 1$ and $\tau = 3$ is 2 and cancels the area of the rectangle between $\tau = 4$ and $\tau = 5$.

Hence, the value for T should be 4.

$$y_2(t) = \int_{-\infty}^{\infty} x_2(\tau)h(t-\tau)d\tau = A\int_{t-T}^{t} x_2(\tau)d\tau$$

$$y_2(t)\,|_{t=9} = A\int_{5}^{9} x_2(\tau)d\tau \quad \text{(given } t = 9)$$

from the second fact, we have

$$y_2(t)\,|_{t=9} = 9 = A\int_{5}^{9} x_2(\tau)d\tau = A\int_{5}^{9}\sin\left(\frac{\pi\tau}{3}\right)d\tau$$

$$= -\frac{A}{\pi/3}\cos\left(\frac{\pi\tau}{3}\right)\Bigg]_5^9$$

$$9 = \frac{9A}{2\pi}$$

$$\therefore \quad A = 2\pi$$

$\therefore$ The value of $A \times T = 2\pi \times 4 = 8\pi = 25.13$

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