RPSC AEn-2024 Main Test Series

ELECTRICAL ENGINEERING | **Test 8**

Test Mode : • Offline • Online

Subjects : Electronics Communication + Microprocessor System and Computer

DETAILED EXPLANATIONS

PART-A

1. Solution:

Rectification is the process of converting an alternating (AC) voltage into one that is limited to one polarity.

2. Solution:

MOSFETs exhibit excellent noise immunity, making them suitable for high-performance analog and digital circuits. The insulating oxide layer between Gate and channel acts as a barrier against external electrical noise, resulting in enhanced signal integrity and reduced susceptibility to interference.

3. Solution:

Machine Language: the binary medium of communication with a computer through a designed set of instructions specific to each computer.

4. Solution:

Compiler is a program that translates English like words of a high-level language into the machine language of a computer. A compiler reads a given program, called a source code, in its entirety, and then translates the program into the machine language which is called an object code. (Ex. *C*, *C++*).

5. Solution:

Interpreter is a program that translates the English-like statements of a high-level language into the machine language of a computer. An interpreter translates one statement at a time from a source code to an object code. (Ex. BASIC)

6. Solution:

Cache memory is a random access memory that a computer microprocessor can access more quickly than a regular RAM. This memory is typically integrated directly with the CPU chip or placed on a separate chip with separate bus interconnect with CPU.

7. Solution:

'READY' is used by the microprocessor to sense whether a peripheral device is ready for data transfer or not. If not the processor waits, for synchronize with (slow) peripherals.

8. Solution:

A \ BC	00	01	11	10
0	1	0	0	1
1	1	1	1	1

$$F = A + \overline{C}$$

9. Solution:

- A circuit which cutoff voltage above or below are both at specified level is called clipper.
- A clamper is a circuit which adds a dc level to an ac signal.

10. Solution:

$$f_{IF} = 455 \text{ kHz}$$
$$f_c = 1000 \text{ kHz}$$
$$\text{we know that image frequency} = f_c + 2f_{IF}$$
$$= 1000 + 2 \times 455 = 1910 \text{ kHz}$$

PART-B

11. Solution:

An ideal operational amplifier has the following characteristics:

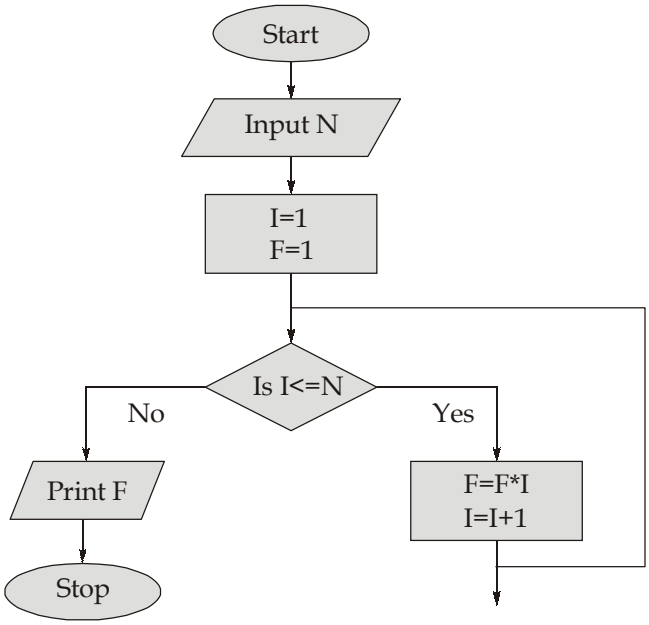
- Infinite open-loop gain.
- Infinite input impedance.
- Zero output impedance.

- Infinite bandwidth.
- Zero input offset voltage.
- Zero noise.
- Infinite common, mode rejection ratio.
- Infinite power supply rejection ratio.

12. Solution:

- Silicon forms a thin layer of SiO_2 on its surface, which is a good insulator and easy to process.
- Silicon can withstand temperatures up to 150°C. While germanium wafers break or melt at 70°C.
- Silicon has a larger band gap (1.12 eV) than germanium (0.7 eV). This means that at the same temperature, silicon generates fewer thermal pairs than germanium.
- Silicon atoms are more stable than germanium atoms at high temperatures.
- Silicon is more abundant than germanium.

13. Solution:



14. Solution:

There are five flags in 8085 microprocessor. These are Sign Flag [*S*], Zero Flag [*Z*], Auxiliary Carry Flag [*AY*], Parity Flag [*P*] and Carry Flag [*CY*].

The microprocessor uses these flags to test data conditions.

These flags have critical importance in decision making process of the microprocessor.

The condition set or reset of the flags are tested through software instruction. For example, the instruction *JC* (Jump on Carry) is implemented to change the sequence of a program when *CY* flag is set.

These flags are affected by execution of an arithmetic or logical operation, data copy instructions do not affect any flags. Its working is as below.

Zero Flag: The zero flag is set to 1 when result is zero otherwise it is reset.

CY (Carry Flag): If an arithmetic operation results in a carry, the *CY* flag is set, otherwise it is reset.

Sign Flag (*S*): The sign flag is set if bit D_7 of the result = 1 otherwise it is reset.

Parity Flag (*P*): If the reset has even on. of 1s, the flat is set, for an odd no. of 1s the flag is reset.

AC (Auxiliary Carry): In an arithmetic operation, when a carry is generated by digit D_3 and passed to digit D_4 the AC flag is set otherwise reset. This flag is used for *BCD* operations, there is no jump instruction associated with this flag.

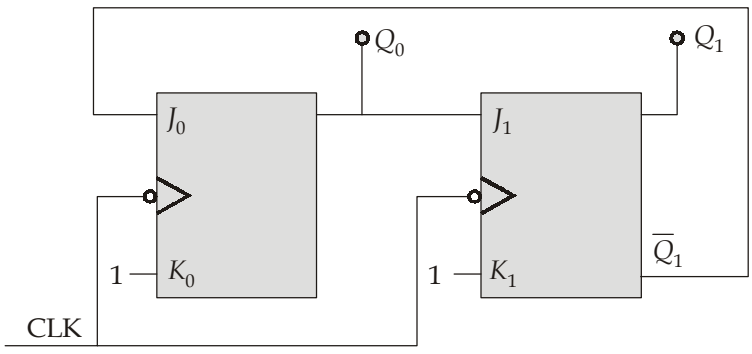
15. Solution:

$$F(A, B, C) = A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + B\overline{C}$$

$$= \Sigma(1, 2, 4, 6)$$

A \ BC	00	01	11	10
0		1		1
1	1			1

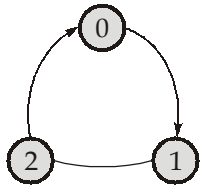
16. Solution:



2-Stage synchronous counter

Present state						next stage	
Q_1	Q_0	J_1	K_1	J_0	K_0	Q_1	Q_0
0	0	0	1	1	1	0	1
0	1	1	1	1	1	1	0
1	0	0	1	0	1	0	0

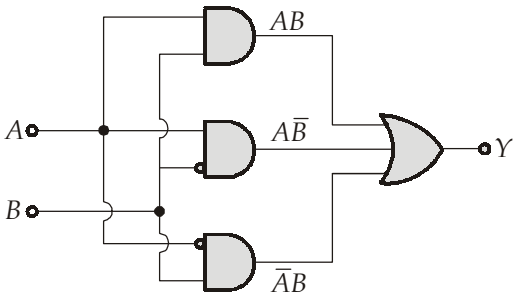
So, state diagram of the counter



From this, our synchronous counter is 3 : 1 counter.

$\therefore$ it has 3-states.

17. Solution:



The expression for Y is, $Y = AB + A\overline{B} + \overline{A}B = A + B$

18. Solution:

$$P_C = \frac{A^2}{2\times 50} = 40 \times 1000$$

$\Rightarrow$ $A = 2$ kV

$m_p = \mu A = (0.707) \times 2 = 1.414$ kV

$\therefore$ Peak amplitude of the output $= A + m_p = 3.414$ kV

PART-C

19. Solution:

(i) $F = x \odot y + \overline{y}\, z$

$F = x \odot y + \overline{y}\, z$

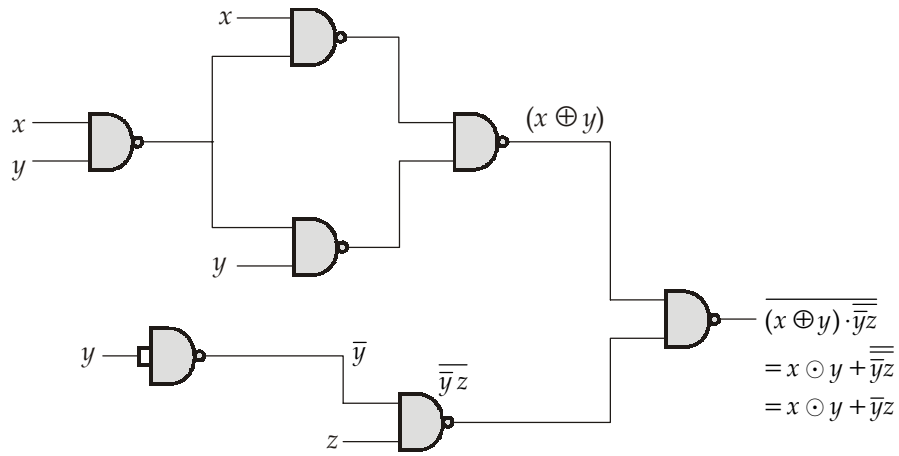
$$\overline{F} = \overline{x \odot y + \overline{y}\, z}$$

$$\overline{F} = x \oplus y + \overline{y}\, z$$

$$F = \underbrace{\overline{x \oplus y}}_{A} + \underbrace{\overline{\overline{y}\, z}}_{B} = \overline{A \cdot B}$$

$$A = x \oplus y$$

$$B = \overline{\overline{y}\, z}$$



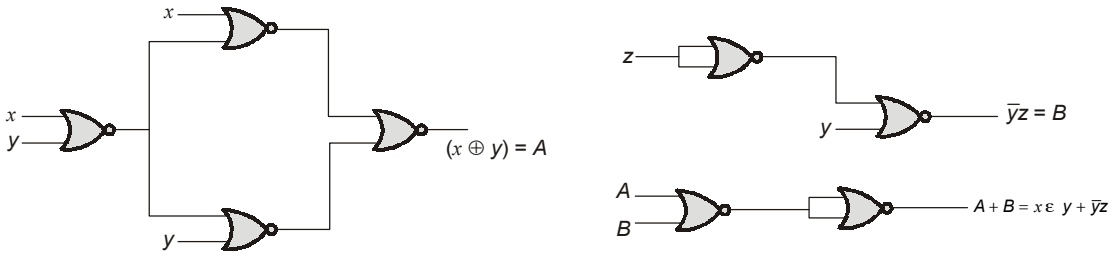
(ii) Using NOR gates:

$$F = \overline{xy} + xy + \overline{y}z$$

$$F = x \odot y + \overline{y}z$$

$$= A + bA + B\left(A = x \odot y, B = \overline{y}z\right)$$

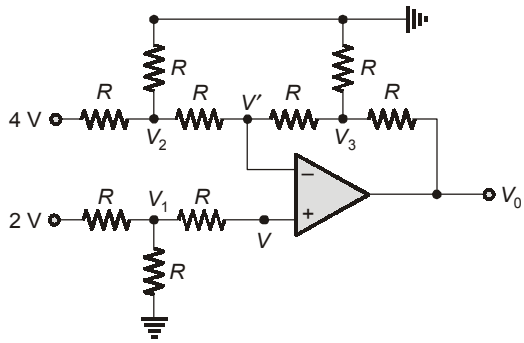
$$\overline{F} = \overline{x \odot y}.\overline{\overline{y}\, z}$$



(iii) ∵ NAND = AND + NOT → So replace all NAND gates in (i) part by AND + NOT

(iv) ∵ NOR = OR + NOT → So replace all NOR gates by OR + NOT.

20. Solution:



Applying KCL for V_1,

$$\frac{V_1 - 2}{R} + \frac{V_1}{R} + \frac{V_1 - V}{R} = 0$$

$$\Rightarrow \quad 3V_1 = 2 + V$$

Since, no current flows into the op-amp,

$$V_1 = V$$

$$\therefore \quad 2V = 2$$

$$\Rightarrow \quad V = 1\text{ V} \qquad \text{...(1)}$$

Also, due to internal short, $V' = V = 1$ V

Applying KCL for V_2,

$$\frac{V_2 - 4}{R} + \frac{V_2}{R} + \frac{V_2 - 1}{R} = 0$$

$$3V_2 = 5$$

$$\Rightarrow \quad V_2 = \frac{5}{3}\text{ V} \qquad \text{...(2)}$$

Applying KCL at node voltage V',

$$\frac{V' - V_2}{R} + \frac{V' - V_3}{R} = 0$$

$$2V' = V_2 + V_3$$

$$\Rightarrow \quad V_3 = 2 - \frac{5}{3}$$

$$V_3 = \frac{1}{3}\text{ V} \qquad \text{...(3)}$$

Now, applying KCL and node V_3,

$$\frac{V_3 - 1}{R} + \frac{V_3}{R} + \frac{V_3 - V_0}{R} = 0$$

$$V_o = 3V_3 - 1 = 0\text{ V}$$

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