



MADE EASY

Leading Institute for ESE, GATE & PSUs

ESE 2025 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

Electronics & Telecommunication Engineering

Test-6 : Advanced Electronics + Computer Organization and Architecture +

Advanced Communication [All topics]

Name :

Roll No :

Test Centres

Delhi ☐ Bhopal ☐ Jaipur ☐ Pune ☐
Kolkata ☐ Hyderabad ☐

Student's Signature

Instructions for Candidates

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. There are Eight questions divided in TWO sections.
3. Candidate has to attempt FIVE questions in all in English only.
4. Question no. 1 and 5 are compulsory and out of the remaining THREE are to be attempted choosing at least ONE question from each section.
5. Use only black/blue pen.
6. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
7. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
8. There are few rough work sheets at the end of this booklet. Strike off these pages after completion of the examination.

FOR OFFICE USE

Question No.	Marks Obtained
Section-A	
Q.1	—
Q.2	—
Q.3	—
Q.4	33
Section-B	
Q.5	40
Q.6	24
Q.7	—
Q.8	45
Total Marks Obtained	142

Signature of Evaluator

Cross Checked by

Checking : A.M.

* Avoid Calculation mistakes.
* You can perform better.

IMPORTANT INSTRUCTIONS

CANDIDATES SHOULD READ THE UNDERMENTIONED INSTRUCTIONS CAREFULLY. VIOLATION OF ANY OF THE INSTRUCTIONS MAY LEAD TO PENALTY.

DONT'S

1. Do not write your name or registration number anywhere inside this Question-cum-Answer Booklet (QCAB).
2. Do not write anything other than the actual answers to the questions anywhere inside your QCAB.
3. Do not tear off any leaves from your QCAB, if you find any page missing do not fail to notify the supervisor/invigilator.
4. Do not leave behind your QCAB on your table unattended, it should be handed over to the invigilator after conclusion of the exam.

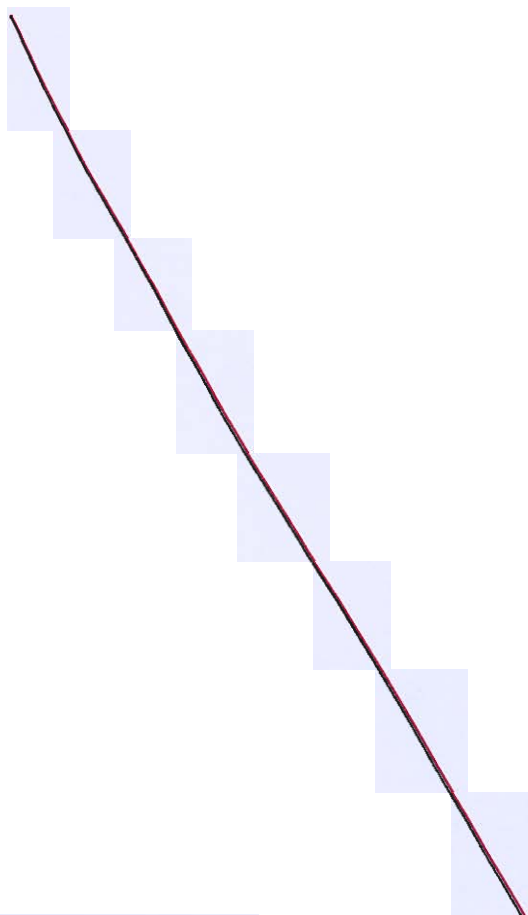
DO'S

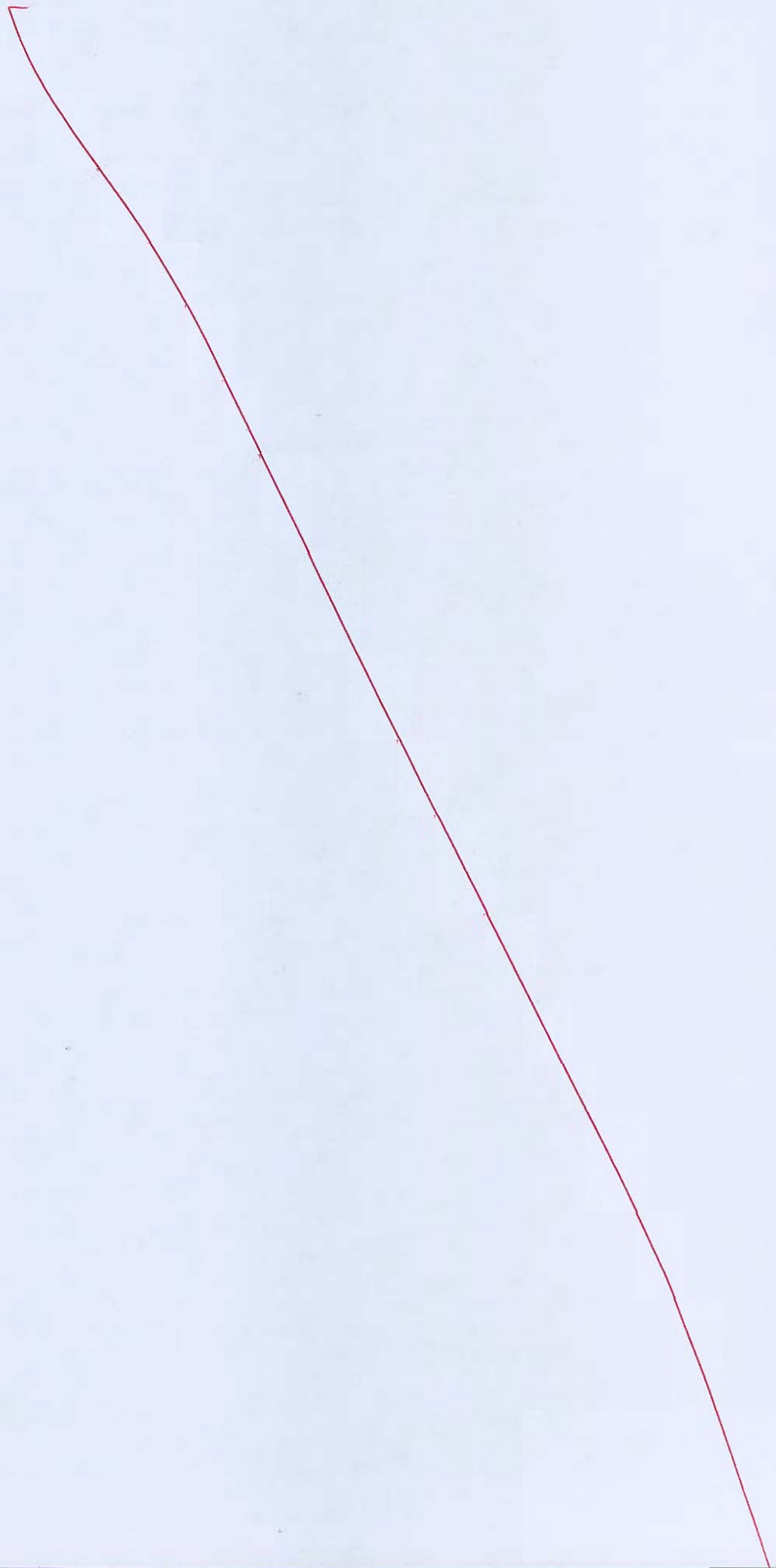
1. Read the Instructions on the cover page and strictly follow them.
2. Write your registration number and other particulars, in the space provided on the cover of QCAB.
3. Write legibly and neatly.
4. For rough notes or calculation, the last two blank pages of this booklet should be used. The rough notes should be crossed through afterwards.
5. If you wish to cancel any work, draw your pen through it or write "Cancelled" across it, otherwise it may be evaluated.
6. Handover your QCAB personally to the invigilator before leaving the examination hall.

**Section A : Advanced Electronics + Computer Organization and Architecture
+ Advanced Communication**

- (a) A $0.6\text{ }\mu\text{m}$ layer of silicon dioxide on a Si substrate to be etched down to the Si substrate. Assume that the normal oxide etch rate is $0.4\text{ }\mu\text{m}/\text{minute}$. There is a $\pm 4\%$ variation in the oxide thickness and a $\pm 5\%$ variation in the oxide etch rate.
- (i) How much overetch is required (in % time) in order to ensure that all the oxide is etched?
- (ii) If the overetch obtained in part (i) is used, then what etch selectivity of the oxide with respect to the Si is required so that a maximum of 0.5 nm of Si is etched?

[12 marks]





- (b) Write a C-program to print first hundred Fibonacci numbers $\text{fib}(i)$ given by,
 $\text{fib}(i) = \text{fib}(i - 1) + \text{fib}(i - 2)$
It is given that, $\text{fib}(0) = \text{fib}(1) = 1$

[12 marks]

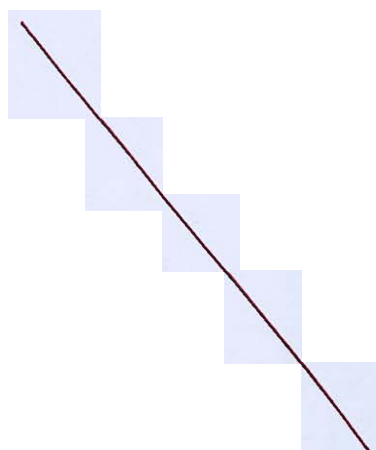
- Q.1 (c) In the transmission and reception of signals to and from moving vehicles, the transmitted signal frequency is shifted in direct proportion to the speed of the vehicle. The so-called Doppler frequency shift imparted to a signal that is received in a vehicle travelling at a velocity v relative to a (fixed) transmitter is given by the formula

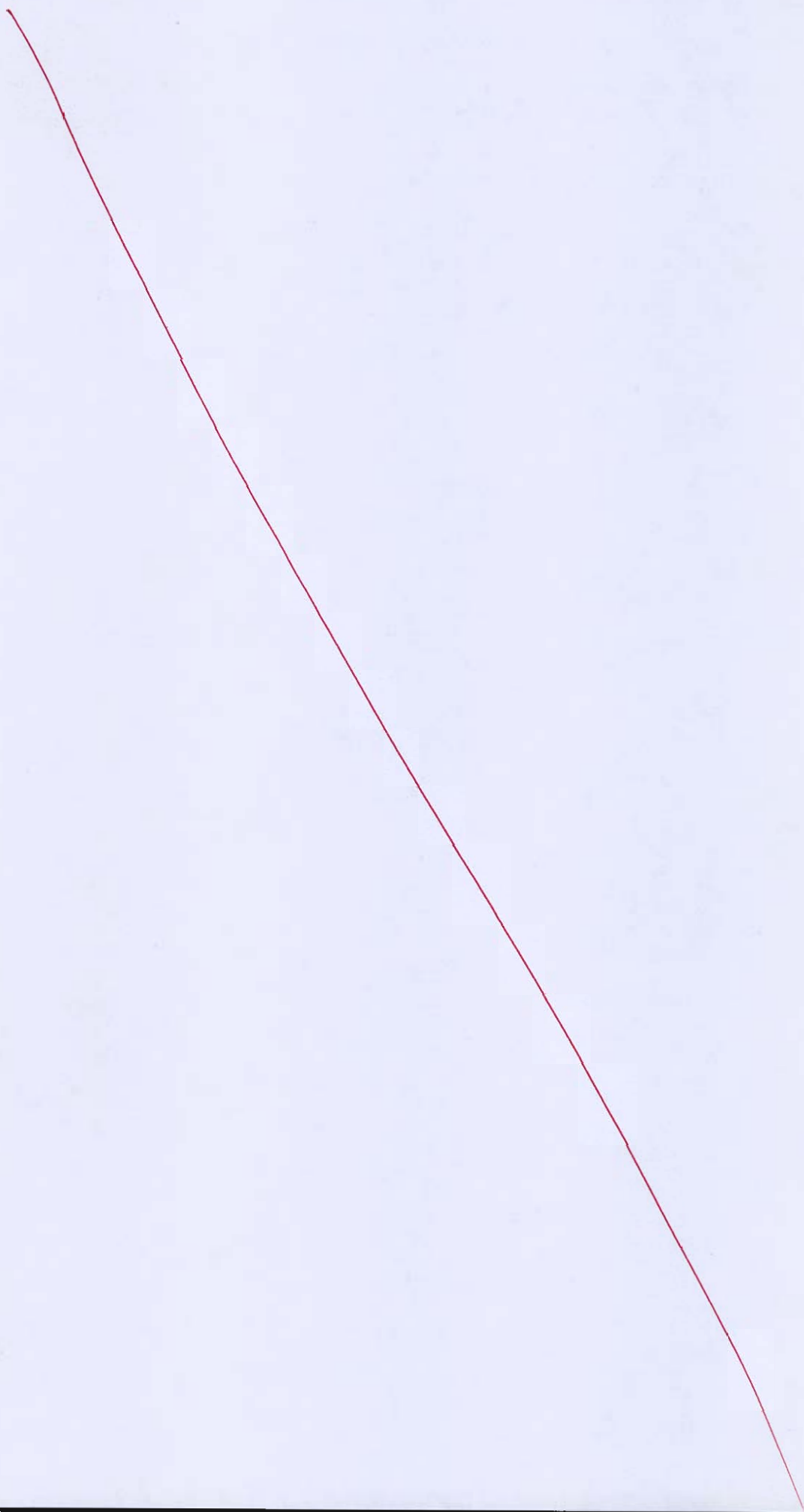
$$f_D = \pm \frac{v}{\lambda}$$

where λ is the wavelength, and the sign depends on the direction (moving toward or moving away) that the vehicle is travelling relative to the transmitter. Suppose that a vehicle is travelling at a speed of 100 km/h relative to a base station in a mobile cellular communication system. The signal is a narrowband signal transmitted at a carrier frequency of 1 GHz.

- (i) Determine the Doppler frequency shift.
- (ii) What should be the bandwidth of a Doppler frequency tracking loop if the loop is designed to track Doppler frequency shifts for vehicles travelling at speeds up to 100 km/h?
- (iii) Suppose the transmitted signal Bandwidth is 2 MHz centered at 1 GHz. Determine the Doppler frequency spread between the upper and lower frequencies in the signal.

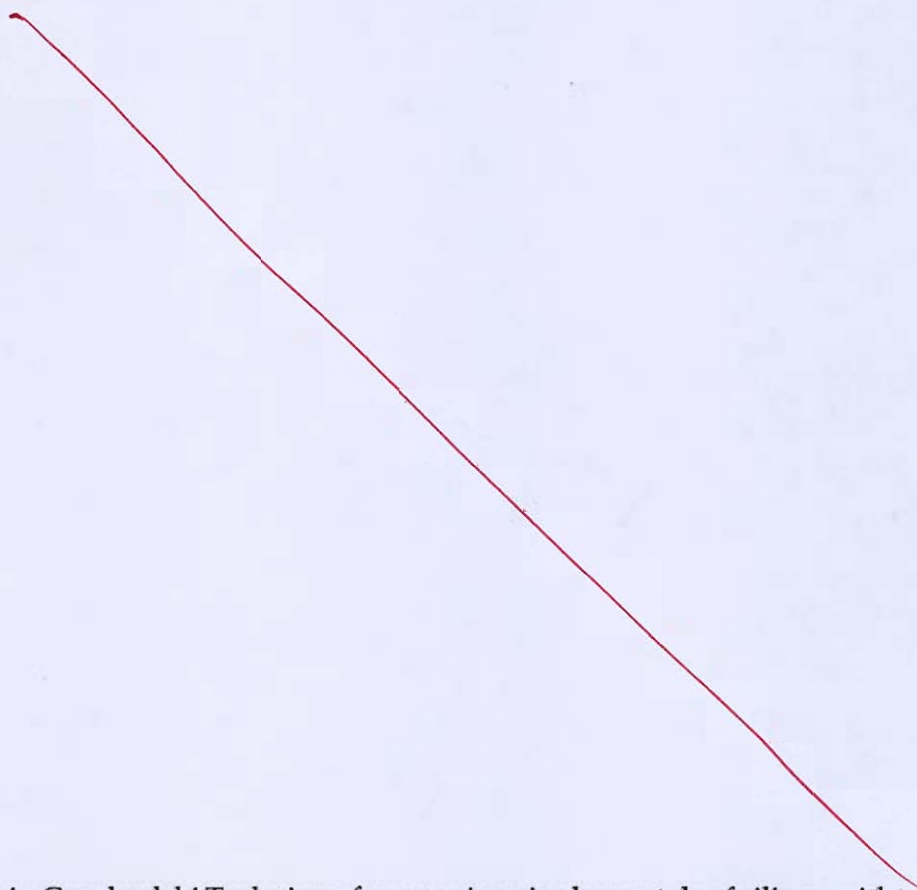
[12 marks]



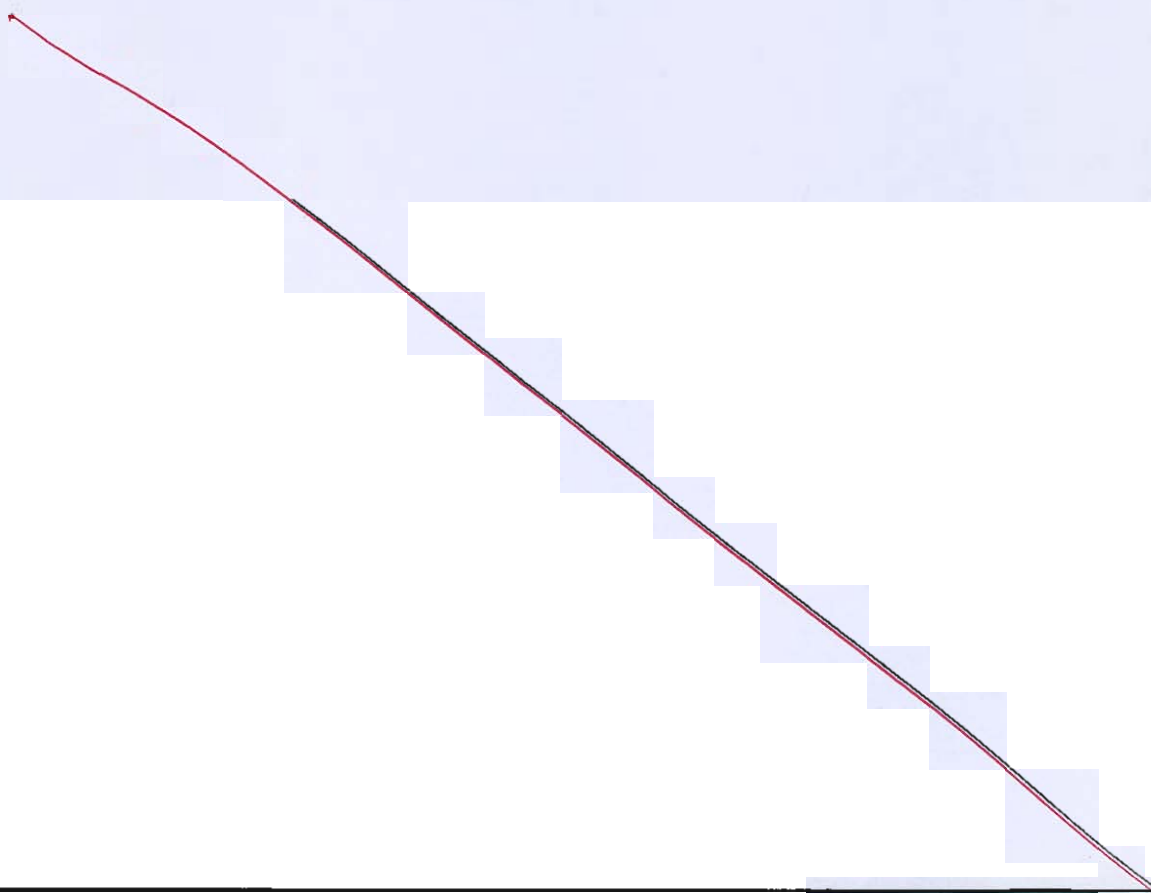


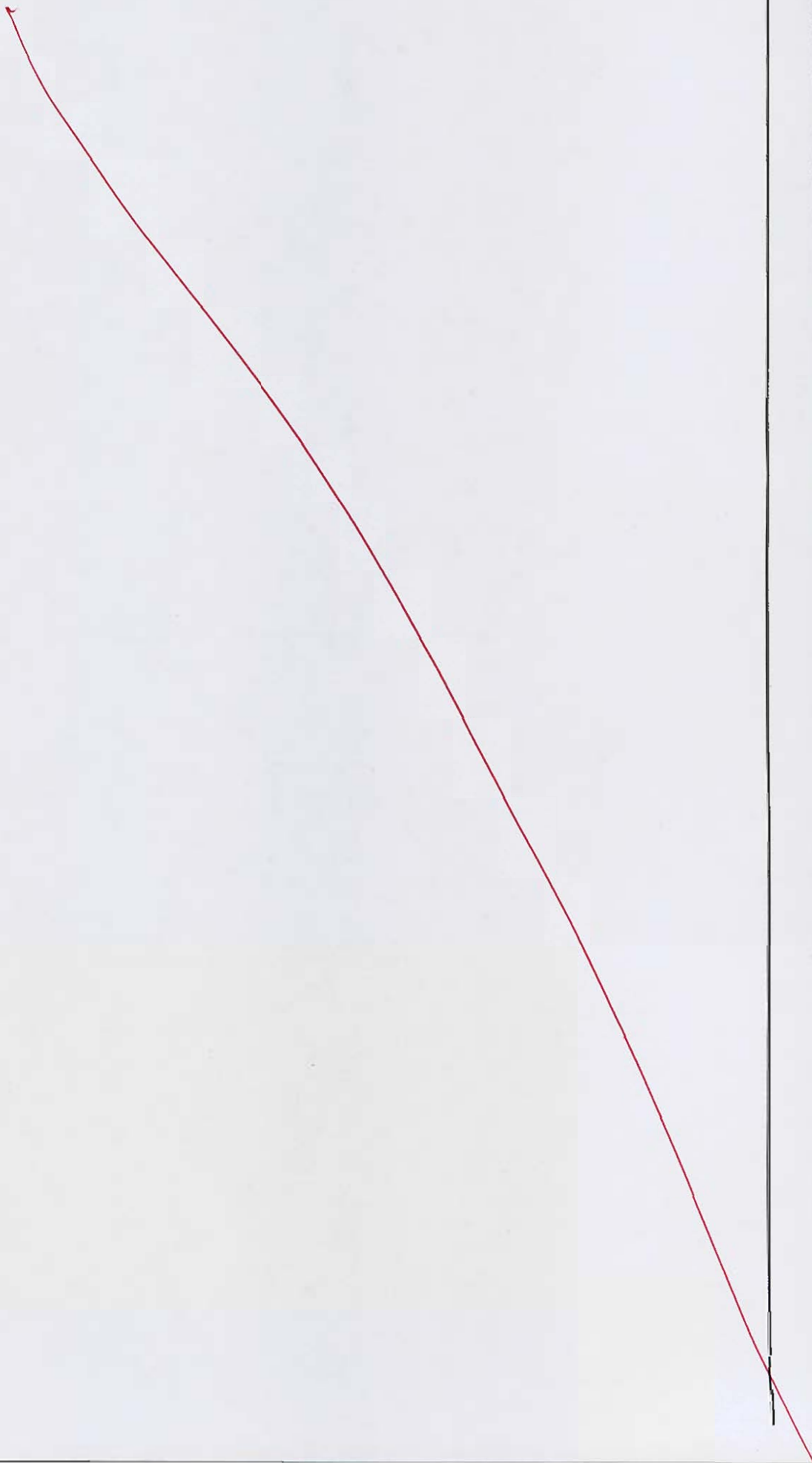
- Q.1 (d) A low earth orbit satellite is in a circular polar orbit with an altitude, h of 1200 km. A transmitter on the satellite has a frequency of 3.56 GHz. [$GM = 3.98 \times 10^{11} \text{ Nm}^2 \text{ kg}$]
- (i) Find the velocity of the satellite in orbit.
 - (ii) Find the component of velocity toward an observer at an earth station as the satellite appears over the horizon, for an observer who is in the plane of the satellite orbit.
 - (iii) Hence, find the Doppler shift of the received signal at the earth station. Use a mean earth radius value, r_e of 6378 km.
 - (iv) The satellite also carries a Ka-band transmitter at 25 GHz. Find the Doppler shift for this signal when it is received by the same observer. What type of receiver will be needed for this?

[12 marks]



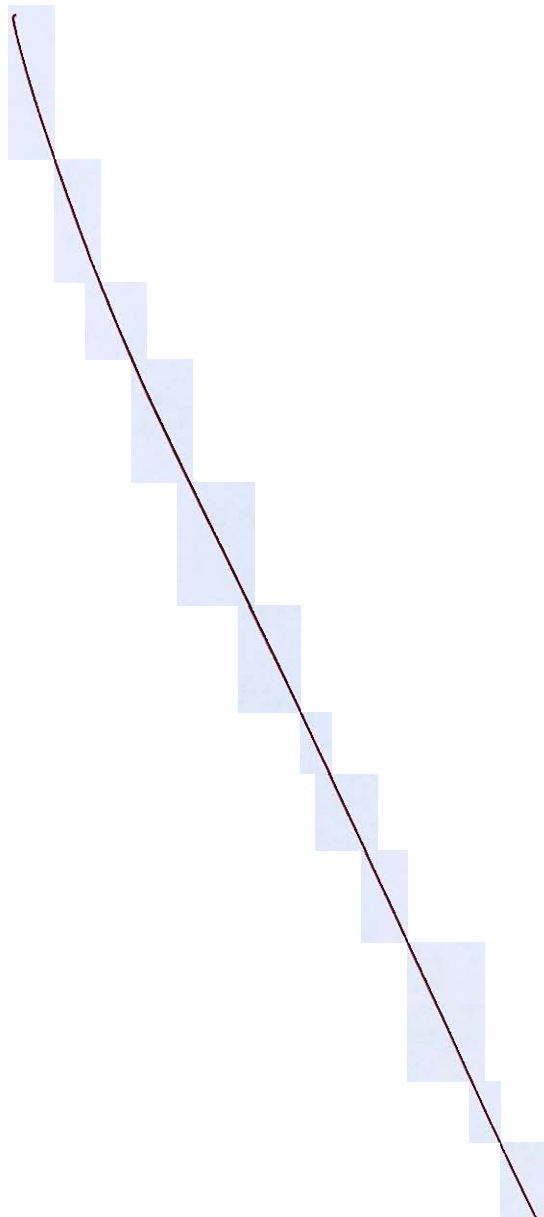
- 2.1 (e) Explain Czochralski Technique for growing single crystals of silicon with a neat diagram. [12 marks]

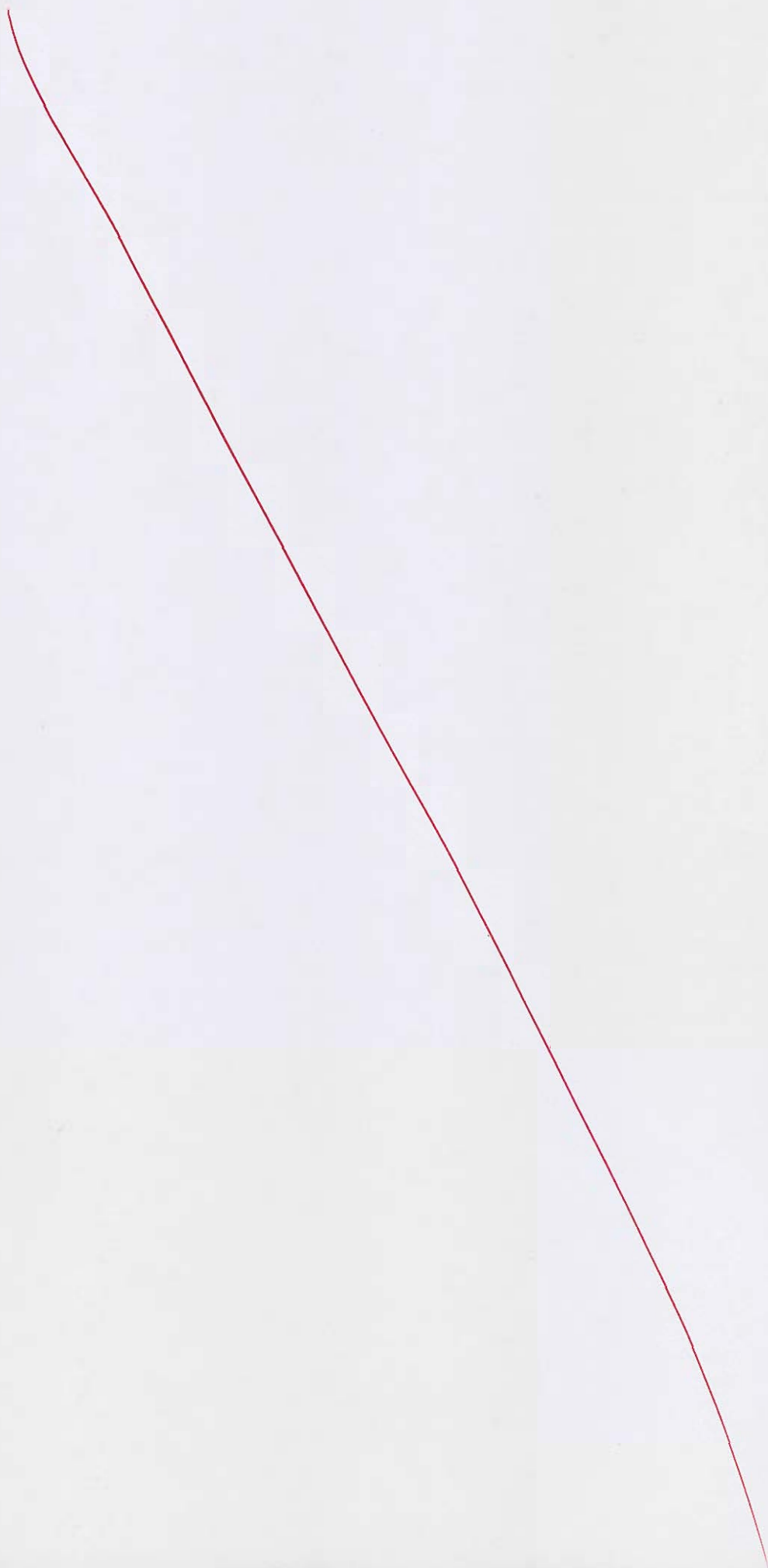




- 2 (a) A p-n junction is to be formed at a depth of $0.5 \mu\text{m}$ from the surface of an n-type Si substrate, which has a doping concentration of 10^{17} phosphorus atoms/ cm^3 . The junction is formed by a two-step diffusion of boron: the solid-solubility limited pre-deposition at 1100°C and the drive-in at 1200°C . After the drive-in step, the surface concentration of boron is 5×10^{19} atoms/ cm^3 . Find out the appropriate diffusion times required for both the steps (pre-deposition and drive-in)
- Assume the following data:
- Diffusion constant for boron (D_0) = $11.8 \text{ cm}^2/\text{sec}$.
- The activation energy for boron diffusion (E_a) = 4.36 eV .
- The solid solubility limit of boron in silicon at 1000°C = 2.6×10^{20} atoms/ cm^3 .

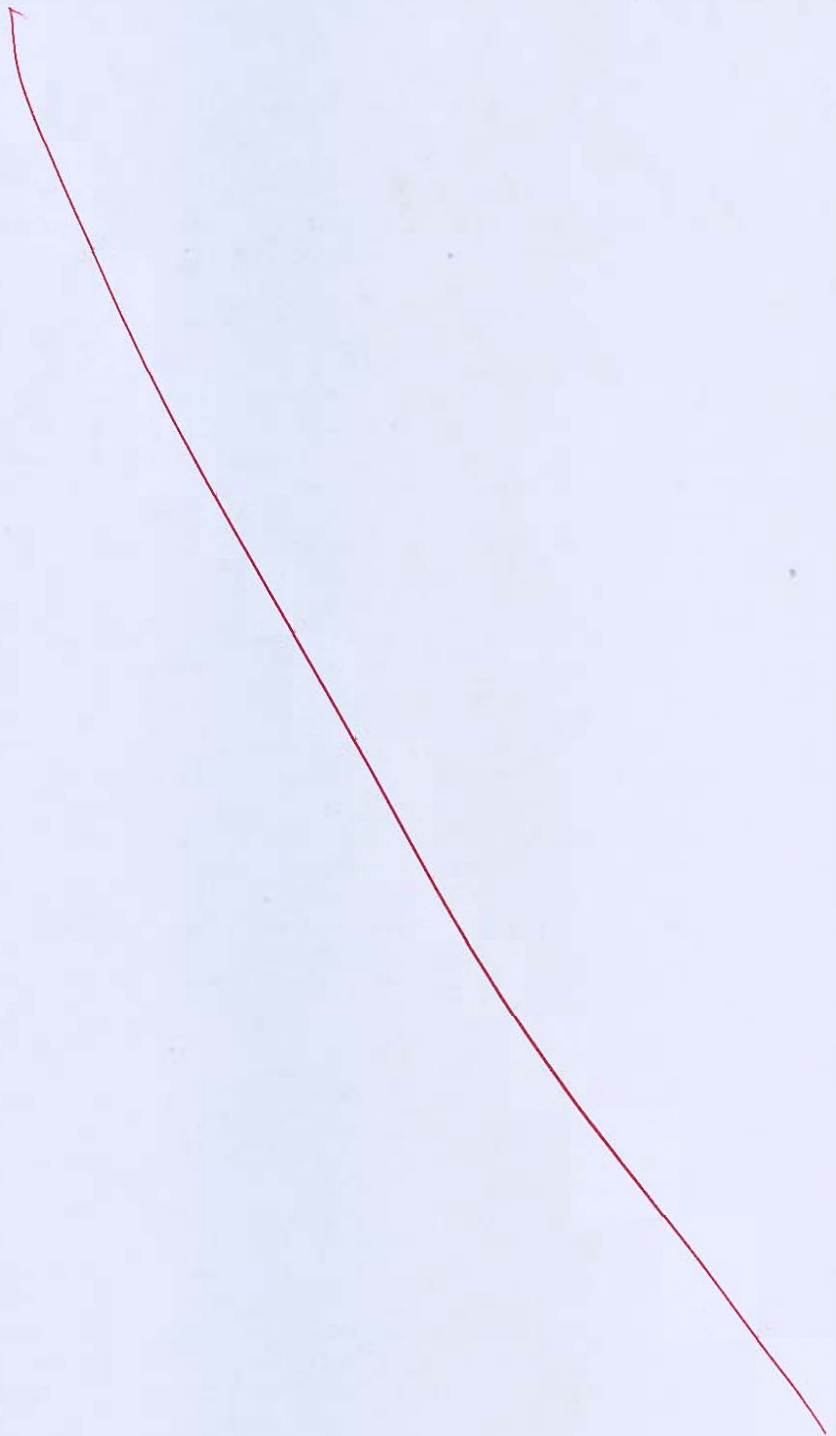
[20 marks]

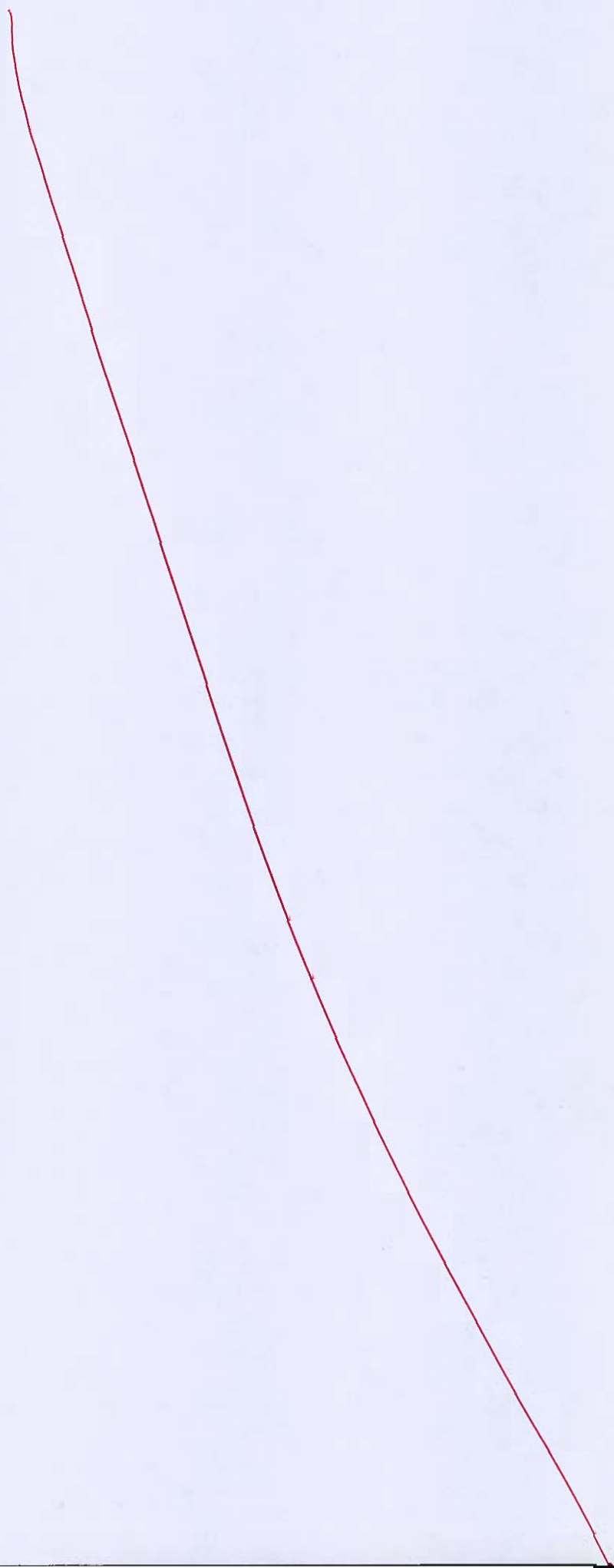




- Q.2(b) (i) Explain what is meant by the gyro frequency and why frequencies in the region of the gyro frequency are not suitable for ionosphere transmission. Calculate the maximum range obtainable in a single hop transmission utilizing F2 layer, situated at 400 km above the earth's surface. Assume earth radius as 6370 km.
- (ii) Assume that reflection take place at a height of 350 km and that the maximum density in the ionosphere corresponds to a 0.8 refractive index at 15 MHz. What will be the range (assume flat earth) for which the MUF is 20 MHz?

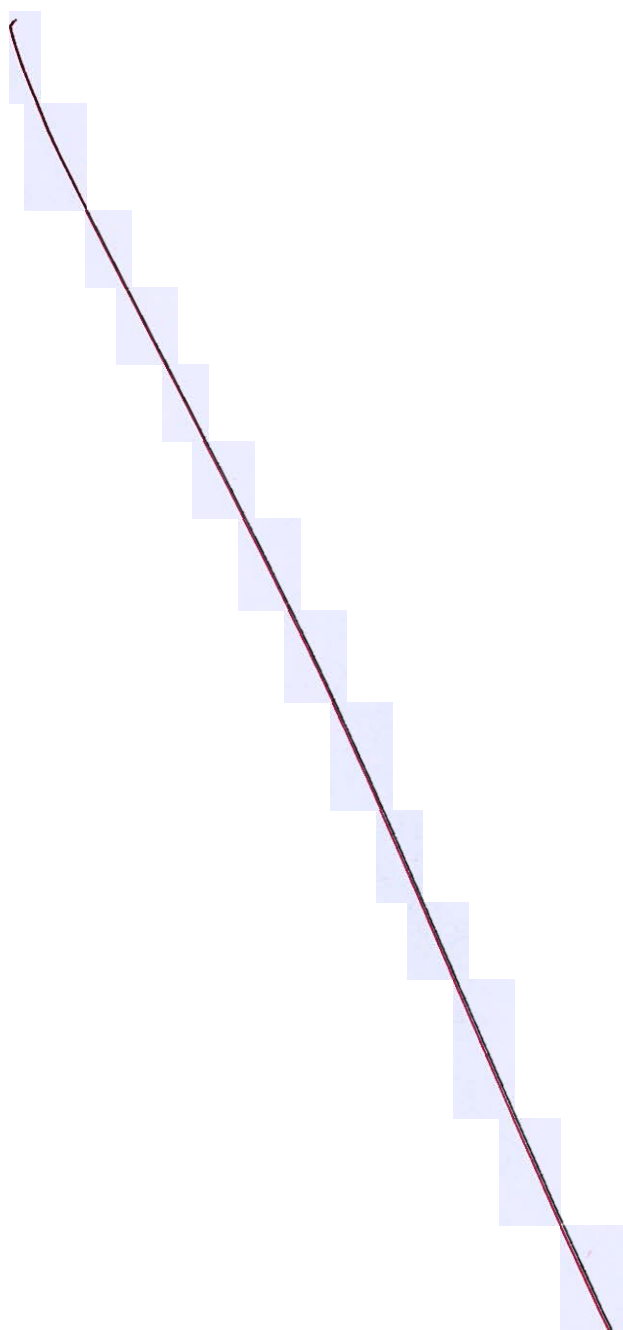
[14 + 6 marks]





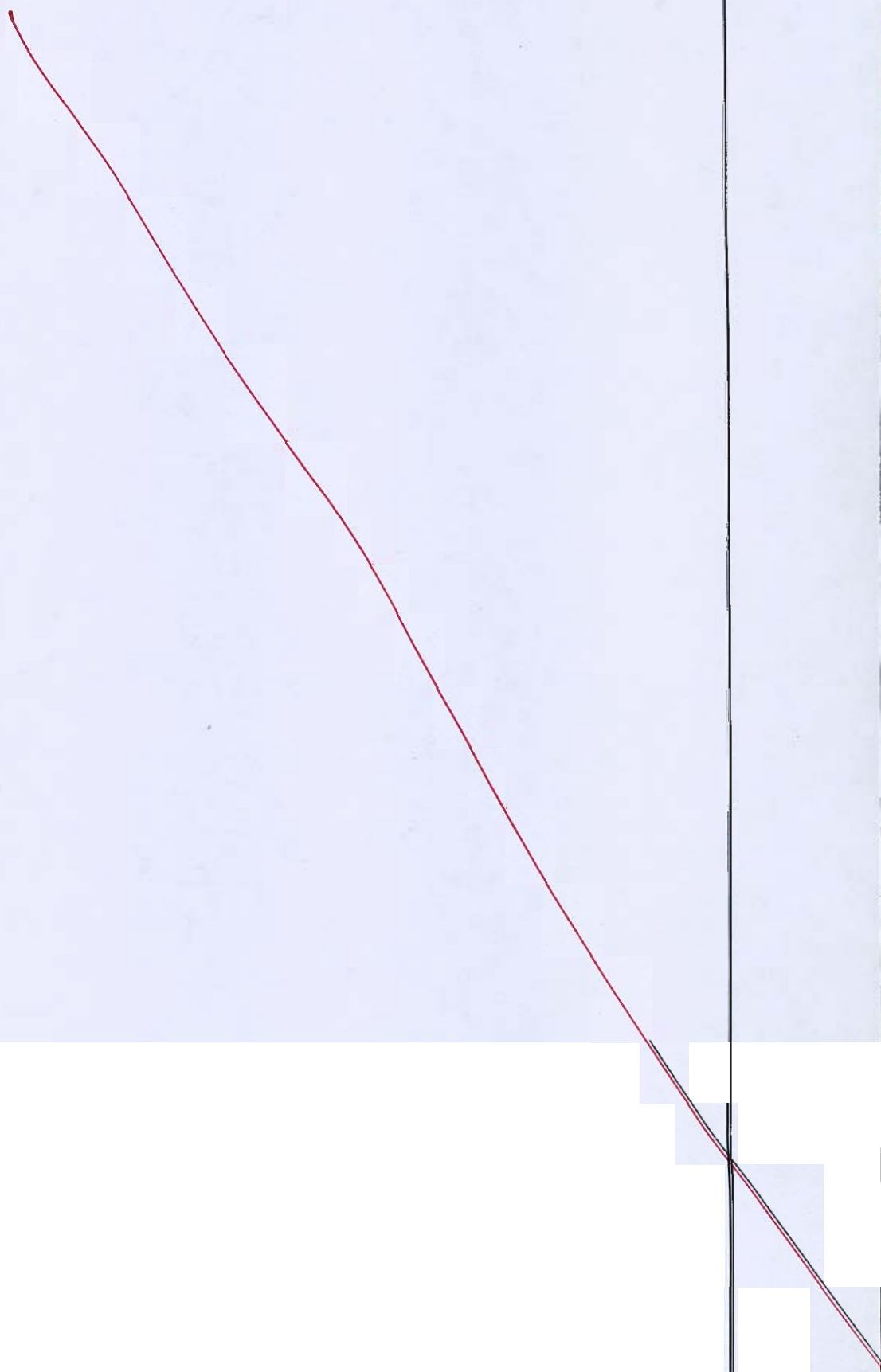
- Q.2 (c) (i) A hard disk with a transfer rate of 1 kbps is constantly transferring data to memory using DMA burst mode. The size of the data transfer is 16 bytes. The processor runs at 400 kHz clock frequency. The DMA controller requires 10 cycles for initialization of operation and transfer takes 2 cycles to transfer one byte of data from the device to the memory. What is the percentage of time for which the CPU is blocked during this DMA operation?
- (ii) Consider a 4 block cache memory (Initially empty) with the following main memory block references 4, 5, 7, 12, 4, 5, 13, 4, 5, 7. Find the hit ratio for the following page replacement algorithms:
1. FIFO
 2. LRU

[10 + 10 marks]



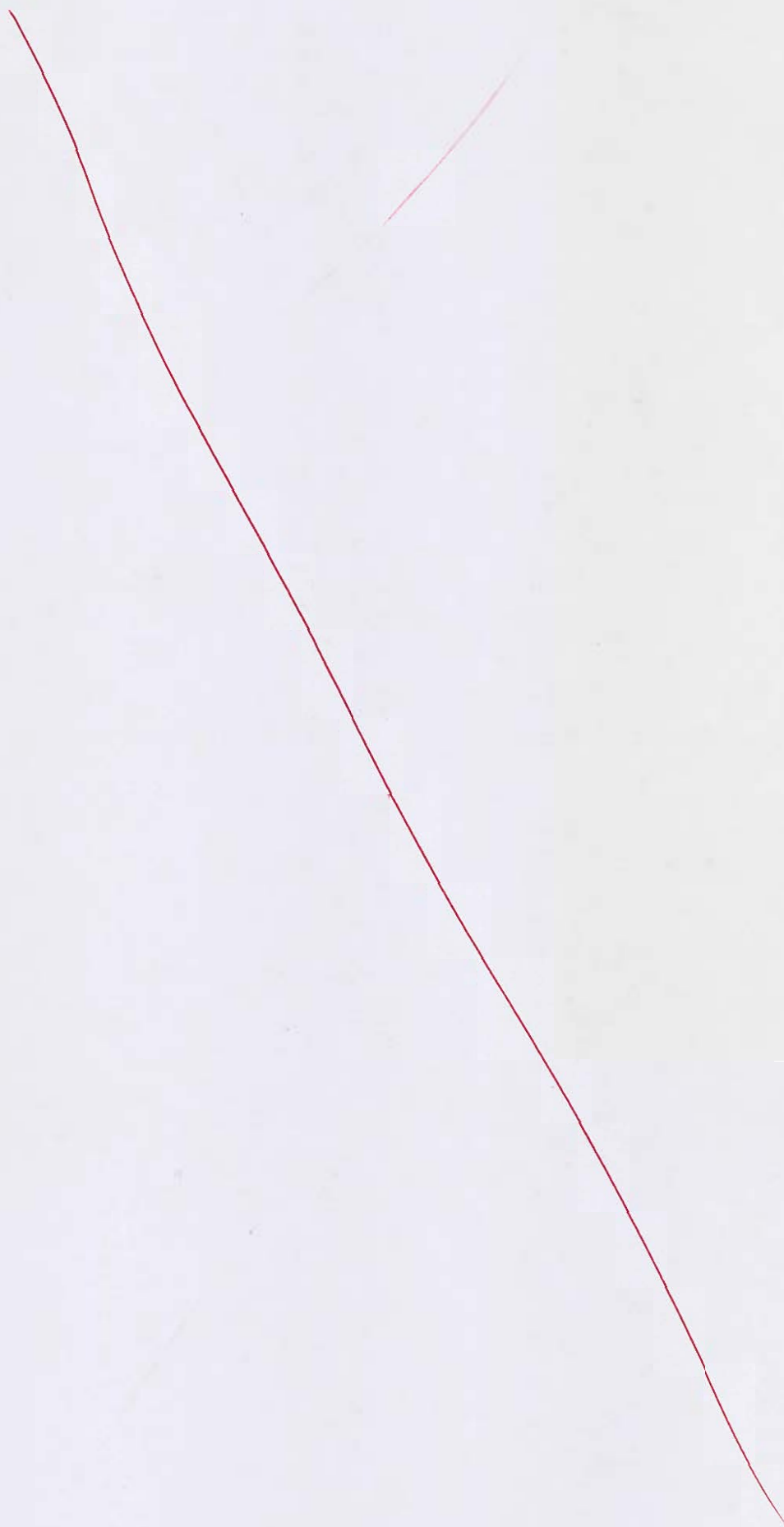
- Q.3 (a) (i) A digital computer has a memory unit with 32 bits per word. The instruction set size is 250. All instructions supported by computer have one mode field to support 10 addressing modes and an address field; apart from opcode field. What is the maximum allowable size of memory if each instruction is stored in one word?
- (ii) Consider a system with instruction set that uses a fixed 19 bits instruction length and length of address is 8 bits. There are 6 two address instructions. What is the maximum number of one address instructions if the number of zero address instructions are 65536?

[8 + 12 marks]



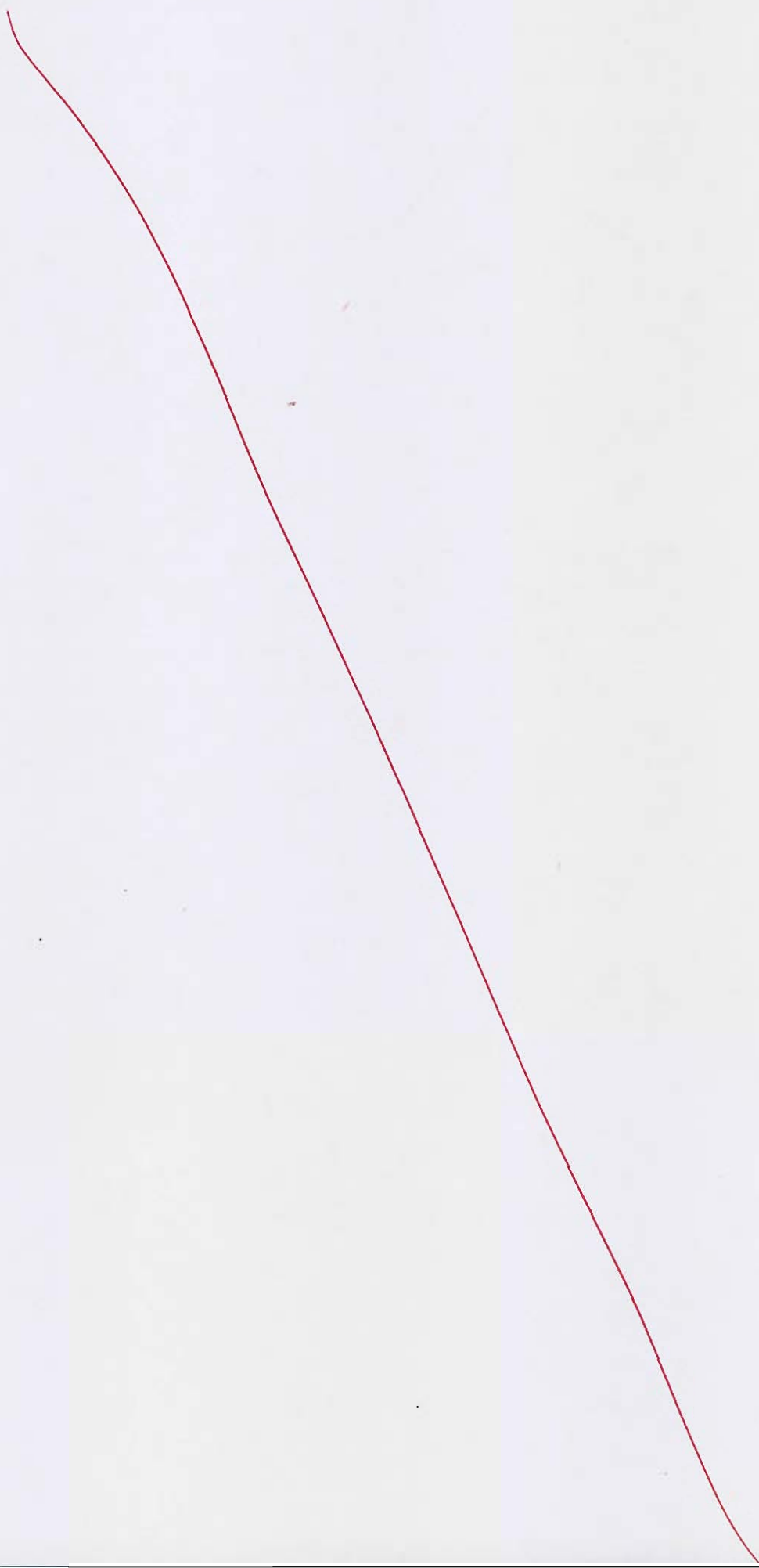
Q.3 (b) Explain in detail how the digital signature works and the assurances provided by digital signature.

[20 marks]



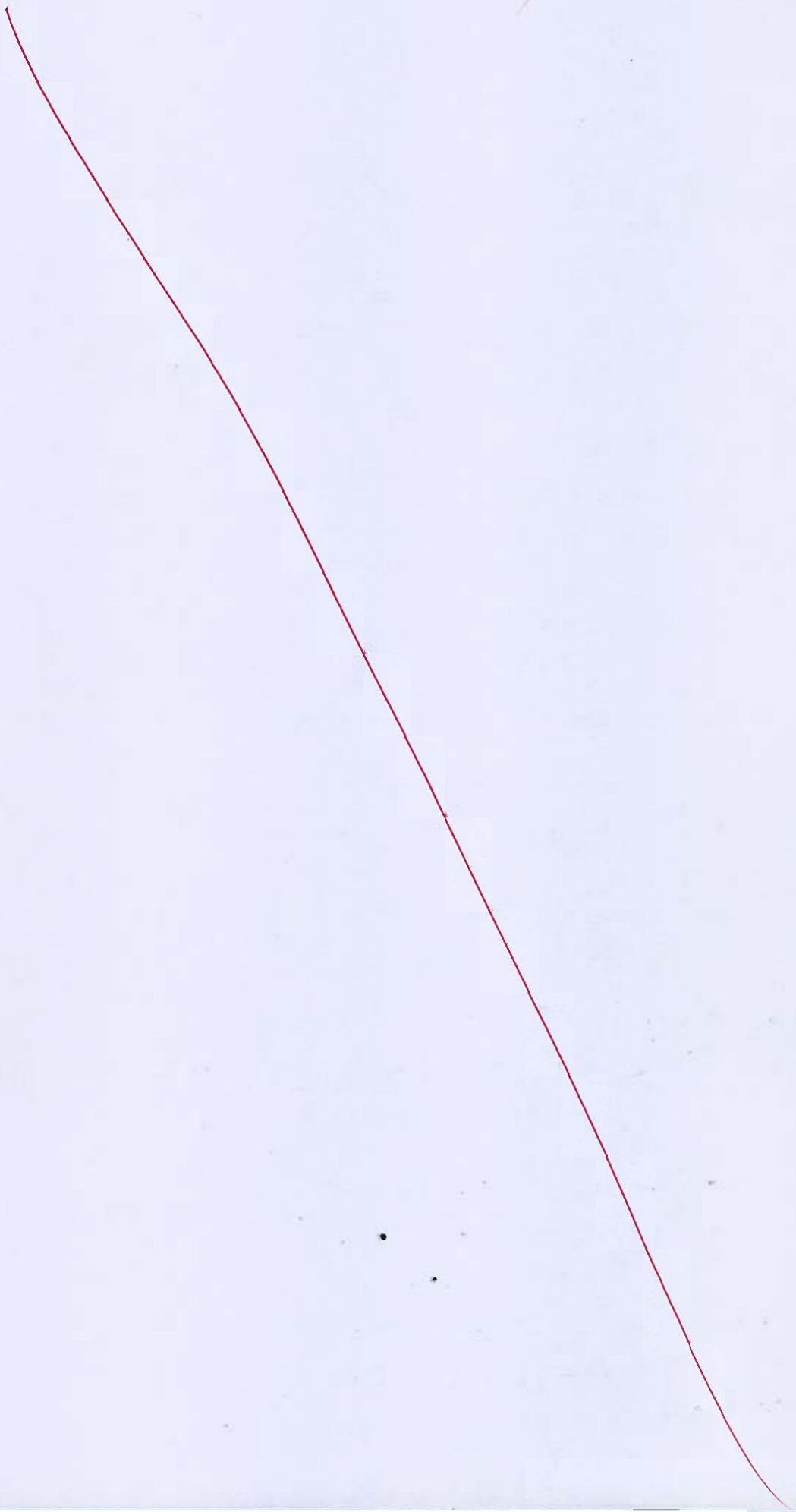
- Q.3 (c) (i) Bismuth is implanted in a p-type silicon sample with a uniform doping concentration of 10^{18} atoms/cm³. If the beam current density is $5 \mu\text{A}/\text{cm}^2$ and the implantation is carried out for 20 minutes, calculate the implantation dose. Also, find the peak impurity concentration.
Assume, $R_p = 2 \mu\text{m}$ and $\Delta R_p = 0.5 \mu\text{m}$.
- (ii) Use frequency sampling method, design a bandpass filter with the following specifications:
- $f_{c1} = 2 \text{ kHz}$
 $f_{c2} = 4 \text{ kHz}$
 $f_s = 8 \text{ kHz}$
- Find the filter coefficients for $N = 5$.

[8 + 12 marks]

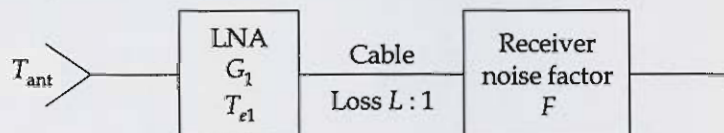


- Q.4 (a) A receiver in a urban cellular radio system detects a 1 mW at $d = d_0 = 1.5$ m from the transmitter. In order to mitigate co-channel interference effects, it is required that the signal received at any base station receiver from another base station transmitter which operates with the same channel must be below '-100 dBm'. A measurement team has determined that the average path loss exponent in the system is $n = 4$. Determine the minimum radius of each cell if a seven-cell reuse pattern is used. What is the minimum radius if a four-cell reuse pattern is used?

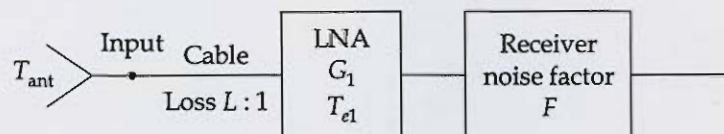
[20 marks]



- Q.4(b) (i) For the system shown in figure below, the receiver noise figure is 12 dB, the cable loss is 8 dB, the LNA gain is 60 dB, and its noise temperature 150 K. The antenna noise temperature is 45 K. Calculate the noise temperature referred to the input.



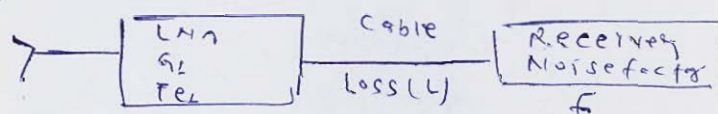
Repeat the calculation when the system of figure (a) is arranged as shown in figure below.



- (ii) Explain Bridgman method used for growth of crystals from molten material with neat diagram.

[10 + 10 marks]

Solution (i)



$$F = 12 \text{ dB} = 15.846$$

$$\text{Cable loss (L)} = 8 \text{ dB} \Rightarrow 10^{0.8} \\ = 6.31$$

$$\text{LNA Gain (G}_1) = 60 \text{ dB} = 10^6$$

$$\text{Noise temperature (T}_{e1}) = 150 \text{ K}$$

$$\text{Antenna noise temperature (T}_{\text{ant}}) = 45 \text{ K}$$

Noise temperature referred to input (T_{eq})

$$T_{eq} = T_{ant} + T_{c1} + \frac{T_{c2}}{G_1} + \frac{T_{n3}}{G_1 G_2} \quad \text{--- (1)}$$

cable Noise temperature (T_{c2}) = $(L-1)T_0$

$$T_{c2} = (6.31-1) \times 300$$

$$T_{c2} = 1593 \text{ K}$$

$$\text{cable gain } (G_1) = \frac{1}{L} =$$

Receiver noise temperature (T_{n3}) = $(F-1) \times T_0$

$$T_{n3} = (15.848-1) \times 300$$

$$T_{n3} = 4454.4 \text{ K}$$

Now from (1)

$$T_{eq} = 45 + 150 + \frac{1593}{206} + \frac{4454.4 \times 6.31}{106}$$

$$= 45 + 150 + 0.001593 + 0.028$$

$$T_{eq} = 195.03^\circ \text{K}$$

$$\text{Ans } \boxed{\text{Noise temperature } (T_{eq}) = 195.03^\circ \text{K}}$$

case-2

Noise temperature referred to input (T_{eq})

$$T_{eq} = T_{ant} + T_{c2} + \frac{T_{c1}}{G_2} + \frac{T_{n3}}{G_2 G_1}$$

$$= T_{ant} + T_{c2} + T_{c1} \times L + \frac{T_{n3} \times L}{G_1}$$

$$= 45 + 1593 + 150 \times 6.31 + \frac{4454.4 \text{ K} \times 6.31}{206}$$

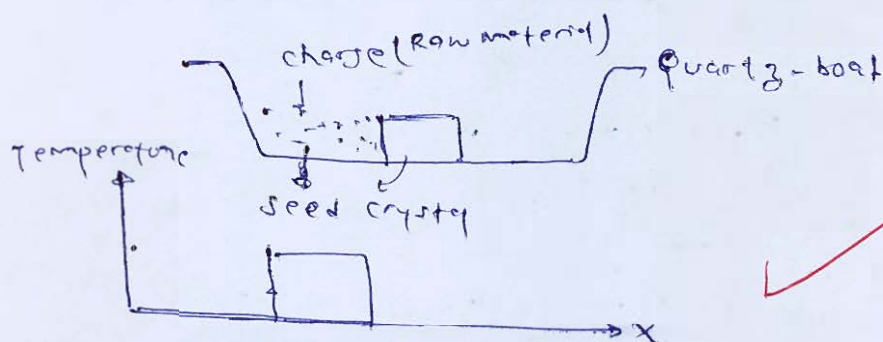
$$T_{eq} = 2584.53 \text{ K}$$

$$\text{Ans } \boxed{T_{eq} = 2584.53 \text{ K}}$$

10

Solution (iii) - 8

Bridgman Method - 8



In Quartz-boat, seed crystal and molten raw material is kept. By using heating mechanism charge is kept into molten state.

• We have to take care of that seed crystal does not melt.

• After solidification, charge take orientation of seed crystal.

Disadvantage.

• In this method after solidification, its volume increases, hence there will be defects comes. Hence it can't be used at high temperature application.

Advantage - In this raw material is silicon charge. Hence it is cost effective effective method.

- (c) (i) Consider a disk with an average seek time of 4 ms, rotation speed of 15000 rpm, and 512-byte sectors with 500 sectors per track. Suppose that we wish to read a file consisting of 2500 sectors for a total of 1.28 Mbytes. Explain and estimate the total time for the transfer in case of
1. Sequential access.
 2. Random access.
- (ii) Explain the functions of following CPU registers:
1. MAR
 2. MDR

[16 + 4 marks]

Solution (i) for given Disk

$$\text{seek time } (t_s) = 4 \text{ ms}$$

$$\text{rotation speed} = 15000 \text{ RPM}$$

$$\text{As } 15000 \text{ revolution made} = 1 \text{ min} = 60000 \text{ ms}$$

$$\text{So } 1 \text{ Revolution time} = \frac{60,000}{15000}$$

$$= 4 \text{ ms}$$

$$\text{average rotational latency time } (t_r) = \frac{\text{one Revolution time}}{2}$$

$$t_r = \frac{4}{2}$$

$$t_r = 2 \text{ ms}$$

$$\text{one-sector transfer time} = \frac{1 \text{ Revolution time}}{\text{Number of sectors/track}}$$

$$= \frac{4}{500}$$

$$= 0.008 \text{ ms}$$

$$\text{given total sector } (n) = 2500$$

(1) sequential access

$$\text{average transfer time } (T_{avg}) = \text{seek time} + \text{average rotational latency} + \text{Number of sectors} \times 1\text{-sector transfer time}$$

$$T_{avg} = 4 + 2 + 2500 \times 0.008$$

$$T_{avg} = 26 \text{ ms}$$

Ans (transfer time $(T_{avg}) = 26 \text{ ms}$)

(i) for Random access

$$\text{Transfer time (T}_{\text{tr}}) = \text{Number of sectors} [\text{seek time} + \text{rotational latency} + \text{sector transfer time}]$$

$$= 2500 [4 + 2 + 0.008]$$

$$= 15020 \text{ ms}$$

Ans Transfer time (T_{tr}) = 15020 ms

Solution (ii)

(1) MAR:- It is referred as 'Memory address register'. MAR is used to send address to memory. In both memory read and memory write cases.

(2) MDR:- It is referred as 'Memory data register'. It is used to send and receive data. In memory read and write case.

**Section B : Advanced Electronics + Computer Organization and Architecture
+ Advanced Communication**

- (a) (i) Explain the types of Cache Misses.
- (ii) Consider a pipeline system with 6 segments. Segment delays are 5 ns, 8 ns, 6 ns, 9 ns, 7 ns and 8 ns. Intermediate register delay is 1 ns which is used after each segment. In the given system, 1000 instructions are to be executed. Among 1000 instructions, 20% are branch instructions each of which incurs 3 pipeline stall cycles. 30% of total 1000 instructions causes resource conflict because of which 1 stall cycles is incurred for such instructions.
- Determine the speed-up of this pipeline as compared to the corresponding non-pipeline system.

[4 + 8 marks]

Solution(i)-

Types of Cache Miss-

There are '3' type of cache misses, which is given below.

- (1) cold or compulsory miss
- (2) capacity miss
- (3) conflict miss

(1) Cold or compulsory miss-

first time access a block or request always miss occurs. This type of miss called cold or compulsory miss.

To minimise this cold miss, we increase size of blocks.

(2) capacity miss-

when cache is full then miss occurs called capacity miss.

To minimise capacity miss, we increase size of cache.

(3) conflict miss-

when cache set is full then miss occurs called conflict miss.

To minimise this associativity increase. i.e. in fully associative memory never conflict miss occurs.

Solution(ii)-

for pipeline system

given

number of segments (K) = 6

Number of instruction (n) = 1000

pipeline cycle time (t_p) = $\max(5ns, 8ns, 6ns, 9ns, 7ns, 8ns)$
+ additional delay (i.e. 1ns)

$$t_p = 9 + 1 \Rightarrow t_p = 10ns$$

task time (t_n) = sum of stage delay i.e. $5 + 8 + 6 + 9 + 7 + 8$
 $t_n = 43ns$

total cycles need in pipeline system i.e.

total cycles = $1 + 1000 \times 20\%$ due to branch $\times 3$ stall cycle
+ 30% of 1000 need to 1 stall cycle

$$= 1 + 3 \times 200 + 300$$

$$= 901 \text{ cycles}$$

execution time for pipeline (T_p) = total cycle $\times t_p$

$$T_p = 901 \times 10$$

$$T_p = 9010ns$$

execution time for non-pipeline system (T_n)

$$T_n = n \times t_n$$

$$= 1000 \times 43$$

$$= 43000ns$$

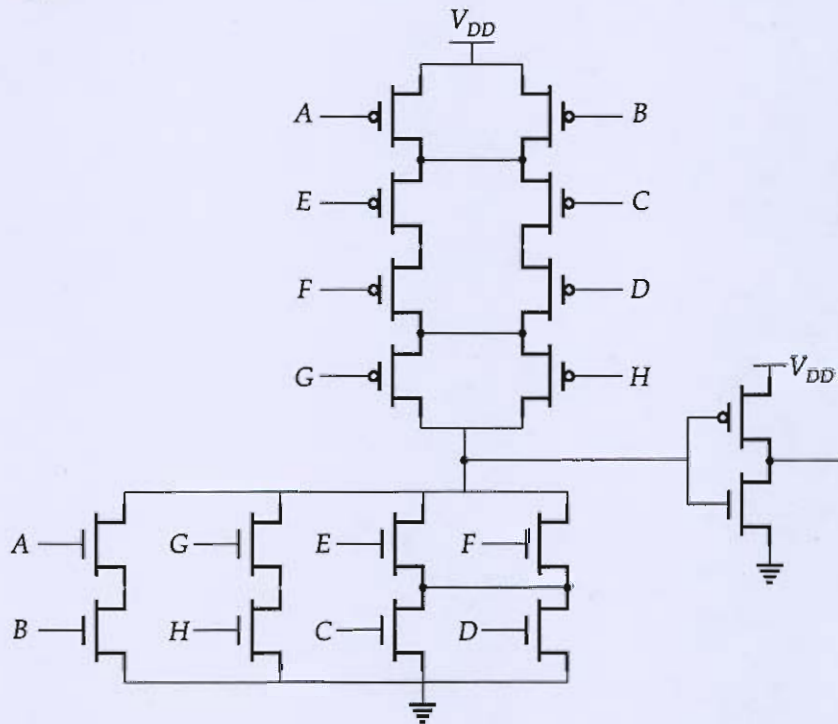
speedup = $\frac{\text{execution time of non pipeline } (T_n) \text{ system}}{\text{execution time of pipeline } (T_p) \text{ system}}$

$$\frac{43000}{9010}$$

$$= 4.77$$

Ans [speedup = 4.77]

5 (b) Explain Domino logic. Draw the domino CMOS logic version of the given conventional CMOS logic.



[12 marks]



- 5 (c) (i) Show that the total broadening of a light pulse ΔT due to intermodal dispersion in a multimode step index fibre may be given by:

$$\Delta T = \frac{L(NA)^2}{2n_1c}$$

where L is the fibre length, NA is the numerical aperture of the fibre, n_1 is the core refractive index and c is the velocity of light in vacuum.

- (ii) A multimode fibre is having a core refractive index of 1.5 and a relative index difference of 3%. Determine the critical radius of curvature at which large bending loss occur if the operating wavelength is $1.3 \mu m$.

[6 + 6 marks]

Solution (i) :-

In multimode step index fibre, there is delay differences between slowest and fastest modes. In extreme meridional rays and axial rays. Due to this intermodal dispersion occurs. These travels with same velocity and core having same refractive index. They arrives at certain distance at different times.

Let fibre length = L

Slowest mode due to axial rays

$$\text{Hence delay } (T_{\min}) = \frac{\text{Distance}}{\text{velocity}} = \frac{L}{c/n_1}$$

n_1 = core refractive index, c = velocity of light

$$T_{\min} = \frac{Ln_1}{c} \quad \text{--- (1)}$$

fastest mode due to extreme meridional rays.

$$\text{Hence delay } (T_{\max}) = \frac{L/\cos\theta}{c/n_1}$$

$$T_{\max} = \frac{Ln_1}{c \cos\theta} \quad \text{--- (2)}$$

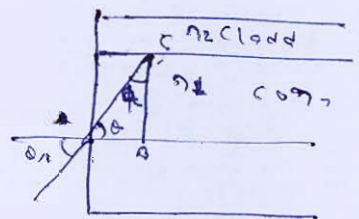
From fig

at total internal reflecting

$$\sin\phi_c = \frac{n_2}{n_1}$$

$$\triangle ABC \quad \cos\theta = \frac{n_2}{n_1}$$

$$\text{Now } T_{\min} = \frac{Ln_1}{c n_2} \quad \text{--- (3)}$$



Total pulse dispersion (ΔT) = $T_{max} - T_{min}$

$$\Delta T = \frac{L n_1^2}{c n_2} - \frac{L n_1}{c}$$

$$= \frac{L n_1}{c} \left[\frac{n_1}{n_2} - 1 \right]$$

$$= \frac{L n_1^2 \Delta}{c n_2}$$

IF $\Delta \ll 1$

$$\Delta T = \frac{L n_1 \Delta}{c} \quad \left[\Delta = \frac{n_1 - n_2}{n_2} \right]$$

Since Numerical aperture (NA) = $n_2 \sqrt{2\Delta}$

$$\text{Hence } \Delta T = \frac{L (NA)^2}{2 n_2 c}$$

$$\text{Hence proved } \Delta T = \frac{L (NA)^2}{2 n_2 c}$$

Solution (ii) :-

considering Multimode fiber

core refractive index (n_1) = 1.5

index difference (Δ) = 3%

wavelength (λ) = 1.3 μ m

$$\text{critical radius (Rc)} = \frac{3 n_1^2 \lambda}{4 \pi (NA)^3}$$

$$NA = n_2 \sqrt{2\Delta} \Rightarrow 1.5 \sqrt{2 \times 0.03}$$

$$NA = 0.128$$

$$\text{Now } Rc = \frac{3 (1.5)^2 \times 1.3}{4 \pi (0.128)^3} \mu\text{m}$$

$$Rc = 445.18 \mu\text{m}$$

$$Rc = 447.37 \mu\text{m}$$

Ans [critical radius (Rc) = 447.37 μ m]

Q.5 (d) (i) A glass fibre exhibits material dispersion given by $\left| \lambda^2 \frac{d^2 n}{d\lambda^2} \right|$ of 0.03 and fibre is used with a light source having rms spectral width of 15 nm.

Determine:

1. Material dispersion coefficient at a wavelength of 1.3 μm .
2. rms pulse broadening per kilometer due to material dispersion.
- (ii) 1. Prove that the maximum value of a/λ is approximately 1.4 times larger for a parabolic refractive index profile single-mode fibre than for a single-mode step index fibre. (a is the core radius)
2. If the refractive index of the core of a single-mode step index fiber is 1.49 and refractive index of the cladding is 1.48, find the fiber core diameter to enable single-mode transmission at a wavelength of 1.5 μm .

[6 + 3 + 3 marks]

Solution (i) - 8

$$\text{given } \left| \lambda^2 \frac{d^2 n}{d\lambda^2} \right| = 0.03$$

$$\text{Source spectral width } (\sigma_\lambda) = 15 \text{ nm}$$

$$\text{Core wavelength } (\lambda) = 1.3 \mu\text{m} = 1300 \text{ nm}$$

$$\text{Material dispersion coefficient } (M) = \frac{\lambda}{c} \left| \frac{d^2 n}{d\lambda^2} \right|$$

$$M = \frac{1}{\lambda c} \left| \lambda^2 \frac{d^2 n}{d\lambda^2} \right|$$

$$= \frac{1}{1300 \times 3 \times 10^8} \times 0.03$$

$$[c = 3 \times 10^8 \text{ km/sec}]$$

$$M = 76.92 \text{ ps nm}^{-1} \text{ km}^{-1}$$

$$\text{Ans [Material dispersion coefficient } (M) = 76.92 \text{ ps nm}^{-1} \text{ km}^{-1}]$$

- ② RMS pulse broadening per km due to material dispersion i.e. $\sigma_M = \sigma_\lambda M L$

$$\sigma_M = 15 \times 76.92 \times 1 = 1153.8 \text{ ps km}^{-1}$$

$$\text{Ans [RMS pulse broadening due to material dispersion } (\sigma_M) = 1153.8 \text{ ps km}^{-1}]$$

Solution (ii) :- (f) for parabolic profile

Numb.

① core index (n_1) = 1.49

clad index (n_2) = 1.48

core diameter = D

wavelength (λ) = 1.5 μm

for single mode

Normalized frequency number (V) = 2.405

As we know

$$V = \frac{2\pi a}{\lambda} (NA) \Rightarrow \frac{\pi \times D}{\lambda} (NA)$$

$$D = \frac{V \times \lambda}{\pi \times NA} \quad \text{--- (1)}$$

Numerical aperture (NA) = $\sqrt{n_1^2 - n_2^2}$

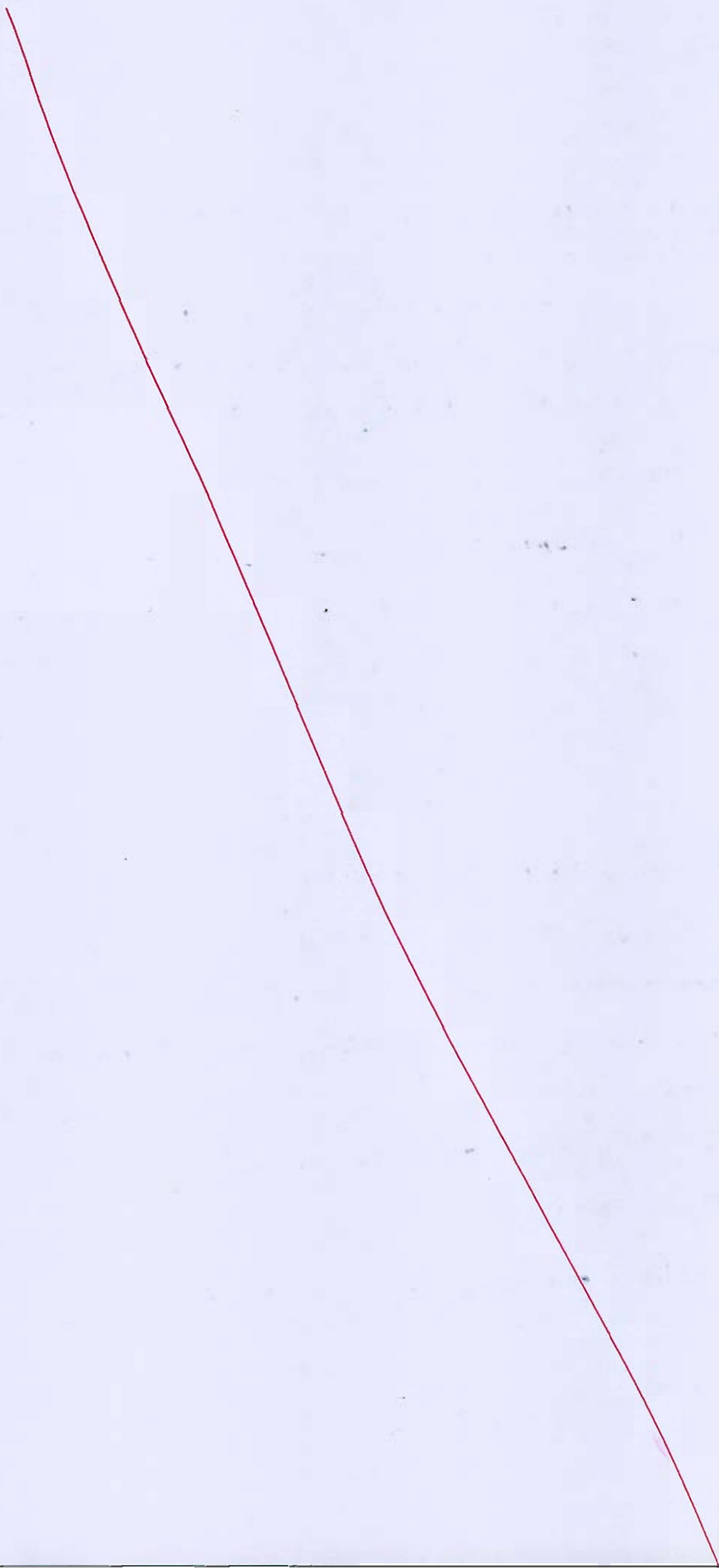
$$= \sqrt{(1.49)^2 - (1.48)^2}$$

$$NA = 0.1723$$

$$D = \frac{2.405 \times 1.5}{\pi \times 0.1723} \text{ } \mu\text{m}$$

$$= 6.66 \text{ } \mu\text{m}$$

$$\text{Ans [core diameter } (D) = 6.66 \text{ } \mu\text{m}]$$



- Q.5 (e) (i) Consider a hierarchical memory system that uses cache memory having access time of 80 ns, main memory with an access time of 200 ns and secondary memory with an access time of 800 ns. Hit ratio of cache memory is 80% and main memory hit ratio is 90%. Find the average memory access time of the memory system.
- (ii) Explain the Memory Hierarchy Design.

[8 + 4 marks]

Solution (i) - Hierarchical memory system

cache access time (T_m) = 80 ns

Main memory access time (T_{mm}) = 200 ns

Secondary memory access time (T_s) = 800 ns

Hit ratio (H_1) = 80% Main memory hit ratio (H_2) = 90%

Average memory access time (T_{avg})

$$T_{avg} = H_1 T_m + (1 - H_1) [H_2 (T_m + T_{mm}) + (1 - H_2) (T_m + T_{mm} + T_s)]$$

$$= 0.8 \times 80 + 0.2 [0.9 (80 + 200) + 0.1 (80 + 200 + 800)]$$

$$= 136 \text{ ns}$$

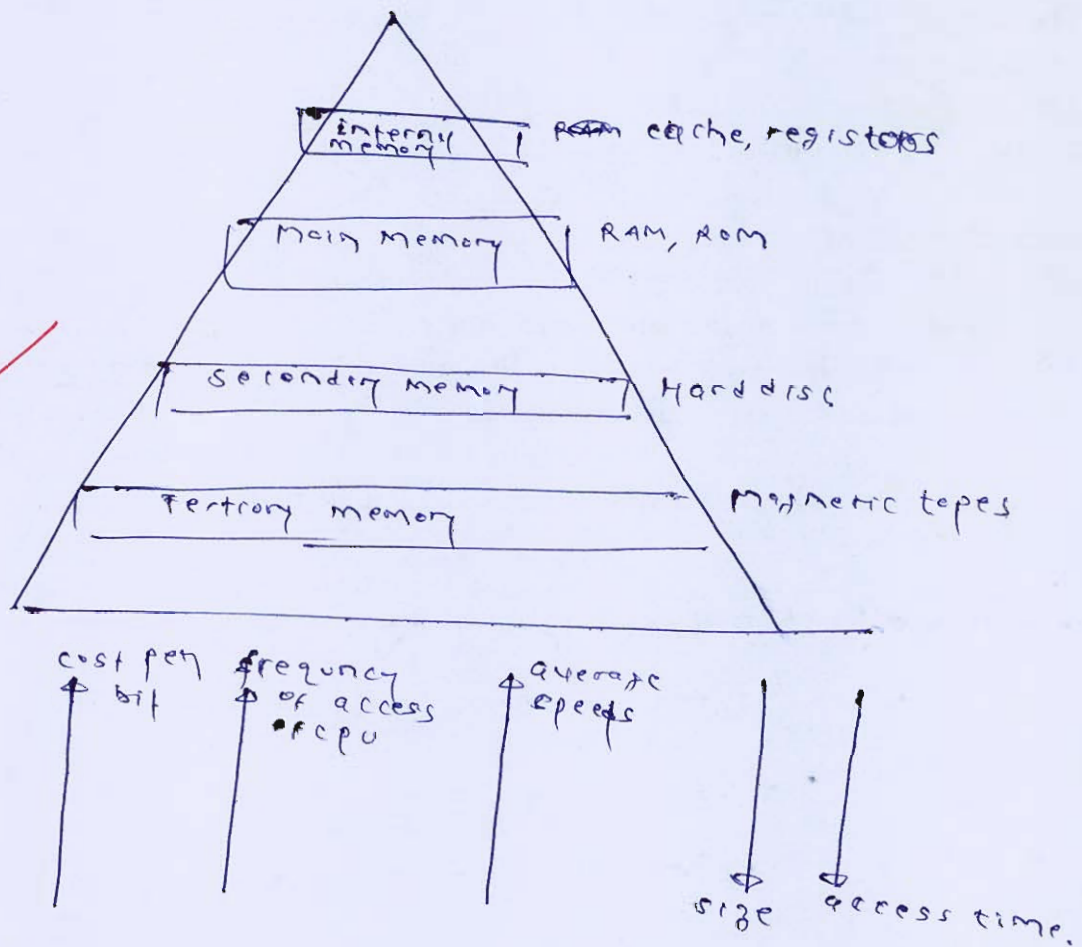
Ans $T_{avg} = 136 \text{ ns}$

(ii) Memory Hierarchy design -

Instead of using single memory, a hierarchy of memory is used. There is following advantage (main goal) of using hierarchy memory.

- (1) It maximise average speed of memory
- (2) It minimise cost per bit of memory.

Hierarchical memory design given below



As moving up, cost per bit, frequency of access of CPU, and average speeds increases.

As we moving down size of memory, and access time increases.

Q.6 (a) The downlink C/N_0 ratio in a direct broadcast satellite (DBS) system is estimated to be 85 dB-Hz.

The specifications of the link are:

Satellite EIRP = 57 dBW,

Downlink carrier frequency = 12.5 GHz,

Data rate = 10 Mb/s,

Required E_b/N_0 at the receiving earth terminal = 10 dB,

Distance of satellite from the receiving earth terminal = 41000 km.

Calculate the minimum diameter of the dish antenna needed to provide a satisfactory TV reception, assuming that the dish has an efficiency of 55 percent and it is located alongside the home where the temperature is 310 K. For this calculation, assume that the operation of the DBS system is essentially downlink limited.

[20 marks]

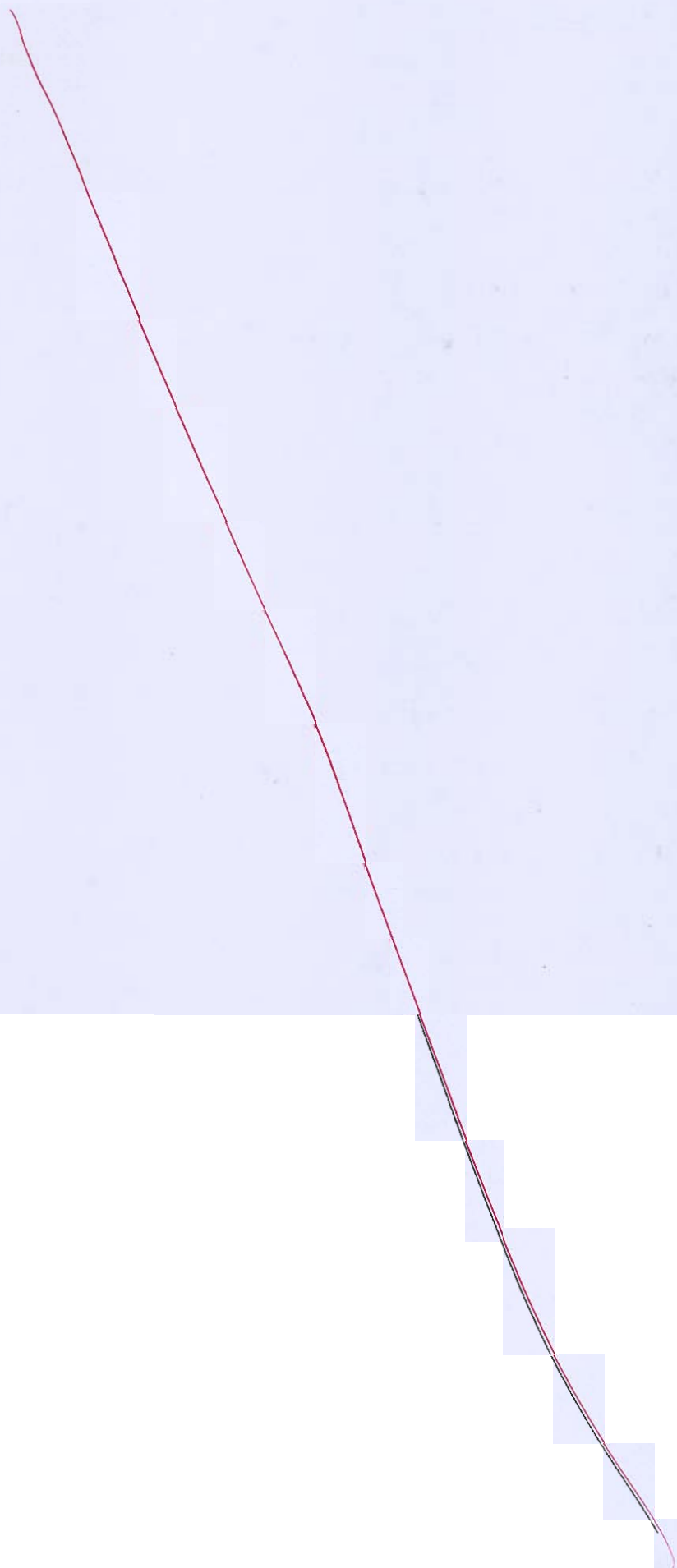
Solution

$$\text{Dish antenna gain } (G_a) = \eta^2 \left(\frac{D}{\lambda} \right)^2$$

where D = diameter of dish antenna

$$\eta = \text{efficiency} = 55\%$$

$$R = \text{distance of satellite and earth terminal} = 41000 \text{ km}$$



- Q.6 (b) (i) Explain in detail the types of scaling used in VLSI technology.
- (ii) What is the oxide thickness after dry oxidation at 1500°C carried out for 2 hours? By assuming initial oxide thickness is zero.
[Given; $A = 0.2 \mu\text{m}$, $B = 0.5 \mu\text{m}^2/\text{hr}$]

[12 + 8 marks]

Solution (ii)

$$\text{time } (t) = 2 \text{ hours}$$

$$A = 0.2 \mu\text{m}, B = 0.5 \mu\text{m}^2/\text{hr}$$

As we know from

Deal-Grove models

oxide thickness (t_{ox}) and time relation is given by Deal-Grove models

$$t_{ox}^2 - A t_{ox} = B(t + \tau)$$

$$\tau = \text{initia} \text{ time} = 0 \text{ (given)}$$

Now

$$t_{ox}^2 - 0.2 t_{ox} = 0.5 \times 2$$

$$t_{ox}^2 - 0.2 t_{ox} - 1 = 0$$

After solving we get

$$t_{ox} = 1.205 \mu\text{m} \text{ or } -0.904$$

we select $t_{ox} > 0$

$$\text{So } t_{ox} = 1.205 \mu\text{m}$$

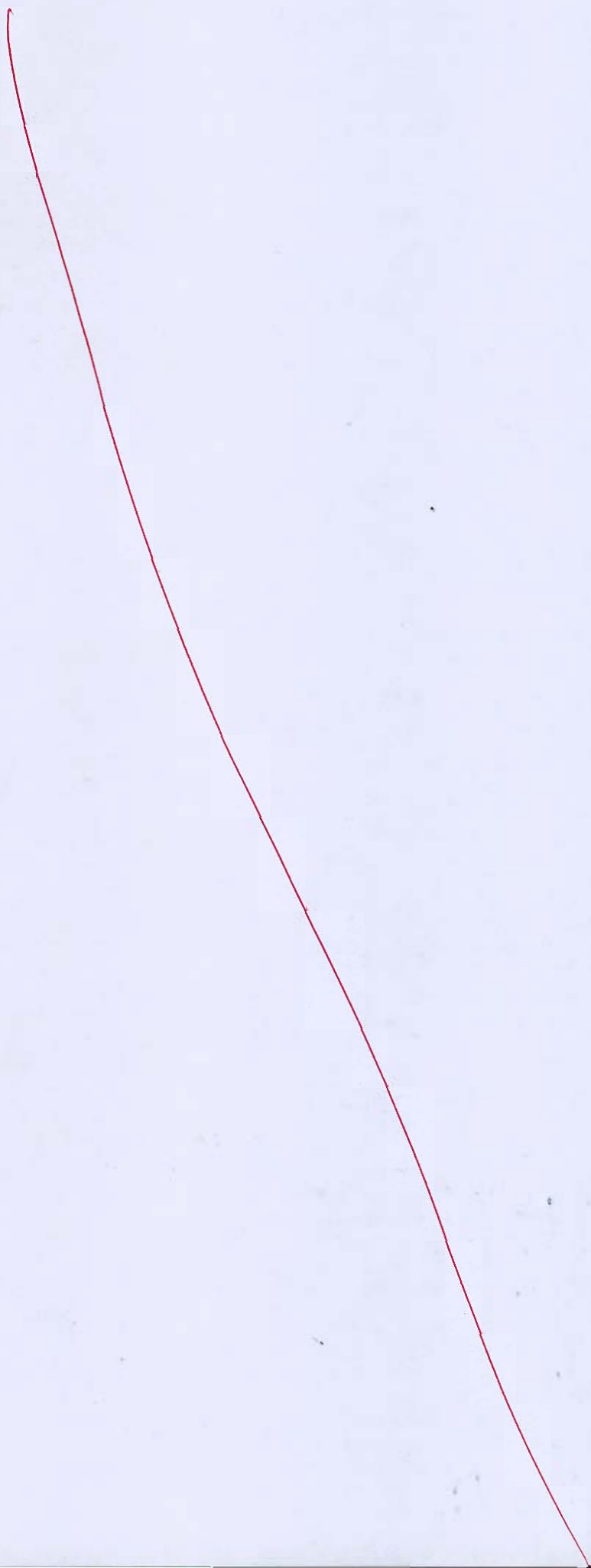
Ans oxide thickness (t_{ox}) = 1.205 μm

Solution (i)

In VLSI-technology, two types of scaling used. which is given below

(1) constant field scaling

(2) constant voltage scaling.



- Q.6 (c) (i) Consider the following set of processes, with the arriving time and length of the CPU burst given in milliseconds:

Process	Arrival Time	Burst Time
P_1	0	6
P_2	1	4
P_3	2	3
P_4	3	1
P_5	4	2
P_6	5	1

Draw the Gantt chart and compute the average process waiting time using shortest remaining time first (SRTF) scheduling algorithm.

- (ii) What are the differences between concurrency and parallelism in the context of processes in operating systems?

[15 + 5 marks]

Solution Let Quantum time (T_q) = 1 ms

criteria = Burst time

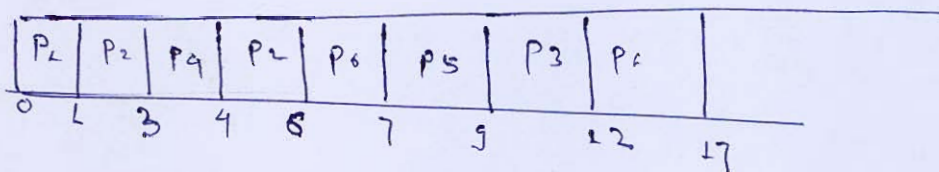
time	process	Burst
$t=0$	P_1	5
$t=1$	P_2	

time	process
$t=0$	P_1
$t=1$	P_1, P_2
$t=2$	P_1, P_2, P_3
$t=3$	P_1, P_2, P_3, P_4
$t=4$	P_1, P_2, P_3, P_5
$t=5$	P_1, P_2, P_3, P_5

$P_1 \rightarrow 5$
 $P_2 \rightarrow 4$
 $P_3 \rightarrow 3$
 $P_4 \rightarrow 1$
 $P_5 \rightarrow 2$
 $P_6 \rightarrow 1$

Using SJRF

Gantt chart



process	Arrival time (AT)	Burst time (BT)	Completion time (CT)	Turn around time (TAT)	Waiting time (WT)
P1	0	6	17	17	11
P2	1	4	6	5	1
P3	2	3	12	10	2
P4	3	1	4	1	0
P5	4	2	9	5	3
P6	5	2	7	2	1

$$\text{Turn around time (TAT)} = \text{CT} - \text{AT}$$

$$\text{Waiting time} = \text{TAT} - \text{BT}$$

$$\text{Average waiting time (Tavg)} = \frac{11 + 1 + 2 + 0 + 3 + 1}{6}$$

$$= 23/6$$

$$= 3.833 \text{ ms}$$

$$\text{Ans } \boxed{\text{Tavg} = 3.833 \text{ ms}}$$

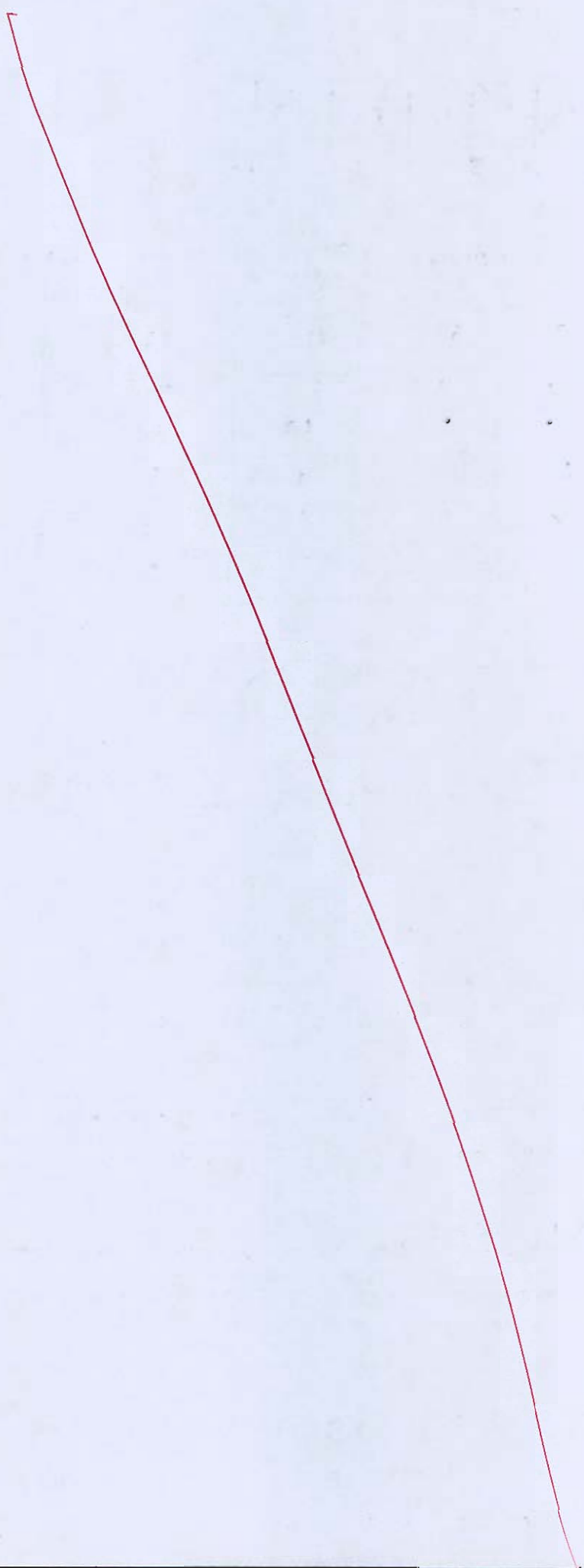
(ii) Difference between concurrency and parallelism is given below:-

Concurrency:-

In concurrency, operating system takes new process, only completion of old process.

Parallelism:- operating system, take new input

before completion of old input. Hence operating system runs new input along with old input.



7 (a) (i) Explain the following two priority based interrupt handling methods:

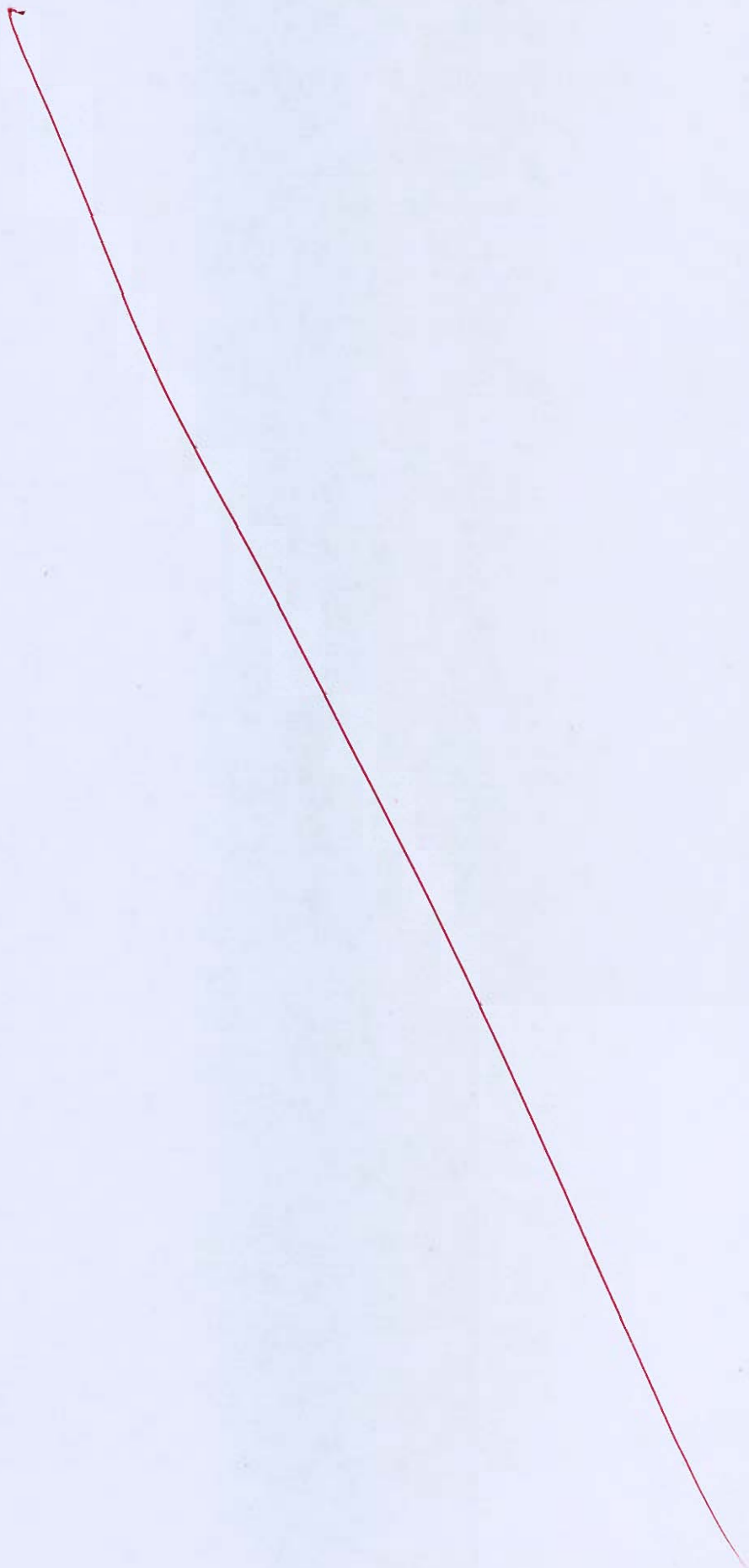
1. Polling
2. Daisy chaining

(ii) Find whether the given schedules are conflict serializable or not.

$S_1 : W_2(x), W_1(x), R_3(x), W_2(y), R_3(y), R_3(z), R_2(x)$

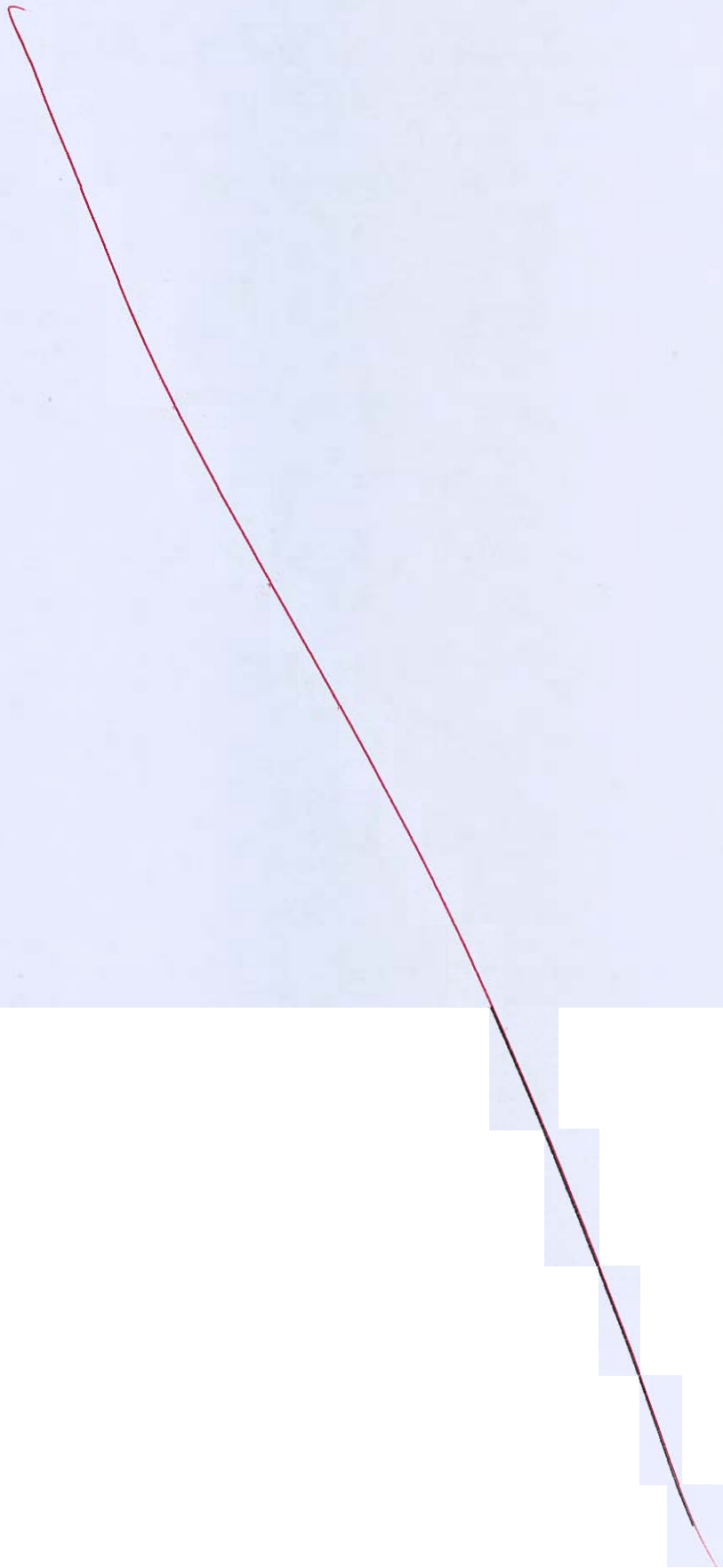
$S_2 : R_3(z), W_2(x), W_2(y), R_1(x), R_3(x), R_2(x), R_3(y), W_1(z)$

[12 + 8 marks]



- (b) (i) Explain briefly about following terms related to design quality in VLSI Chip Design:
1. Testability
 2. Yield
 3. Manufacturability
 4. Reliability
- (ii) Consider a cellular system which consists of 34 cells with the cell radius as 1.4 km. A total frequency bandwidth is capable of supporting 343 traffic channels. Find what geographical area (in km) can be covered and the number of channels available per cell. What is the total number of concurrent calls that can be handled? [Assume reuse factor of $N = 7$]

[10 + 10 marks]



2.7 (c) Describe in detail the layered architecture of TCP/IP protocol and define type of address used at each layer.

[20 marks]



- 2.8 (a) (i) Implement a Binary to Gray code converter using PLA.
(ii) Define the following parameters related to Testability of a circuit:
1. Controllability
 2. Observability

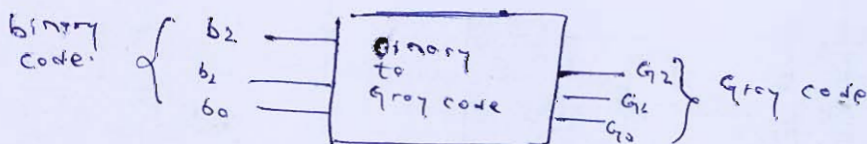
[14 + 6 marks]

Solution (i) - 6

Let consider '3' bit binary to Gray code converter using PLA.

PLA (programmable logic array)

Block diagram



Truth table

Decimal	b ₂	b ₁	b ₀	G ₂	G ₁	G ₀
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	0
3	0	1	1	0	1	1
4	1	0	0	1	0	0
5	1	0	1	1	0	1
6	1	1	0	1	1	0
7	1	1	1	1	1	1

$$G_2 = \Sigma m(4, 5, 6, 7), \quad G_1 = \Sigma m(2, 3, 5)$$

$$G_0 = \Sigma m(1, 2, 5, 6)$$

Simplification using K-map

G_2

	$b_2 b_1$	00	01	11	10
b_2	0				
1		1	1	1	1

$G_2 = b_2$

G_1

	$b_2 b_1$	00	01	11	10
b_2	0			1	1
1		1	1		

$$G_1 = \bar{b}_2 b_1 + b_2 \bar{b}_1$$

$$G_1 = b_2 \oplus b_1$$

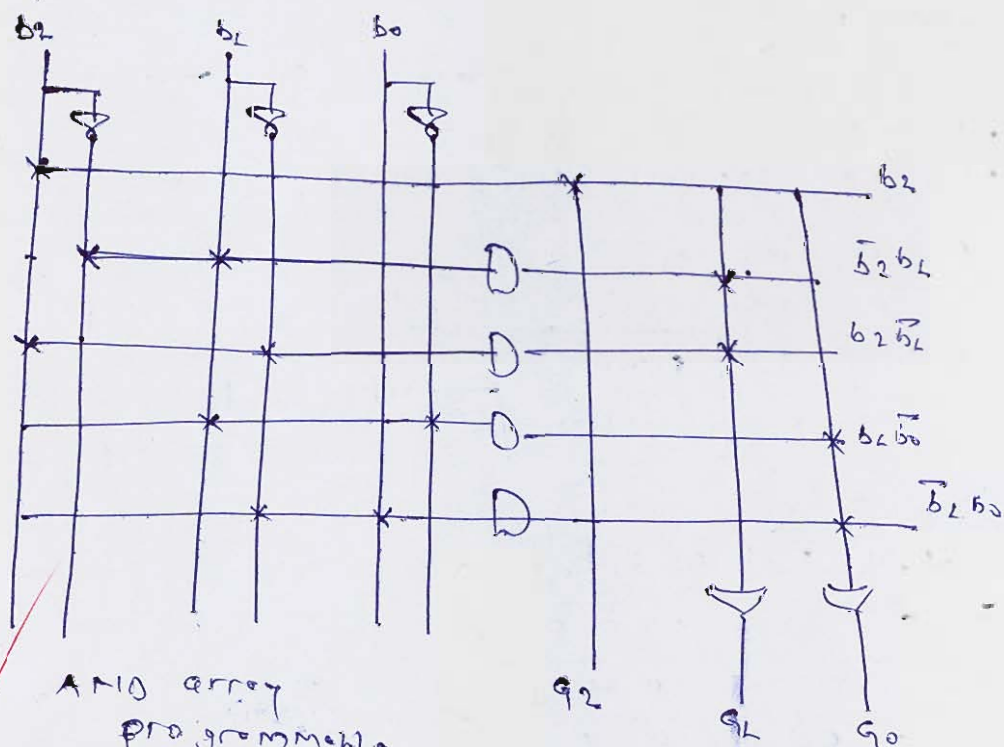
G_0

	$b_2 b_1$	00	01	11	10
b_2	0		1		1
1		1			1

$$G_0 = b_2 \bar{b}_1 + \bar{b}_2 b_1$$

$$G_0 = b_2 \oplus b_1$$

In PLA both AND array and OR-array both are programmable.



AND array
programmable

OR-array programmable

Binary to Gray code conversion using
PLA

Solution (ii)

controllability -

In testability of circuit, controllability is define in such a way, that if it is possible to set any node logic '1' at short period of time, then such circuit called controllable circuit.

② Observability -

If it is possible to investigate all nodes in short period of time called observability of circuit.

- Q.8 (b) (i) Explain the following components of Entity-Relationship Model (ER Model) of DBMS:
1. Entity
 2. Attributes
 3. Relationship
 4. Domain
- (ii) Consider 8-way set associative cache of 64 KB organised into a 32B blocks. CPU generates 28 bit physical address to access the data. The cache controller contains tag information along with 2 valid bits, 2 update bits and 3 replacement bits along with the bits needed to identify the memory block mapped in the cache. Find the tag space in the line and tag directory size.

[8 + 12 marks]

Solution (i) - 8Entity:- Let $A \rightarrow B$ (A relation to B)

Entt. Entity in DBMS system relates to objects of system.

Attributes:-

Attributes, is unique quality of name in DBMS system. So that any object/entity is identified.

Relationship:-

It is an established relationship between one entity of DBMS system to other entity of DBMS system.

Domain:- Range of entity sets.Solution (ii) - 8

given set associative cache.

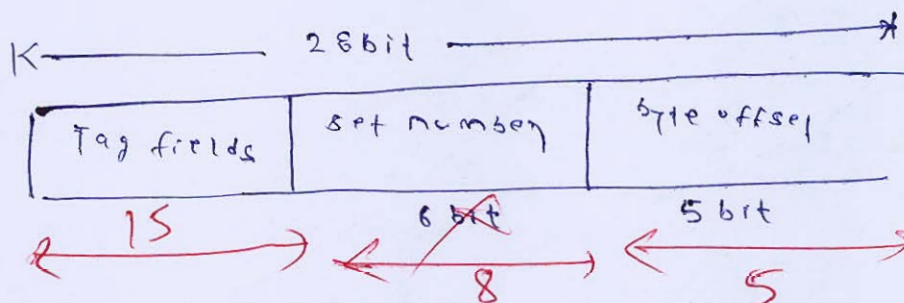
Number of sets (K) = 8

cache size = 64 KB

block size = 32 B

Physical address size = 28 bit

cpu generates main memory address. And this address is divided into '3' parts as shown



Number of bits for byte offset = $\log_2 32 = 5 \text{ bit}$

$$\begin{aligned} \text{Number of cache blocks} &= \frac{\text{cache size}}{\text{block size}} \\ &= \frac{64 \text{ KB}}{32 \text{ B}} = \frac{2^{16} \times 8}{2^5 \text{ B}} \end{aligned}$$

Number of cache blocks = 29

$$\begin{aligned} \text{Number of sets} &= \frac{\text{Number of cache blocks}}{\text{Number of sets}} \\ &= \frac{29}{8} \end{aligned}$$

Number of set = 26

Number of bits for set = $\log_2 6 = 6 \text{ bit}$

$$\begin{aligned} \text{Tag field bits} &= 28 - (6 + 5) \\ &= 17 \text{ bit} \end{aligned}$$

Ans (tag space = 17 bits)

$$\begin{aligned} \text{Tag directory size} &= \text{Number of cache blocks} \times (\text{Tag bits} + \text{valid bit} + \text{update bit} + \text{replacement bit}) \\ &= 2^9 \times (17 + 2 + 2 + 3) \\ &= 2^9 \times 24 \text{ bits} \end{aligned}$$

Ans | Tag directory size = $2^9 \times 24 \text{ bits}$

- Q.8 (c)
- (i) Obtain the binary notation and also determine the network address for the following classful IP addresses (Assume that subnetting is not being used):
1. 23.56.89.12
 2. 133.45.78.65
 3. 201.150.47.19
- (ii) Determine and explain clearly the address class for the following IP addresses:
1. Binary: 11000000 10101000 00000001 00000001
 2. Hexadecimal : 8F 7C 2A 1B
 3. Dotted Decimal: 172.31.0.1

[10 + 10 marks]

Solution - 8

This is given IP addresses are of IPv4. Hence it is IPv4 is 32 bit. There are 4 blocks of 8 bits.

- (i) (1) IP address
23.56.89.12

This address is class-A address.
Since class A lies between (1 to 127)

(A) 133: 45: 78: 65

This is class-B address. Since class-B address lies between (128 to 191)

(B) 201: 250: 47: 19

This is class-C address. Since class-C address lies between (192 to 223).

Solution/iii (2)

Binary: 11000000 10101000 00000001 00000001

Since IP-4 is 32 bit long address.

Hence it is divided into 4 blocks of 8 bit each.

192: 168: 1: 1

This is class-C address. class-C address lies between (192 to 223)

(1) (2) 8F 7C 2A 1B

converting it into decimal equivalent

143: 124: 42: 27 (IP address)

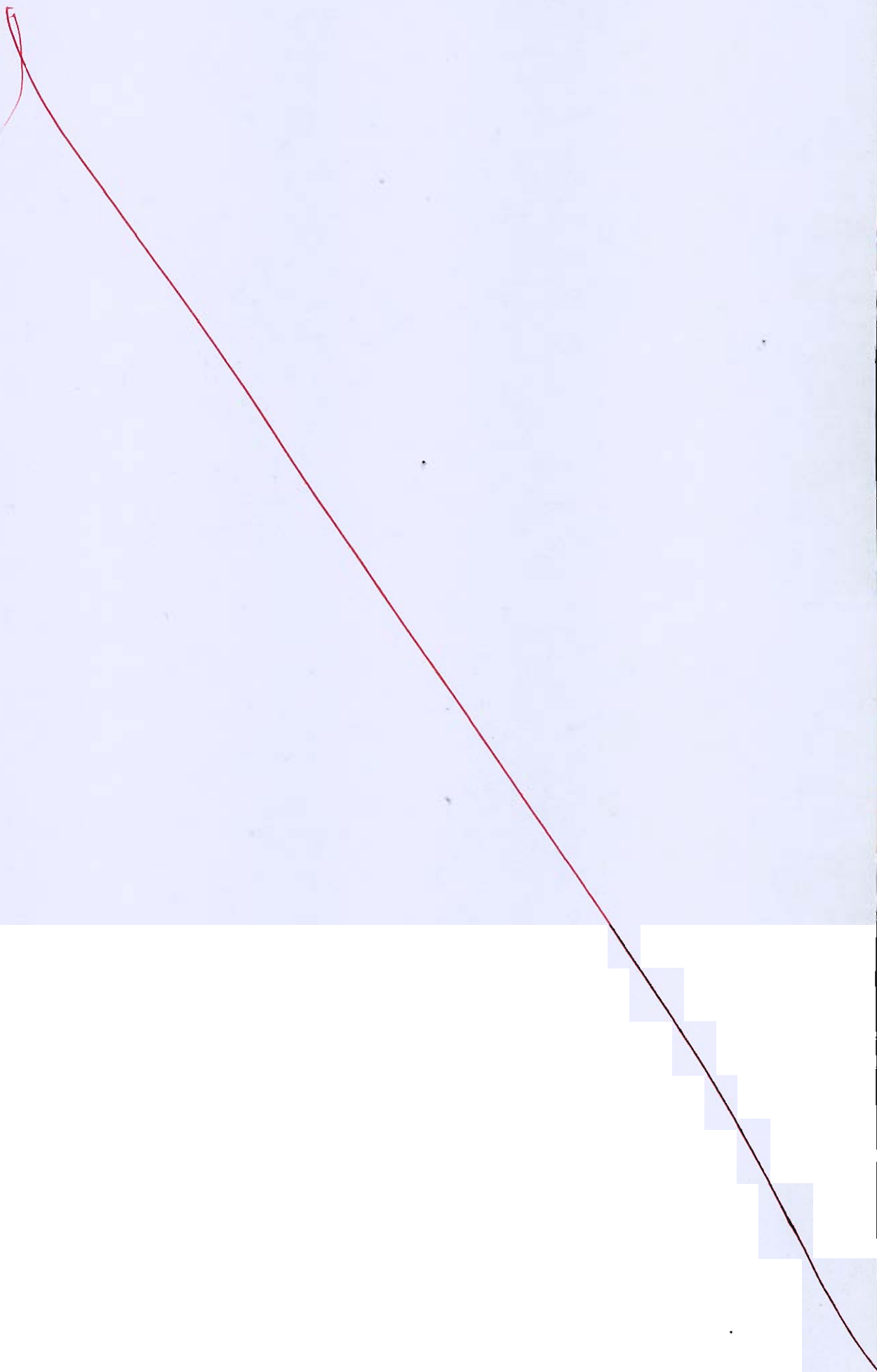
This is class-B address.

Since class-B address lies (128 to 191)

(3) 172: 31: 0: 1

This is class-A address.

Space for Rough Work



space for the

$$\frac{L n_1}{c} - \frac{L n_2}{c n_2}$$

$$\frac{L n_1}{c} \left(1 - \frac{n_1}{n_2} \right)$$

$$7.69 \times 10^{-11} \text{ v } 10 \times 10^{-9}$$

$\frac{2}{4/51}$
 $\frac{297}{-}$

2/10/20

$$\frac{t_{0.1} - A t_{0.2} \leq D(1+2)}{\sqrt{D/2}}$$

from
from
PAL
from

~~p_n~~

$$\begin{array}{r} 9 \times 9 \times 48 \\ \hline 2 \times 1 \times 1 \times 2 \\ \hline 18.73 \\ \hline 17.3 \end{array}$$

26127
641228

C4P

$p \geq E_{b^*}$
 $(c \geq p \leq f)$
 E

108

(F-1/KTS)

A hand-drawn diagram consisting of two rows of symbols. The top row contains three symbols: a circle with a dot inside, a solid black oval, and two parallel vertical lines. The bottom row contains four symbols: a vertical line with a small circle at its base, a circle with a dot inside, a solid black oval, and two parallel vertical lines.

1011
1012
1013
1014

23 25 27
8 10 12 13

100
1140
110
114

12/10/11

9 10
3 4
C 1 2
C 1 3
C 1 4
7 1

5 pages

2426x7
10126x8