MADE EASY

Leading Institute for ESE, GATE & PSUs

· Try to avoid calculation mistake

ESE 2025 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

Electrical Engineering

Test-5 : Basic Electronics Engineering + Computer Fundamentals + Electromagnetic Field Theory

Name : ....

Roll No :

Test Centres			Student's Signature
Delhi ☑	Bhopal ☐	Jaipur ☐	
Pune ☐	Kolkata ☐	Hyderabad ☐	

Instructions for Candidates

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. There are Eight questions divided in TWO sections.
3. Candidate has to attempt FIVE questions in all in English only.
4. Question no. 1 and 5 are compulsory and out of the remaining THREE are to be attempted choosing at least ONE question from each section.
5. Use only black/blue pen.
6. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
7. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
8. There are few rough work sheets at the end of this booklet. Strike off these pages after completion of the examination.

FOR OFFICE USE	
Question No.	Marks Obtained
Section-A	
Q.1	41
Q.2	46
Q.3	
Q.4	46
Section-B	
Q.5	39
Q.6	44
Q.7	
Q.8	
Total Marks Obtained	216

Signature of Evaluator: Sourabh Kumar

Cross Checked by: ....

→ Read instruction carefully.

IMPORTANT INSTRUCTIONS

CANDIDATES SHOULD READ THE UNDERMENTIONED INSTRUCTIONS CAREFULLY. VIOLATION OF ANY OF THE INSTRUCTIONS MAY LEAD TO PENALTY.

DONT'S

1. Do not write your name or registration number anywhere inside this Question-cum-Answer Booklet (QCAB).
2. Do not write anything other than the actual answers to the questions anywhere inside your QCAB.
3. Do not tear off any leaves from your QCAB, if you find any page missing do not fail to notify the supervisor/invigilator.
4. Do not leave behind your QCAB on your table unattended, it should be handed over to the invigilator after conclusion of the exam.

DO'S

1. Read the Instructions on the cover page and strictly follow them.
2. Write your registration number and other particulars, in the space provided on the cover of QCAB.
3. Write legibly and neatly.
4. For rough notes or calculation, the last two blank pages of this booklet should be used. The rough notes should be crossed through afterwards.
5. If you wish to cancel any work, draw your pen through it or write "Cancelled" across it, otherwise it may be evaluated.
6. Handover your QCAB personally to the invigilator before leaving the examination hall.

Section A : Basic Electronics Engineering + Computer Fundamentals + Electromagnetic Field Theory

Q.1 (a) If $\vec{J} = \frac{1}{r^3}(2\cos\theta\,\hat{a}_r + \sin\theta\,\hat{a}_\theta)$ A/m², calculate the current passing through

(i) a hemispherical shell of radius 20 cm, $0 < \theta < \frac{\pi}{2}$, $0 < \phi < 2\pi$.

(ii) a spherical shell of radius 10 cm.

[12 marks]

$$J = \frac{1}{r^3}\left(2\cos\theta\, \hat{a_r} + \sin\theta\, \hat{a_\theta}\right) \text{ A/m}^2$$

(i) $r = 20$ cm, $0 < \theta < \frac{\pi}{2}$, $0 < \phi < 2\pi$, Hemispherical shell

$$I = \iint J \cdot ds$$

$$I = \iint \frac{1}{r^3}\left(2\cos\theta\, \hat{a_r} + \sin\theta\, \hat{a_\theta}\right) \cdot r^2 \sin\theta\, d\theta\, d\phi\, \hat{a_r}$$

$$I = \iint \frac{1}{r^3}(2\cos\theta) \cdot r^2 \sin\theta\, d\theta\, d\phi$$

$$I = \frac{1}{r}\int_0^{2\pi}\int_0^{\pi/2} \sin 2\theta\, d\theta\, d\phi$$

$$I = \frac{1}{r}\frac{(\cos 2\theta)_{\pi/2}^{0}}{2} \times (\phi)_0^{2\pi}$$

$$I = \frac{1}{20\times10^{-2}\times 2} 2\pi \times 2$$

$$\boxed{I = 10\pi = 31.42 \text{ A}}$$

(ii) Spherical shell $I = \iint J \cdot ds$

$$I = \iint \frac{1}{r^3}\cdot\left(2\cos\theta\, \hat{a_r} + \sin\theta\, \hat{a_\theta}\right) \cdot r^2 \sin\theta\, d\theta\, d\phi\, \hat{a_r}$$

Here, $r = 10$ cm, $\boxed{0 < \theta < \pi,}$ $0 < \phi < 2\pi$

Do not write in this margin

$$I = \frac{1}{r}\int_0^{2\pi}\int_0^{\pi} \sin 2\theta \, d\theta \, d\phi$$

$$I = 10 \times 2\pi \; (\cos 2\theta)_{\pi}^{0}$$

$$\boxed{I = 0}$$

Good Approach

11

Q.1 (b) A charge distribution with spherical symmetry has density $\rho_v = \begin{cases} \frac{\rho_0 r}{R}, & 0 \le r \le R \\ 0, & r > R \end{cases}$.

Determine $\vec{E}$ everywhere.

[12 marks]

$$\rho_v = \begin{pmatrix} \frac{\rho_0 r}{R} , & 0 \le r \le R \\ 0 , & r > R \end{pmatrix}$$

<u>By Gauss law</u>

$$Q = \iint D \cdot dS = \iiint \rho_v \cdot dv$$

<u>In spherical coordinates</u>

$$dv = r^2 \sin\theta \, dr \, d\theta \, d\phi$$

1) $0 \le r \le R$

$$\iint D \cdot dS = \iiint \rho_v \cdot dv$$

$$\iint D_r \cdot dS = \int_0^{2\pi}\int_0^{\pi}\int_0^{r} \frac{\rho_0 r}{R} \times r^2 \sin\theta \, dr \, d\theta \, d\phi$$

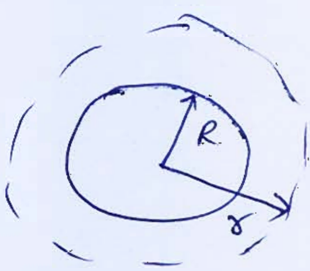
$$D_r \times 4\pi r^2 = \frac{\rho_0}{R} \int_0^r r^3 dr \times 4\pi$$

$$D_r = \frac{\rho_0}{r^2 R} \times \frac{r^4}{4} \Rightarrow \boxed{D_r = \frac{\rho_0 r^2}{4R}}$$

$$D_r = \varepsilon_0 E_r$$

$$\boxed{\vec{E}_r = \frac{\rho_0 r^2}{4R\varepsilon_0} \hat{a}_r}$$

2) $r > R$



$$\iint D \cdot ds = \iiint \rho_v \, dV$$

$\boxed{\rho_v = 0}$ for $r > R$

$D = 0$

$\boxed{E = 0}$

6

Q.1 (c) Consider a network connecting two systems located 3000 kilometers apart. The bandwidth of the network is 1.544 Mbps. The propagation speed of the media is 0.16×10^6 km/sec. It is needed to design a Go-Back-N sliding window protocol for this network. The average frame size is 64 B. The network is to be used to its full capacity. Assume processing delays at nodes are negligible. Calculate the window size.

[12 marks]

Given, $l = 3000$ km

$BW = 1.544$ Mbps

$v = 0.16 \times 10^6$ km/sec.

frame size = 64B

Transmission time

$t_{tr} = \frac{.1}{1.544 \times 10^6} = 0.647 \mu sec.$

Propagation delay

$t_{pd} = \frac{l}{v} = \frac{3000}{0.16 \times 10^6} = 0.01875$ sec.

for Go back-N sliding

$t_r = 2 t_{pd} = 0.0375$ sec.

$T = t_{tr} + 2t_{pd}$

$T =$

Window size = $(64B) \times \frac{1}{T}$

=

5

Q.1 (d) What does "computer architecture" term means in regards to computing system? Enumerate properties of reduced instruction set computer architecture.

[12 marks]

Computer Architecture is defined as the interconnection of different components present in the computer organization. Computer Architecture basically has several parts connected together to do their specific tasks.
Van Neuman architecture was the first computer architecture where single memory was present.

Properties of Reduced Instruction Set Computer Arch.

1) It uses very less instruction set
2) It uses more registers
3) It requires less addressing modes
4) Pipelining is successfull in RISC
5) Cycle per Instruction i.e CPI = 1
6) It uses hardwired control unit
7) Less flexible control unit
8) ex. used in ARM processor.

8

Q.1 (e) Determine the curl of the following vector fields:

(i) $\vec{A} = \rho z^2 \hat{\rho} + \rho \sin^2\phi\,\hat{\phi} + 2\rho z \sin^2\phi\,\hat{z}$, in circular cylindrical coordinate system.

(ii) $\vec{B} = r\hat{r} + r\cos^2\theta\,\hat{\phi}$, in spherical coordinate system.

[6 + 6 marks]

(i) $A_\rho = \rho z^2 \quad A_\phi = \rho \sin^2\phi \quad A_z = 2\rho z \sin^2\phi$

In cylindrical system

$$\nabla \times A = \frac{1}{\rho}\begin{vmatrix} \hat{a_\rho} & \rho\,\hat{a_\phi} & \hat{a_z} \\ \frac{\partial}{\partial \rho} & \frac{\partial}{\partial \phi} & \frac{\partial}{\partial z} \\ \rho z^2 & \rho^2 \sin^2\phi & 2\rho z \sin^2\phi \end{vmatrix}$$

$$= \frac{1}{\rho}\Big[\hat{a_\rho}(2\rho z \times 2\cos\phi\sin\phi - 0) - \rho\hat{a_\phi}(2z\sin^2\phi - 2\rho z) + \hat{a_z}(2\rho \times \sin^2\phi - 0)\Big]$$

$$= (2\sin 2\phi \cdot z)\hat{a_\rho} - (2z\sin^2\phi - 2\rho z)\hat{a_\phi} + \hat{a_z}\sin^2\phi \times 2\rho$$

$$\boxed{\nabla \times A = 2z\sin 2\phi\,\hat{a_\rho} - 2z(\sin^2\phi - \rho)\hat{a_\phi} + \hat{a_z}\sin^2\phi \times 2\rho}$$

(ii) In spherical coordinate system

$B_r = r \quad B_\theta = 0 \quad B_\phi = r\cos^2\theta$

$$\nabla \times B = \frac{1}{r^2 \sin\theta}\begin{vmatrix} \hat{a_r} & r\hat{a_\theta} & \hat{a_\phi}\, r\sin\theta \\ \frac{\partial}{\partial r} & \frac{\partial}{\partial \theta} & \frac{\partial}{\partial \phi} \\ r & 0 & r^2 \sin\theta\cos^2\theta \end{vmatrix}$$

$$\nabla \times B = \frac{1}{r^2\sin\theta}\Big[\hat{a_r}\big(r^2(\cos^3\theta - 2\cos\theta\sin^2\theta)\big) - r\hat{a_\theta}(2r\sin\theta\cos^2\theta) + \hat{a_\phi}\, r\sin\theta \times 0\Big]$$

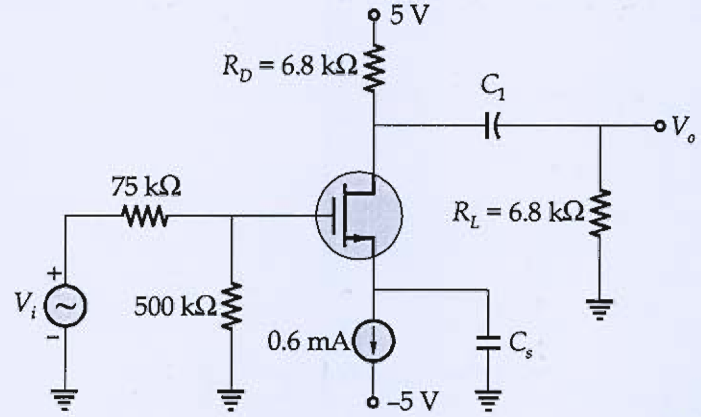
$$\nabla \times B = a_{\hat{r}}\left(\frac{\cos^3\theta - 2\cos\theta\sin^2\theta}{\sin\theta}\right) - 2a_{\hat{\theta}}\cos^2\theta$$

$$\nabla \times B = \left(\frac{\cos^3\theta}{\sin\theta} - 2\cos\theta\sin\theta\right) a_{\hat{r}} - 2a_{\hat{\theta}}\cos^2\theta$$

Good Approach

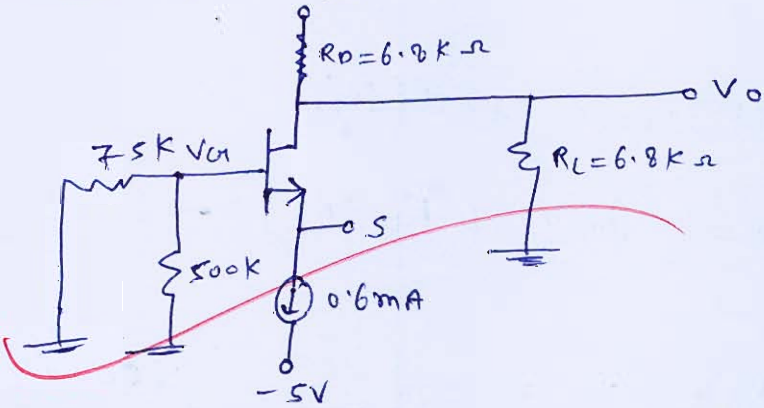
11

Q.2 (a) Determine the small signal voltage gain of the circuit shown in below figure having parameters $V_T = 0.8$ V, $k = \dfrac{\mu_n C_{ox} W}{2L} = 1.2$ mA/V², $\lambda = 0$. Also calculation gate-to-source voltage (V_{GSQ}).



[20 marks]

DC Analysis → All capacitors open & ac sources zero



$I_D = 0.6$ mA, MOFET is in saturation mode

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 \rightarrow (1)$$

$$0.6 = 1.2(V_{GS}-0.8)^2$$

$$0.707 = V_{GS}-0.8$$

$$\boxed{V_{GS} = 1.507} \text{ volts}$$

Now,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

from equation (1)

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_n C_{ox} W}{2L} \times 2(V_{GS}-V_T)$$

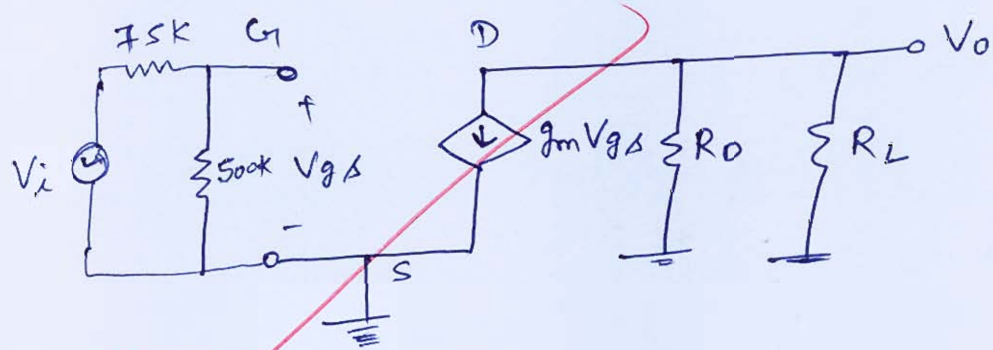
$g_m = 1.2 \times 2(1.507 - 0.8)$

$g_m = 1.69$

AC Analysis → Drawing small signal model

Capacitor → short circuited

dc sources → off



From the above small signal model

$V_o = -g_m V_{gs}(R_D \| R_L) \rightarrow (1)$

From input side

$V_{gs} = V_i \times \frac{500}{500+75} = \frac{500V_i}{575} \rightarrow (2)$

from (1) & (2)

$V_o = -g_m \times \frac{500\,V_i}{575} \times (R_D \| R_L)$

$A_v = \frac{V_o}{V_i} = -g_m \times \frac{500}{575} \times (6.8 \| 6.8k\Omega)$

$A_v = -1.69 \times \frac{500}{575} \times 3.4$

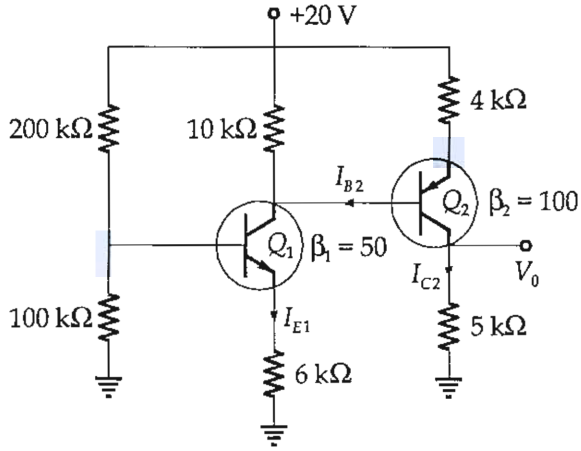
$\boxed{A_v \simeq -5}$

↳ small signal voltage gain

18

Good Approach

Q.2 (b) Consider the transistor configuration shown below.



Determine:

(i) Base current of transistor, Q_2.

(ii) Collector current of transistor, Q_2.

(iii) Emitter current of transistor, Q_1.

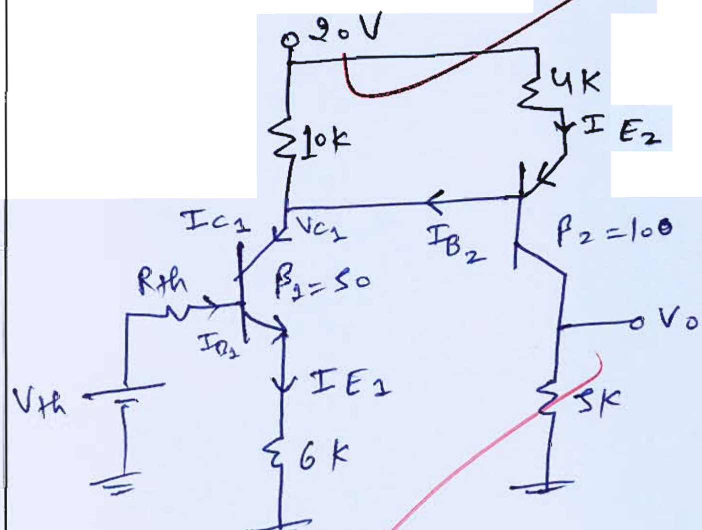
(iv) Output voltage, V_0.

[20 marks]

Applying thevenin equivalent at input/base of Q_1 transistor.

$$V_{th} = 20 \times \frac{100}{300} = 6.67\,V$$

$$R_{th} = 200 \| 100\,k\Omega = \frac{200 \times 100}{300} = 66.67\,k\Omega$$



KVL in Q_1

$$-V_{th} + I_{B1} R_{th} + 0.7 + 6 I_{E_1} = 0$$

$$I_{B1} \times 66.67 + 6 \times 51 \times I_{B1} = 5.97$$

$$\boxed{I_{B1} = 0.016\ mA}$$

So Emitter Current of transistor Q_1

$I_{E1} = (1+\beta_1) I_{B1} = 51 \times 0.016$

$I_{E1} = 0.816\ mA$

$I_{C1} = I_{E1} - I_{B1} = 0.8\ mA$

Again KVL in upper loop

$-20 + 4I_{E2} + 0.7 + 10(I_{B2} - I_{C1}) = 0$

$4(1+\beta_2) I_{B2} + 10 I_{B2} - 8 = 20 - 0.7$

$I_{B2} = 0.0659\ mA$

↳ Base current of Q_2

10

$I_{C2} = \beta_2 I_{B2}$

$I_{C2} = 6.59\ mA$

↳ Collector current of Q_2

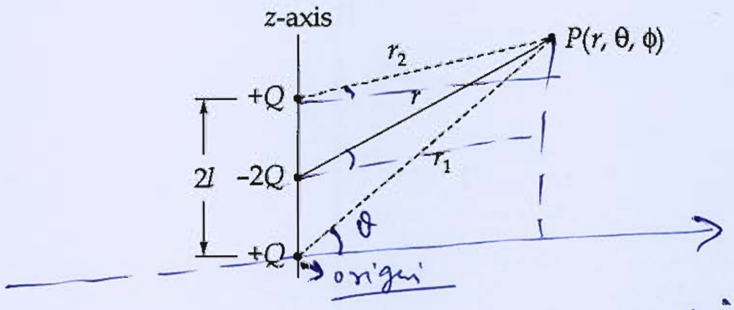
$V_o = 5 I_{C2}$

$V_o = 5 \times 6.59$

$V_o = 32.97$ Volts

↳ output voltage

Q.2 (c) (i) Figure below shows a linear quadrupole arrangement, with charges +Q, –2Q and +Q disposed as indicated. Show that the potential due to this quadrupole at a large distance 'r' in comparison with the spacing '$2l$' is $V = \frac{Ql^2}{4\pi\varepsilon_0 r^3}(3\cos^2\theta - 1)$.



[12 marks]

Assume the origin as shown in figure

$+Q\,(0,0,0)$
$-2Q\,(0,0,l)$
$+Q\,(0,0,2l)$
} In cartesian system

$V_P = V_1 + V_2 + V_3$

$V_P = \frac{KQ}{r_1} + \frac{K(-2Q)}{r} + \frac{KQ}{r_2} \rightarrow (1)$

for +Q

$\cos\theta = \frac{\sqrt{r_1^2 - 4l^2}}{r_1} \rightarrow (3)$

for −2Q

$\cos\theta = \frac{\sqrt{r^2 - l^2}}{r} \rightarrow (2)$

for +Q

$\cos\theta \Rightarrow$ same as (i)

from (2)

$\cos^2\theta = \frac{r^2 - l^2}{r^2}$

$r^2\cos^2\theta = r^2 - l^2$

from (3)

$$\cos^2\theta = \frac{r_1^2 - 4l^2}{r_1^2}$$

$$3\cos^2\theta - 1 = \frac{3r^2 - 3l^2}{r^2} - 1$$

$$= -\frac{3l^2}{r^2}$$ → using this V formula

$$V = \frac{KQ}{r}(3\cos^2\theta - 1)$$

$$V = \frac{KQ}{r} \times -\frac{l^2}{r^2}(3\cos^2\theta - 1)$$

$$V = \frac{Ql^2}{4\pi\varepsilon_0 r^3}(3\cos^2\theta - 1)$$

11

Good Approach

Do not write in this margin

Q.2 (c) **(ii)** Region $y \leq 0$ consists of a perfect conductor while $y \geq 0$ is a dielectric medium ($\varepsilon_r = 2$). If there is a surface charge of 2 nC/m^2 on the conductor, determine $\vec{E}$ and $\vec{D}$ at $A(3, -2, 2)$ and $B(-4, 1, 5)$.

[8 marks]

$\rho_s = 2\, nC/m^2$

$\varepsilon_r = 2$ — $y > 0$

y-axis

$\varepsilon_r = 1$ — $y < 0$

at point A (3, −2, 2)

$y = -2$ means $\boxed{y < 0}$

$\vec{D} = \rho_s = 2\, nC/m^2\, \hat{a}_y$

$E = \frac{D}{\varepsilon_0} = \frac{2 \times 10^{-9}}{\varepsilon_0} = \frac{2 \times 10^{-9}}{8.854 \times 10^{-12}}$

$\boxed{E = 225.88\, \hat{a}_y\, V/m}$

at point B (−4, 1, 5)

$y = 1$ means $\boxed{y > 0}$

$D = \rho_s = 2\, nC/m^2\, \hat{a}_y$

$E = \frac{D}{\varepsilon_0 \varepsilon_r} = \frac{2 \times 10^{-9}}{8.854 \times 10^{-12} \times 2}$

$\boxed{E = 112.94\, \hat{a}_y\, V/m}$

7

Good Approach

Q.3 (a) Two extensive homogeneous isotropic dielectric meet on plane $z = 0$. For $z > 0$, $\varepsilon_{r1} = 4$ and for $z < 0$, $\varepsilon_{r2} = 3$. A uniform electric field $\vec{E}_1 = 5\hat{a}_x - 2\hat{a}_y + 3\hat{a}_z$ kV/m exists for $z \geq 0$.

Find:

(i) $\vec{E}_2$ for $z \leq 0$.

(ii) The angles $\vec{E}_1$ and $\vec{E}_2$ make with the interface.

(iii) The energy densities (in J/m^3) in both dielectrics.

(iv) The energy within a cube of side 2 m centered at (3, 4, –5).

[20 marks]

Q.3 (b) A solid conductor of circular cross-section with a radius of 5 mm has a conductivity that varies with radius, the conductor is 20 m long and there is a potential difference of 0.1 V dc between its two ends. Within the conductor $\vec{H} = 10^5 \rho^2 \hat{a}_\phi$ A/m.

(i) Find conductivity σ.

(ii) Determine the resistance between the two ends.

[20 marks]

Do not write in this margin

Do not write in this margin

Q.3 (c) **(i)** Write a 'C' program to check whether a character is a vowel or a consonant.

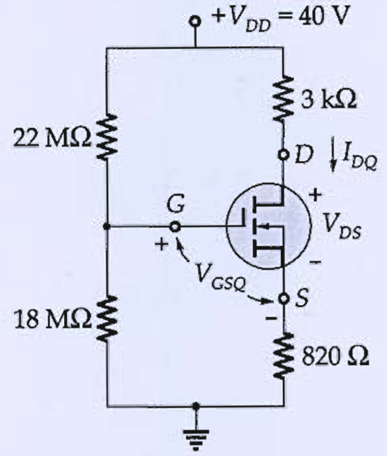
(ii) Differentiate between the following in C programming:

1. Do-while loop and while loop.

2. Iteration and recursion.

[20 marks]

Q.4 (a) Determine I_{DQ}, $V_{GS\,Q}$ and V_{DS} for the circuit shown in figure,



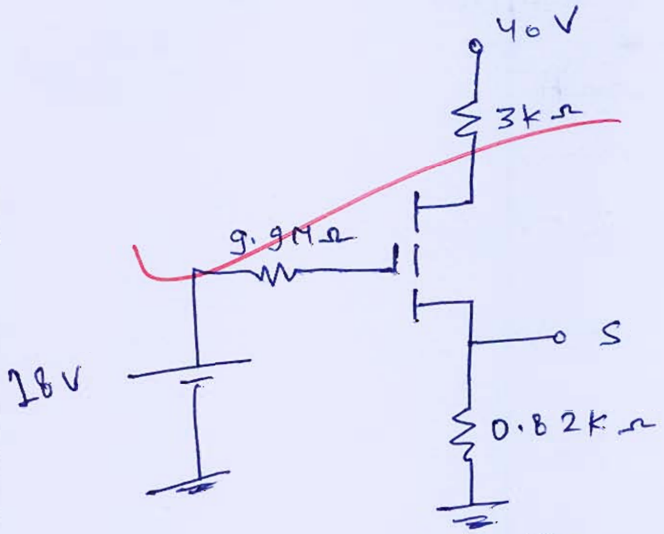
$V_{GS\,(Th)} = 5$ V, $I_D(\text{on}) = 3$ mA at $V_{GS}(\text{on}) = 10$ V.

[20 marks]

Applying thevenin equivalent at input of gate.

$$V_{th} = 40 \times \frac{18}{18+22} = 18\text{ V}$$

$$R_{th} = \frac{18 \times 22}{18+22} = 9.9\text{ M}\Omega$$



From the given values

$V_{th} = 5$V $\quad I_D = 3$mA $\quad V_{GS} = 10$V

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_t}\right)^2$$

$$3 = I_{DSS}\left(1 - \frac{10}{5}\right)^2$$

$$\boxed{I_{DSS} = 3\text{mA}}$$

Now, from the circuit drawn

$V_G = 18V \quad V_S = 0.82 I_D$

$V_{GS} = 18 - 0.82 I_D$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_T}\right)^2$

$I_D = 3\left(1 - \frac{18 - 0.82 I_D}{5}\right)^2$

$\frac{25 I_D}{3} = (5 - 18 + 0.82 I_D)^2$

$25 I_D = (0.82 I_D - 13)^2$

$0.672 I_D^2 + 169 - 21.32 I_D = 25 I_D$

$0.672 I_D^2 - 46.32 I_D + 169 = 0$

$\boxed{I_D = 3.86 mA}$

12

$V_{GS} = 18 - 0.82 \times 3.86$

$\boxed{V_{GS} = 14.83 V}$

Now, KVL

$-40 + 3I_D + V_{DS} + 0.82 I_D = 0$

$V_{DS} = 40 - 3.82 I_D$

$V_{DS} = 40 - 3.82 \times 3.86$

$\boxed{V_{DS} = 25.25 V}$

Q.4 (b) **(i)** Write a program in C language to sort the array of numbers in ascending order using bubble sort.

(ii) Explain briefly the terms: Translator software, assembler, compiler and interpreter. Differentiate between a compiler and an interpreter.

[10 + 10 marks]

(i) <u>Sorting the array using bubble sort</u>

```
int <stdio.h>
int <conio.h>
int main ();
{ int i, j, temp, n ;

for (i=0, i<n-1, i++) ;
 for(j=0 , j<n-1-i , j++);
 { if a(j) > a(j+1);
     temp = a(j) ;
     a(j) = a(j+1);
     a(j+1) = temp;
 }
}
```

<u>C Program</u>

```
int <stdio.h>
int <conio.h >
int <math.h >
int main ( ) ;
int i, j, temp, n ;
    int a[n] ;
Printf (" load the array",) ;
Scanf ("%d", &n) ;
  For ( i=0, i<n-1, i++) ;
  for( j=0, j <n-1-i, j++);
```

```
{  if a[j] > a[j+1] ;
      temp ==a[j] ;
      a[j]== a[j+1] ;
      a[j+1]== temp ;
   }
      break
}
```

8

(ii) Assembler → Assembler is used to convert assembly language program into machine language code that processor can understand.

Compiler → In computing, a compiler is a computer program that translates computer code written in one programming (High level) language into another language.

Interpreter → Interpreter also used in computer programs to translate the computer code from one language to other and then execute the program.

8

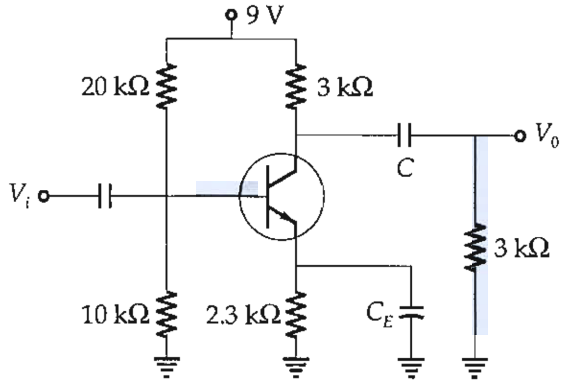
Translator Software → This tool is used to translate the language from one form to other.

Difference between Compiler & Interpreter

Both Compiler and ~~Sof~~ Interpreter do the same job of translating the high level language into machine understandable language. However they both differ in approach/perfomance of that translation.

Compiler translates the entire program into machine understandable code at once while Interpreter translates & also executes the code line by line.

Q.4 (c) **(i)** In the following transistor circuit, $V_{BE} = 0.7$ V, $V_T = 25$ mV and the capacitance are very large.



Find:

1. The value of DC current I_E.
2. The mid band voltage gain of the amplifier.

(ii) What is meant by Direct Memory Access (DMA)? Explain briefly different types of DMA transfer modes.

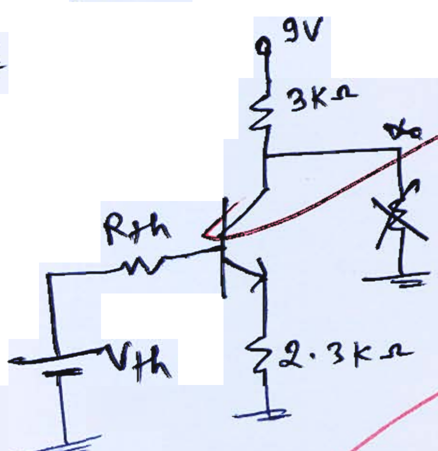
[12 + 8 marks]

(i) DC Analysis

Capacitor → open

AC sources → shorted

1.



$V_{th} = 9 \times \frac{10}{30}$

$\boxed{V_{th} = 3V}$

$R_{th} = \frac{10 \times 20}{30} = 6.67 k\Omega$

KVL

$\Rightarrow -V_{th} + I_B R_{th} + 0.7 + 2.3 I_E = 0$

Assuming $\boxed{\beta = \infty}$ $I_B = 0$

$I_E = \frac{V_{th} - 0.7}{2.3}$

$I_E = \frac{2.3}{2.3}$

$\boxed{I_E = 1 mA}$

2. Mid band voltage gain

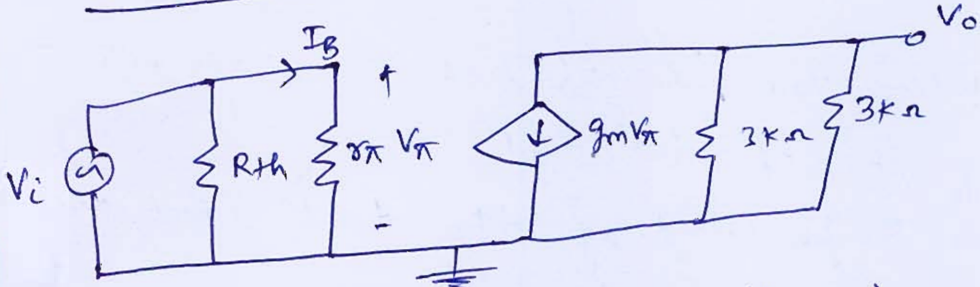
$$g_m = \frac{I_c}{V_T} = \frac{1}{25} = 0.04 \text{ mA/V}$$

AC analysis

Capacitor → shorted

dc sources → OFF

Small signal model



$$V_o = -g_m V_\pi (3k\Omega \,||\, 3k\Omega)$$

$$A_v = \frac{V_o}{V_i} = \frac{V_o}{V_\pi} = -g_m (1.5k\Omega)$$

$$A_v = \frac{1}{25} \times 1.5 \quad k\Omega$$

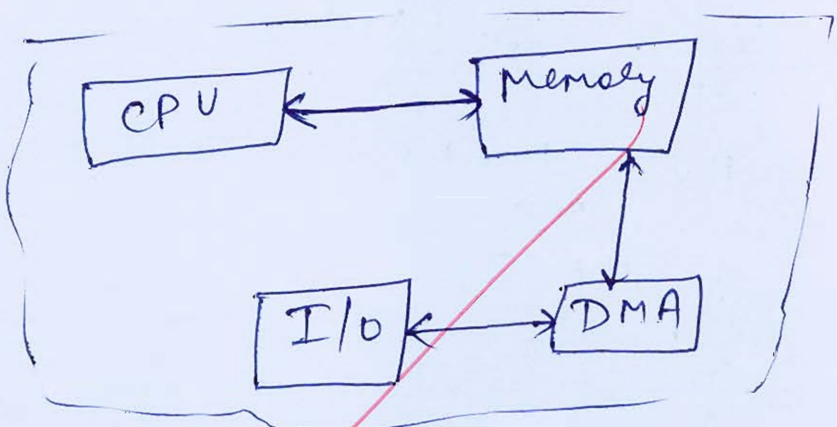
$$\boxed{A_v = -0.06}$$

(11)

(ii) Direct Memory Access (DMA)

Direct Memory access is the easiest and fastest way to make possible the data transfer between I/O device and memory. With the help of DMA, data is transferred from memory to I/O or vice versa. Unlike other processes, DMA is much faster and reliable process.

DMA utilizes the internal buses of processor in doing the operation. CPU meanwhile during that time keeps on doing the task which doesn't require the use of buses



7

Modes of data transfer

1) Block transfer mode → In this mode, a block of data is keep on transfering from I/O device to memory or vice versa.

2) Interleaved mode →

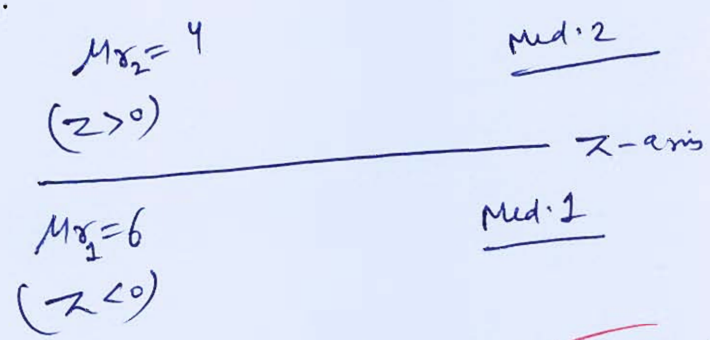
3) Cycle stealing mode → It is the fastest mode where data is transferred in one cycle

Do not write in this margin

Section B : Basic Electronics Engineering + Computer Fundamentals + Electromagnetic Field Theory

Q.5 (a) The *xy*-plane serves as the interface between two different mediums. Medium-1 ($z < 0$) is filled with a material whose $\mu_r = 6$ and medium-2 ($z > 0$) is filled with a material whose $\mu_r = 4$. If the interface carries current $\left(\frac{1}{\mu_0}\right)\hat{a}_y$ mA/m and $\vec{B}_2 = 5\hat{a}_x + 8\hat{a}_z$ mWb/m², find $\vec{H}_1$ and $\vec{B}_1$.

[12 marks]



$$I = \frac{1}{\mu_0}\hat{a_y} \text{ mA/m} \quad B_2 = 5\hat{a_x} + 8\hat{a_z} \ \frac{\text{mwb}}{\text{m}^2}$$

$$B_{2n} = 8\hat{a_z}$$

Since, normal component of B is continuous

$$\boxed{\vec{B}_{1n} = \vec{B}_{2n} = 8\hat{a_z}} \rightarrow (3)$$

$$B_{2t} = 5\hat{a_x}$$

$$H_{2t} = \frac{B_{2t}}{\mu_0 \mu_{r_2}} = \frac{5\hat{a_x}}{4\mu_0} \rightarrow (1)$$

Now,

$$\vec{H}_{1t} - \vec{H}_{2t} = (\hat{K} \times \hat{n})$$

$$\vec{H}_{1t} - \vec{H}_{2t} = \frac{1}{\mu_0}(\hat{a_y} \times \hat{a_z})$$

$$\boxed{\vec{H}_{1t} - \vec{H}_{2t} = \frac{\hat{a_x}}{\mu_0}} \rightarrow (2)$$

from (1) & (2)

$$\vec{H}_{1t} = \left(\frac{5}{4\mu_0} + \frac{1}{\mu_0}\right) \hat{a_n}$$

$$H_{1t} = \frac{9}{4\mu_0} \hat{a_n}$$

from eq^n (3)

$$\mu_1 H_{1n} = \mu_2 H_{2n} = 8 \hat{a_z}$$

$$H_{1n} = \frac{8 \hat{a_z}}{\mu_0 \times 6} = \frac{4 \hat{a_z}}{3\mu_0}$$

6

$$H_1 = H_{1t} + H_{1n}$$

$$H_1 = \frac{9}{4\mu_0} \hat{a_n} + \frac{4}{3\mu_0} \hat{a_z}$$

$$H_1 = \frac{1}{\mu_0}\left(\frac{9}{4} \hat{a_n} + \frac{4}{3} \hat{a_z}\right) \text{ mA/m}$$

$$B_1 = B_{1t} + B_{1n}$$

$$B_1 = \frac{27}{2} \hat{a_n} + 8 \hat{a_z} \text{ mwb/m}^2$$

Q.5 (b) In spherical coordinates, electric field intensity is given by $\vec{E} = \frac{2r}{(r^2+a^2)^2}\hat{a}_r$ V/m. Find the potential at any point, using the reference

(i) $V = 0$ at infinity.

(ii) $V = 0$ at $r = 0$.

(iii) $V = 100$ at $r = a$.

[12 marks]

Given, $E = \frac{2r}{(r^2+a^2)^2} \hat{a_r}$ V/m

$$V = -\int E \cdot dl = -\int \frac{2r}{(r^2+a^2)^2} dr$$

V ⇒ $r^2 + a^2 = t$

$2r\,dr = dt$

$$V = -\int \frac{dt}{t^2} = \frac{1}{t} = \frac{1}{(r^2+a^2)} + C$$

$$\boxed{V = \frac{1}{r^2+a^2} + C}$$

(i) $V = 0$ at $r = \infty$

$0 = \frac{1}{\infty} + C$

$\boxed{C = 0}$

$$\boxed{V = \frac{1}{r^2+a^2}}$$

(ii) $V = 0$ at $r = 0$

$0 = \frac{1}{a^2} = C \Rightarrow C = -\frac{1}{a^2}$

$$\boxed{V = \frac{1}{r^2+a^2} - \frac{1}{a^2}} = \frac{a^2 - r^2 - a^2}{a^2(r^2+a^2)}$$

$$V = \frac{-r^2}{a^2(r^2+a^2)} \text{ V}$$

(iii) $V = 100$ at $r = 9$

$$100 = \frac{1}{r^2 + 9^2} + C$$

$$C = 100 - \frac{1}{2 \cdot 9^2}$$

$$V = \frac{1}{r^2 + 9^2} + 100 - \frac{1}{2 \cdot 9^2}$$

$$\boxed{V = 100 + \frac{1}{r^2 + 9^2} - \frac{1}{2 \cdot 9^2}}$$

11

Good Approach

Q.5 (c) Consider a two level memory hierarchy, L_1 (cache) has an accessing time of 5 ns and main memory has an accessing time of 100 ns. Writing or updating contents takes 20 ns and 200 ns for L_1 and main memory respectively. Assume L_1 gives misses 20% of the time with 60% of the instructions are read only instructions. What is the average access time for system (in ns) if it uses WRITE-THROUGH technique?

[12 marks]

Given, two level memory hierarchy

$L_1 \rightarrow t_{c_1} = 5ns \quad t_{m_1} = 100ns$

$\downarrow$ 20ns $\quad \downarrow$ 200ns

For read only instruction

$H = 0.6$

$t_{avg.} = H\,t_c + (1-H)\,t_m$

$t_{avg} = 0.6 \times 5 + 0.4 \times 100$

$t_{avg} = 43 ns$

Now, by using WRITE-THROUGH technique

$H = 0.8$ → given only 20% miss so 80% hit

$t'_{avg.} = 0.8 \times (43 + 20) + 0.2 \times (100 + 200)$

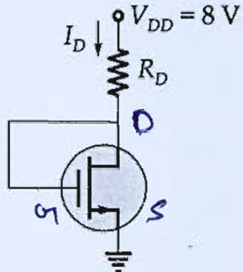
$t_{avg} = 50.4 + 60$

$t'_{avg} = 110.4 ns$

4

Do not write in this margin

Q.5 (d) In the circuit shown, V_T is 1 V. When R_D is 3 kΩ then I_D is 2 mA and when R_D decreased by 1 kΩ then find the value of I_D.



[12 marks]

Given, $V_T = 1V$ $R_D = 3k\Omega$ $I_D = 2mA$

$R_D = 2k\Omega$ $I_D = ?$

from circuit ⇒ $V_S = 0$ $V_G = V_D$

$V_{GS} = V_{DS}$

KVL

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

$$2 = \frac{8 - V_{DS}}{3} \Rightarrow \boxed{V_{DS} = 2V}$$

when $R_D = 2k\Omega$

$$I_D = \frac{8 - 2}{2}$$

$$\boxed{I_D = 3\ mA}$$

9

Do not write in this margin

Q.5 (e) What are the basic functions of an operating system?

[12 marks]

Operating system is a large complex software used to functions given below -

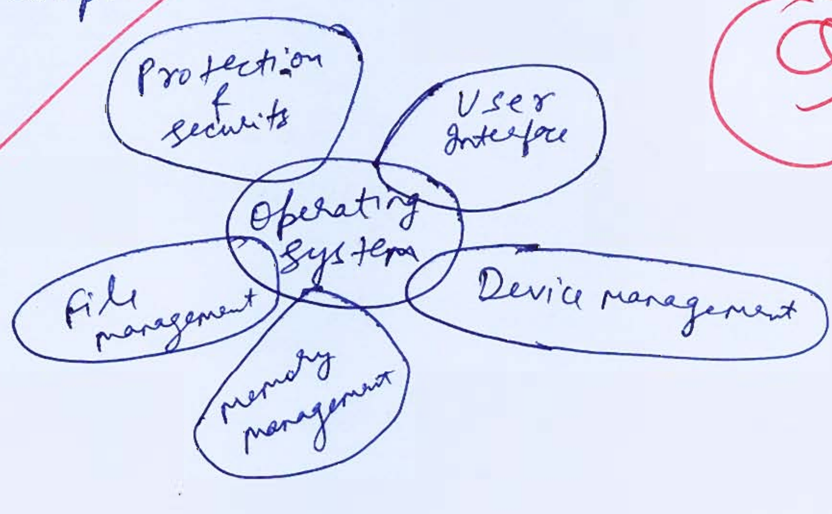
1) File management → a) Managing the file and directories
b) Deleting the corrupt files
c) Controlling the file storage.

2) Device Management → managing the device driver

3) Memory management → a) allocation of optimum memory
b) Preventing fragmentation

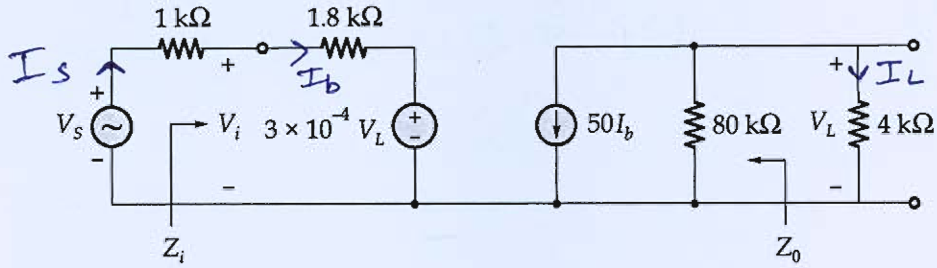
4) Protection & Security → a) Protection of data
b) Authentication of programs & data

5) User Interface → Providing an interface between computer network & computer user.



9

Q.6 (a) The small signal h-parameter ac equivalent circuit of a certain transistor connected in CE configuration is as shown in figure below.



Calculate:

(i) Current gain.

(ii) Voltage gain $\frac{V_L}{V_S}$.

(iii) Input impedance Z_{in}.

(iv) Output impedance Z_{out}.

[20 marks]

From the given small signal h-parameter model

(i) Current Gain

$$A_I = \frac{I_L}{I_S}$$ I_L & I_S are denoted in above circuit

From o/p

$$I_L = -50 I_b \times \frac{80}{80+4}$$

$$I_L = -47.62 I_b$$

Since $I_S = I_b$

$$A_I = \frac{I_L}{I_S} = \frac{I_L}{I_b} = -47.62$$

(ii) Voltage gain

$$A_V = \frac{V_L}{V_S}$$

$$V_L = -50 I_b \times \left(\frac{80 \times 4}{84}\right)$$

$$V_L = -190.47 I_b \rightarrow (1)$$

From i/p loop

KVL

$$-V_s + (1+1.8)I_b + 3\times10^{-4}V_L = 0$$

$$V_s = 2.8 I_b + 3\times10^{-4}\times(-190.47 I_b)$$

$$V_s = 2.74 I_b \rightarrow (2)$$

from (1) & (2)

$$A_v = \frac{V_L}{V_s} = \frac{-190.47 I_b}{2.74 I_b}$$

$$\boxed{A_v = -69.44}$$

(iii) Input Impedance (Z_{in})

from equation (2)

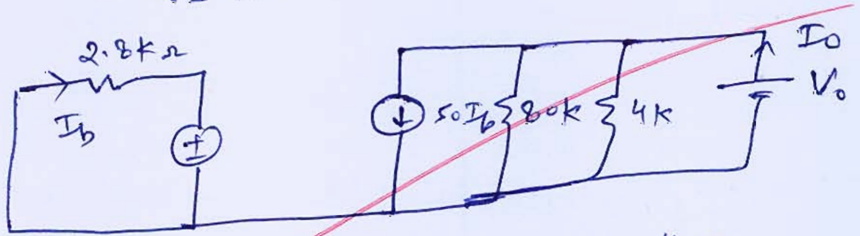
$$V_s = 2.74 I_b$$

$$I_b = I_s$$

$$Z_{in} = \frac{V_s}{I_s} = 2.74\ k\Omega$$

(iv) Output Impedance (Z_{out}), $Z_{out} = \frac{V_o}{I_o}$

$V_s = 0$



from KVL $\quad 2.8 I_b = -3\times10^{-4} V_L$

$$\boxed{I_b = -\frac{3\times10^{-4}}{2.8} V_o} \rightarrow (3)$$

~~$I_L = -47.62 I_b \rightarrow (4)$~~

~~$Z_{out} =$~~

$$I_L = -50 I_b \times \frac{4}{84}$$

$$Z_{out} = \frac{V_o}{I_o} = \frac{2.8 \times 10 \, I_b}{2.38 \, I_b \times 3}$$

$$Z_{out} \simeq 3.92 \, k\Omega$$

(iii) Input Impedance

Also, $Z_{in} = \frac{V_i}{I_b}$

$$V_i = 1.8 I_b + 3 \times 10^{-4} V_L$$

$$V_i = 1.8 I_b + 3 \times 10^{-4} \times (-50 I_b) \times \frac{80 \times 4}{84}$$

$$Z_{in} = \frac{V_i}{I_b} = 1.8 - 3 \times 10^{-4} \times 190.47$$

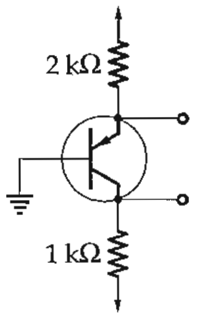
$$\boxed{Z_{in} = 1.742 \, k\Omega}$$

If Z_{in} is asked before source

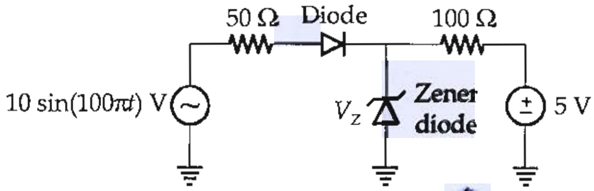
15

then $Z_{in} = 1.742 + 1 = 2.742 \, k\Omega$

Q.6 (b) (i) Determine the voltages at all nodes and currents through all branches. (Assume $\beta = 100$).

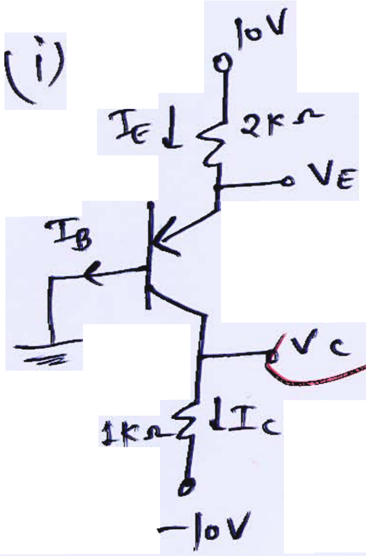


(ii) If the diodes in the circuit shown are ideal and the breakdown voltage V_z of the zener diode is 5 V, find the power dissipated in the 100 Ω resistor.



[10 + 10 marks]

(i)



$\beta = 100$

KVL

$-10 + 2I_E + 0.7 = 0$

$I_E = \frac{9.3}{2}$

$I_E = 4.65\,mA$

$I_B = \frac{I_E}{1+\beta} = \frac{4.65}{101}$

$I_B = 0.046$ mA

$I_C = I_E - I_B \Rightarrow I_C = 4.603\ mA$

$V_E = 10 - 2I_E = 10 - 2 \times 4.65$

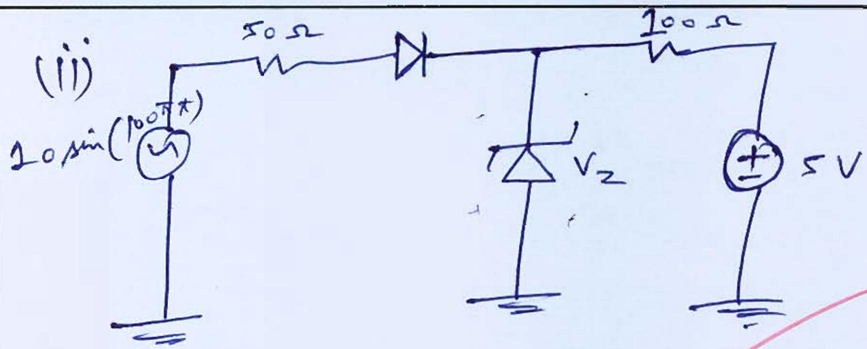
$V_E = 0.7V$ $\quad V_B = 0V$

$V_C = I_C - 10 \Rightarrow V_C = -5.397\,V$

9

Good Approach

(ii)

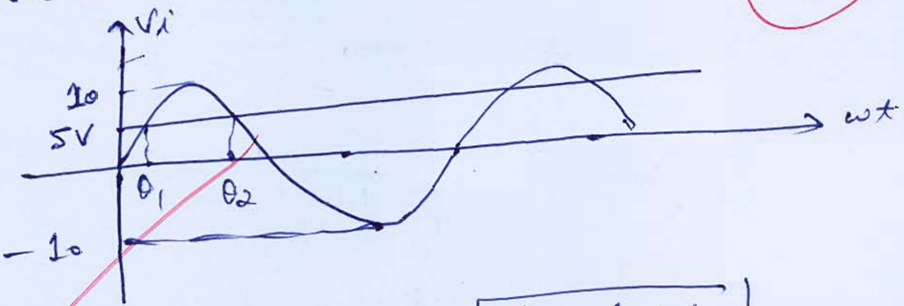


Given, Diode → ideal

$V_Z = 5V$

$P_{100\Omega} = ?$

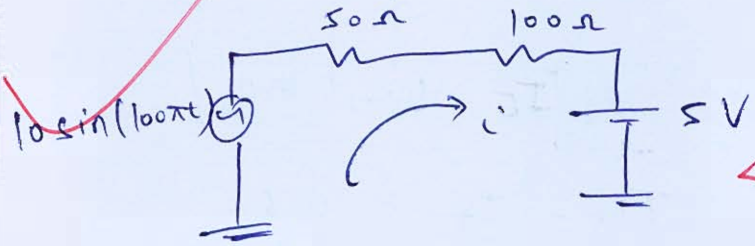
$V_i = 10 \sin(100\pi t)$



(3)

+ve cycle of input $V_i < 5V$

D ON, ZD → off

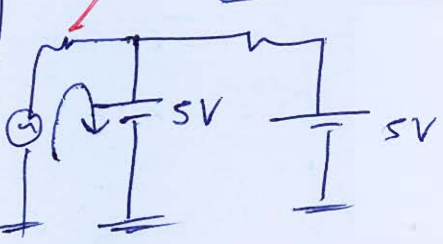


$$i = \frac{10 \sin(100\pi t) - 5}{150}$$

$i = 0.067 \sin(100\pi t) - 0.033 A$ → (1)

+ve cycle of input $V_i > 5V$

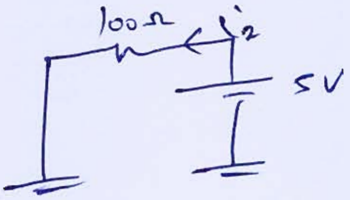
ZD → Breakdown $V_Z = 5V$



$i_{100\Omega} = 0$

-ve cycle of input

D off ZD → ON (FB)



$i_2 = \frac{5}{100} = 0.05$

$P_2 = i^2 \times 100$

$P_2 = (0.05)^2 \times 100$

$P_2 = 0.25W \rightarrow (2)$

from equation (1)

$$i_{rms} = \left[\frac{1}{T}\int_{\theta_1}^{\theta_2}[0.067\sin(100\pi t) - 0.033]^2 dt\right]^{1/2}$$

$T = 0.02 sec.$

~~$\theta_1 = \sin^{-1}\frac{5}{10} = 30^\circ$~~

~~$\theta_2 = 150^\circ$~~

$i_{rms} = 0.348 A$

$P_1 = i_{rms}^2 \times 100$

$P_1 = 12.11 W$

$P_{dissipated} = P_1 + P_2$

$= 12.11 + 0.25$

$= 12.36 W$

Q.6 (c) (i) Explain the IEEE standard 754 floating point numbers representation.

(ii) Determine the size of subfields (in bits) in the address for direct mapping and associative mapping cache scheme:
Size of main memory = 256 MB
Size of cache memory = 1 MB
The address space of this processor is 256 MB. The block size is 128 bytes.

[10 + 10 marks]

(i) IEEE standard 754 floating point no. representation

It is a method of representing any number into a very easy form to understand and implement. This representation helps in executing & calculating very complex problems. This IEEE standard saves time, quite reliable.

There are three terms included in it

1) Sign bit → Sign bit is used to tell about whether the number written is positive or negative.

0 → +ve number
1 → -ve number

2) Exponent → Here, the actual exponent is converted into stored exponent with the help of bias.

actual exponent ← $e + \text{bias} = E$ → stored exponent

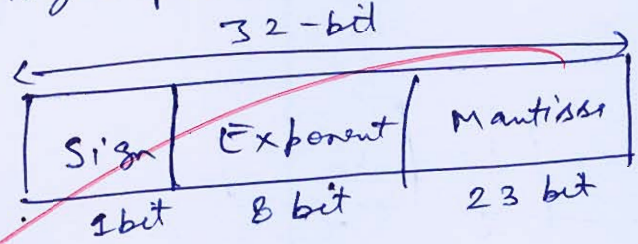
bias = 2^{k-1}, k-bits

3) Mantissa → Mantissa is the magnitude represented in the form of 0 and 1. The representation of mantissa is in two ways implicit & explicit

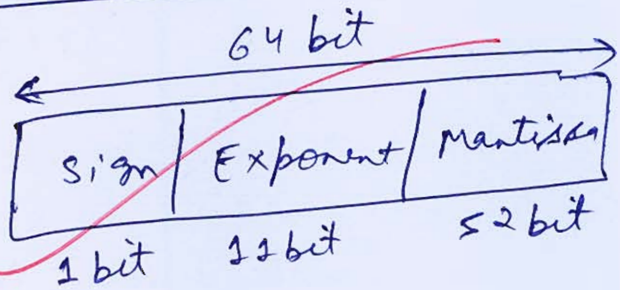
representation. It is represented after decimal as M and before decimal a '1' is taken.

IEEE754 standard

1) Single precision



2) Double Precision



(ii) Given

Size of MM = 256MB = 28 bits

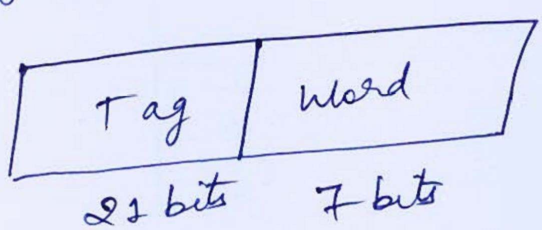
Size of CM = 1MB = 20 bits

Block size = 128 bytes = 7 bits

Associative mapping

Total processor space = 28 bits

Tag space = 28 − 7 = 21 bits



Direct Mapping

No. of cache lines = $\frac{1 MB}{128 \text{ bytes}} = \frac{2^{20}}{2^{7}} = 2^{13}$

No. of bits for word/blocks = 7

tag	LO	WO
8 bits	13 bits	7 bits

Tag = $28 - (13+7) = 8$ bits

17

Q.7 (a) (i) A processor has 16 integer registers (R0, R1, ..., R15) and 64 floating point registers (F0, F1, ..., F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3 and Type-4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (IF). Find the maximum value of N.

[12 marks]

Do not write in this margin

.7 (a) **(ii)** The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. Find the average memory access time (in nanoseconds) in executing the sequence of instructions.

[8 marks]

Do not write in this margin

Q.7 (b) An electrostatic field is given by,

$$\bar{E} = -8xy\,\hat{a}_x - 4x^2\hat{a}_y + \hat{a}_z \text{ V/m}$$

The charge of 6 C is to be moved from $B(1, 8, 5)$ to $A(2, 18, 6)$. Find the work done in each of the following cases:

(i) The path selected is $y = 3x^2 + z$, $z = x + 4$.

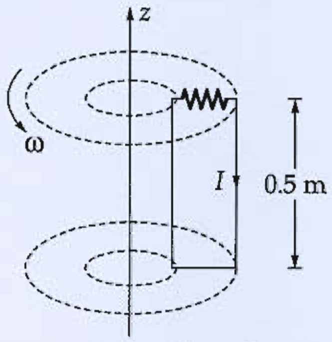
(ii) The straight line from B to A.

Show that work done remains same and is independent of the path selected.

[20 marks]

Do not write in this ma

Q.7 (c) (i) A rectangular conducting loop with resistance of 0.2 Ω rotates at 500 rpm, as shown in figure below. The vertical conductor at $r_1 = 0.03$ m is in the field $\vec{B}_1 = 0.25\hat{a}_r T$ and other conductor is at $r_2 = 0.05$ m and is in the field $\vec{B}_2 = 0.8\hat{a}_r T$. Find the current flowing in the loop.

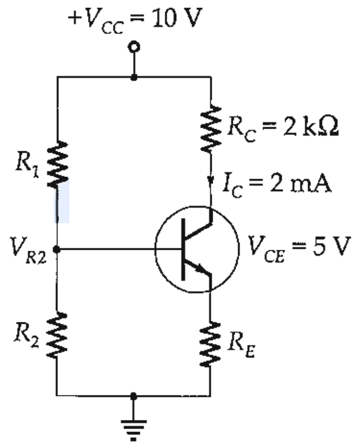


(ii) A wire of non-magnetic material with radius R and length l carries a current I, which is uniformly distributed over its cross-section. What is the magnetic energy inside the wire?

[14 + 6 marks]

Do not write in this ma

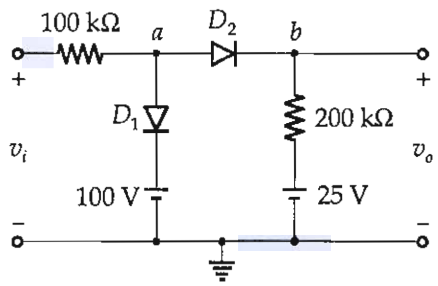
Q.8 (a) A silicon n-p-n transistor operated with self bias gives $V_{CEQ} = 5$ V, $I_{CQ} = 2$ mA for $V_{CC} = 10$ V and $R_C = 2$ K. If β for the transistor is 50, $V_{BE} = 0.7$ V and stability factor "S" is 5 calculate, the values of biasing resistors R_1, R_2 and R_E.



[20 marks]

Do not write in this margin

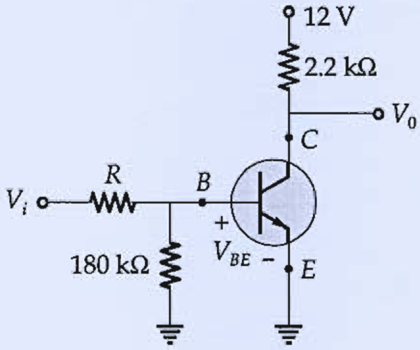
8 (b) Determine and sketch the voltage transfer characteristic of the circuit shown in the figure below.



(Assume that the diodes are ideal)

[20 marks]

Q.8 (c) In the circuit shown below, a silicon transistor with specifications: $\beta \geq 30$ and $I_{CBO} = 100$ nA.



Determine :

(i) The value of V_0 for $V_i = 12$ V and $R = 20$ kΩ and show that transistor is in saturation.

(ii) The minimum value of R for the transistor to remain in the active region for $V_i = 12$ V.

(iii) The value of V_0 for $V_i = 1$ V and $R = 15$ kΩ, also find the region of operation.

[20 marks]

Do no
write i
this m

0000

Space for Rough Work

Space for Rough Work

Space for Rough Work