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ESE 2019 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

Electronics & Telecommunication Engineering

Test-2: Network Theory + Microprocessors and Microcontroller

Digital Circuits-1 + Control Systems-1

Name : .....

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Student's Signature

Instructions for Candidates

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. Answer must be written in English only.
3. Use only black/blue pen.
4. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
5. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
6. Last two pages of this booklet are provided for rough work. Strike off these two pages after completion of the examination.

FOR OFFICE USE

Question No.	Marks Obtained
Section-A	
Q.1	44
Q.2	—
Q.3	—
Q.4	34
Section-B	
Q.5	38
Q.6	41
Q.7	40
Q.8	**
Total Marks Obtained	197

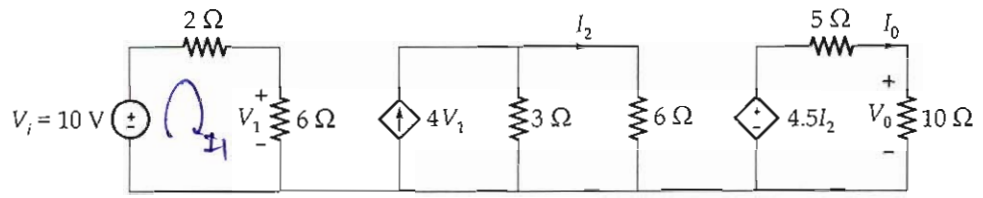
197

Try to avoid calculation error in network theory problems

Signature of Evaluator ..... Cross Checked by .....

Section A : Network Theory + Microprocessors and Microcontroller

Q.1 (a) Consider the circuit shown below:



Determine the output voltage (V_0), output current (I_0) and voltage gain (V_0/V_i).

[12 marks]

* Referring the given circuit diagram and applying the KVL in the loop 1

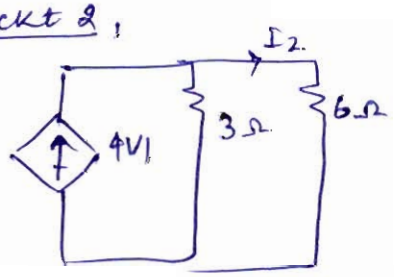
$$-V_i + 2I_1 + 6I_1 = 0$$

$$(8I_1 = V_i)$$

$$I_1 = \left(\frac{10}{8}\right)$$

$$V_i = \left(\frac{10 \times 6}{8}\right) = 7.5 \text{ volts.}$$

* Applying the current division in the ckt 2;

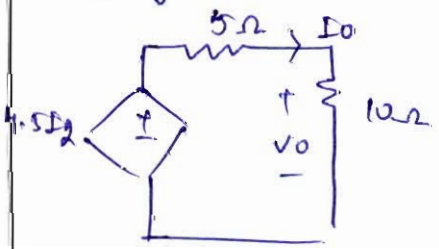


⇒ hence

$$I_2 = \left(\frac{3 \times 4V_1}{9}\right)$$

$$I_2 = \frac{3 \times 4 \times 15}{9 \times 2} = 10\text{A}$$

* Applying the KVL in the outer loop,



⇒ $4.5I_2 = 5I_0 + 10I_0$

$$4.5I_2 = 15I_0$$

$$I_2 = 10\text{A}$$

$$\left(\frac{4.5 \times 10}{15}\right) = I_0 = 3\text{A}$$

hence $V_o = 10 I_o$

$V_o = 10 \times 3$

$V_o = 30$ volts

⇒ Therefore the value of the voltage gain $\left(\frac{V_o}{V_i}\right) = \left(\frac{30}{10}\right) = 3$

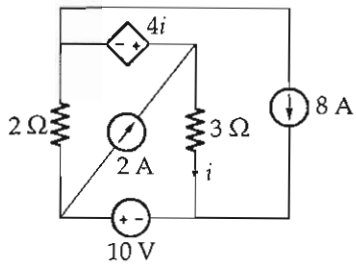
Ans = $V_o = 30$ volts

$I_o = 3A$

$\left(V_o/V_i\right) = \text{gain} = 3.$

12

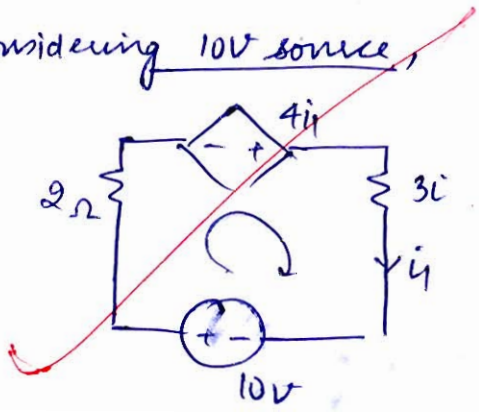
Q.1 (b) For the circuit shown in the figure below, find the current (i), using superposition theorem.



[12 marks]

* For applying the superposition theorem, consider one independent source at a time and disable the rest of independent sources whereas the dependent sources are kept as it is.

* Considering 10V source,

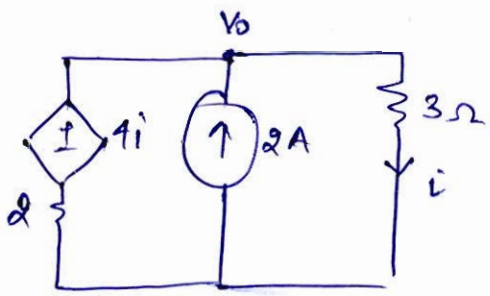


Applying the KVL

$-10 + 2i_1 - 4i_1 + 3i_1 = 0$

$(10 \overset{A}{=} i_1)$

* Considering the 2A source



Let the voltage be V_o,

$\therefore i = \frac{V_o}{3} \Rightarrow V_o = 3i$

Applying the KCL,

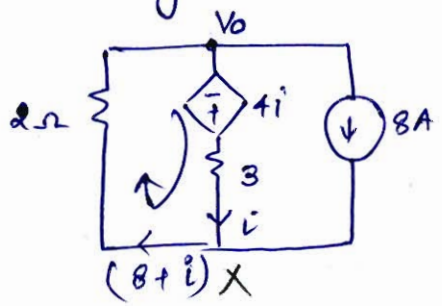
$$2 = \frac{V_o}{3} + \left(\frac{V_o - 4i}{2}\right)$$

$$2 = \frac{3i}{3} + \left(\frac{3i - 4i}{2}\right)$$

$$2 = \left(i - \frac{i}{2}\right)$$

$(i_2 \overset{A}{=} 4A)$

* Considering the 8A source,



applying the KCL at node Vo.

$$\left(\frac{V_o}{2} + 8 + \frac{V_o + 4i}{3}\right) = 0$$

$-V_o - 4i + 3i = 0$

$\frac{V_o + 4i}{3}$

applying the KVL,

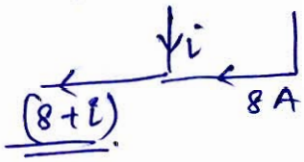
$$-4i + 3i + 2(8+i) = 0$$

$$\Rightarrow -i + 2i + 16 = 0$$

$$(i_3 = -16A)$$

Current flowing in 2Ω

By KCL at node X



hence the net value of the current i =

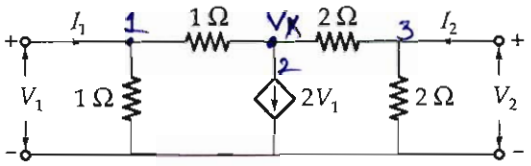
$i_1 + i_2 + i_3 = i$ By superposition theorem

$$\therefore i = (10 + 4 - 16)$$

Ans $\boxed{i = -(2A)}$

hence the current flows in upward direction.

Q.1 (c) Obtain Z-parameter matrix for the circuit shown in the figure below:



[12 marks]

* Refering the given circuit shown,

→ applying the KCL at node 1

$$I_1 = \frac{V_1}{1} + \frac{V_1 - V_x}{1} \quad \text{—(1)}$$

→ applying the KCL at node 2.

$$\frac{V_1 - V_x}{1} = 2V_1 + \frac{V_x - V_2}{2} \quad \text{—(2)}$$

→ applying the KCL at node 3.

$$\frac{V_x - V_2}{2} + I_2 = \frac{V_2}{2} \quad \text{—(3)}$$

* Simplifying the above equations,

→ $I_1 = 2V_1 - V_x$ —(4)

→ $2V_1 - 2V_x = 4V_1 + V_x - V_2$

$V_2 - 2V_1 \Rightarrow 3V_x$ —(5)

→ $V_x - V_2 + 2I_2 = V_2$

$(V_x + 2I_2 = 2V_2)$ —(6)

Substituting (5) in (4)

$$I_1 = 2V_1 - \left(\frac{V_2 - 2V_1}{3}\right)$$

$$I_1 = 2V_1 + \frac{2V_1}{3} + \frac{V_2}{3}$$

$$I_1 \Rightarrow \frac{8V_1}{3} - \frac{V_2}{3}$$

$$3I_1 = 8V_1 - V_2$$

Substituting (5) in (6)

$$2V_2 - 2I_2 = \left(\frac{V_2 - 2V_1}{3}\right)$$

$$6V_2 - 6I_2 \Rightarrow V_2 - 2V_1$$

$$5V_2 + 2V_1 = 6I_2$$

$$I_2 = \left(\frac{5V_2}{6} + \frac{2}{6}V_1\right)$$

$$\Rightarrow \quad 3I_1 = 8V_1 - \left[\frac{6I_2 - 2V_1}{5}\right]$$

$$15I_1 = 40V_1 - 6I_2 + 2V_1 = 42V_1 - 6I_2$$

(1) $V_1 \Rightarrow \left(\frac{15I_1 + 6I_2}{42}\right)$

$$V_1 = 0.3571 I_1 + 0.142 I_2$$

(2) $$5V_2 + 2\left[\frac{3I_1 + V_2}{8}\right] = 6I_2$$

$$40V_2 + 6I_1 + 2V_2 = 48I_2$$

$$V_2 = \frac{-6I_1 + 48I_2}{42}$$

$$V_2 = -0.142 I_1 + 1.142 I_2$$

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

Ans.

$$= \begin{bmatrix} 0.357 & 0.142 \\ -0.142 & 1.142 \end{bmatrix}$$

Q.1 (d) Consider the following subroutine program of an 8085 microprocessor, which is operating with a clock frequency of 2 MHz:

```
        MVI B, DATA_8 bit
LOOP:   DCR B
        JNZ LOOP
        RET
```

Let "*N*" is the decimal equivalent of the DATA_8 bit stored in B register. By analyzing the above program, derive an expression for the overall time delay produced by the subroutine. Using the result obtained, determine the value of "*N*" required to produce the overall time delay of 70 μs.

[12 marks]

* The given loop runs for N times if N is the decimal equivalent of the 8 bit number stored in the register B. Out of those & N executions, (N-1) times the loop runs for true condⁿ of the loop & once it's false i.e. the last case

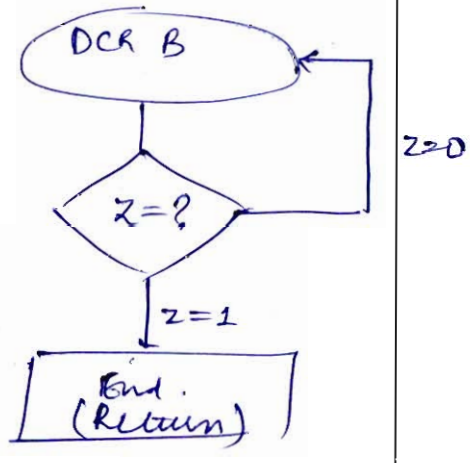
* No. of T states reqd for execution of DCR B = 4 states

* JNZ LOOP is a condⁿ ~~loop~~ jump instruction which takes • 10 T states, if true
  • 7 T states, if false

* RET, it takes a total of 10 T states for the execution.

* When the loop is true, only (DCR B & JNZ LOOP) executes,

∴ Total execution time
= (N-1)[4+10] T states



When the cond^n becomes false, the loop will execute for, 1 time

$t \Rightarrow (4 + 7 + 10)$ Tstates

DCR — JNZ (false) — Return

$\Rightarrow$ Total Tstates

$= \{(N-1)[14] + 21\}$ Tstates

given $f =$ 2MHz,

$\therefore T = \left(\frac{1}{2}\ \mu s\right) = (0.5\ \mu s)$

$\rightarrow$ In order to produce overall delay of 70 μs

Wrong approach

$\frac{1}{2}\{(N-1)14 + 21\} = 70$

$(N-1)14 + 21 = 140$

$(N-1)14 = 119$

$(N-1) = 8.5$

$(N = 9.5)$

Ans = decimal eq = 10 Ans

Q.1 (e) Differentiate between embedded and general purpose computing systems.

[12 marks]

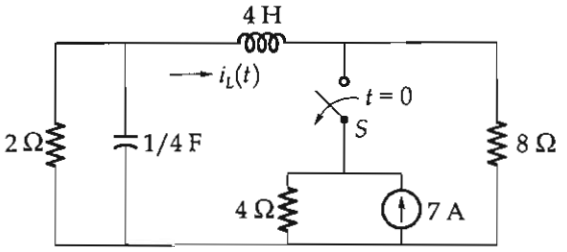
* Embedded systems are the computer which can perform only the specific operations unlike the general purpose which can perform a wide of operations

* Memory has to applied externally in them whereas in general purpose inbuild

* faster than general purpose computers.

* Can be used for variety but not so with embedded.

Q.2 (a) In the circuit shown in the figure below, the switch S is closed for a long time and opened at $t = 0$. Find the time domain expression of the current $i_L(t)$ for $t > 0$.



[20 marks]

Q.2 (b) The reduced incidence matrix of a linear graph is given below:

$$A = \begin{array}{c} \begin{matrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 \end{matrix} \leftarrow \text{Branches} \\ \begin{bmatrix} 0 & 0 & 1 & 1 & 1 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 1 & 1 \\ -1 & 0 & -1 & 0 & 0 & -1 & 0 \end{bmatrix} \end{array}$$

The branches [2, 3, 4] constitute a tree.

(i) Without drawing the graph, determine the f-cutset matrix Q_C.

(ii) Determine the number of trees possible for the graph.

(iii) Draw the graph and verify the result for Q_C.

[20 marks]

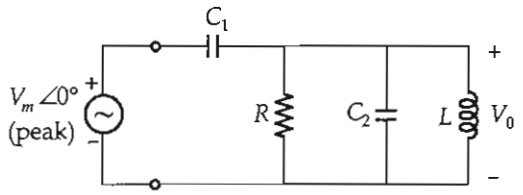
Q.2 (c) (i) Complete the following table by indicating the logic level (1 or 0) on each control or status pin of 8085 microprocessor for various machine cycles shown.

Machine Cycle	$\overline{RD}$	$\overline{WR}$	IO/$\overline{M}$	S_1	S_0
Memory read					
Memory write					
I/O read					
I/O write					
Opcode fetch					
Halt					

(ii) Draw the timing diagram of data flow when the 8085 instruction MOV C, A (machine code 4FH), stored in the memory location 2005H, is being fetched.

[8 + 12 marks]

Q.3 (a) Consider the circuit shown in the figure below:



(i) Derive an expression for the resonant frequency of the above circuit.

(ii) If $V_m = 10$ V, $R = 1$ kΩ, $C_1 = 2$ nF, $C_2 = 8$ nF and $L = 5$ mH, then determine the effective value of the voltage V_0 at resonant frequency by using the result obtained in part (i).

[25 marks]

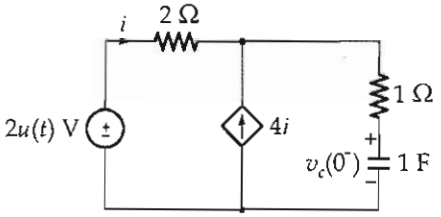
Q.3 (b) Assuming the microprocessor is completing an RST7.5 interrupt request, check to see if RST6.5 is pending. If it is pending, enable RST6.5 without affecting any other interrupt; otherwise, return to the main program.

[15 marks]

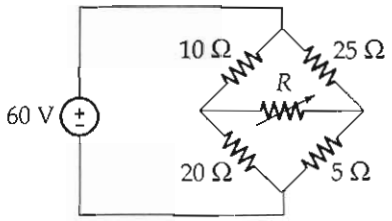
Q.3 (c) Write an 8085 assembly language program to arrange a data array in ascending order. The array is stored from the memory location 2501H and the length of the array is stored at 2500H. The resultant array should be stored from the memory location 2601H. Assume that the numbers in the data array are represented in unsigned 8-bit format.

[20 marks]

Q.4 (a) (i) In the circuit shown below, the initial voltage across the capacitor is $v_c(0^-) = 1$ V. Find the expression of the voltage $v_c(t)$ for $t > 0$.



(ii) Determine the maximum power that can be delivered to the variable resistor R in the circuit shown below.



[13 + 12 marks]

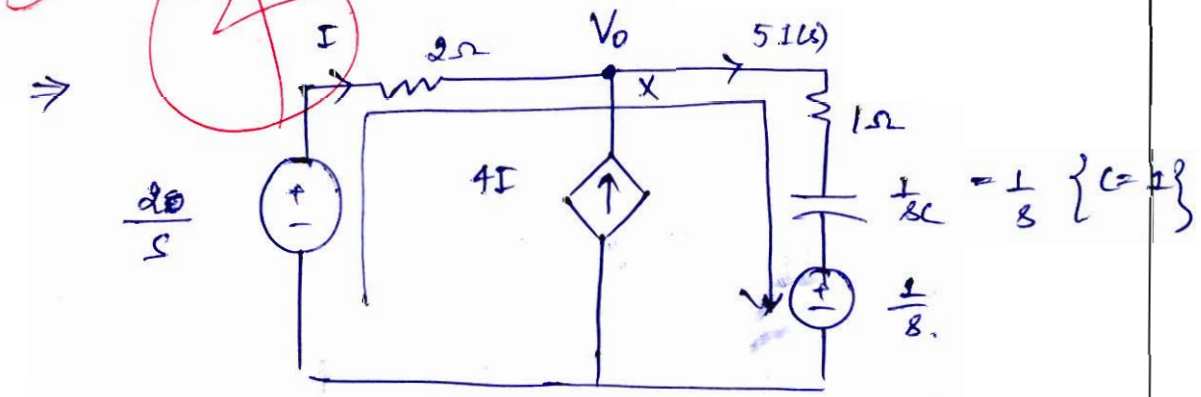
Sol^n 1). $V_C(0^-) = 1V$ given,

Drawing the s-equivalent n/w of the given ckt diagram, we know that for capacitor

$$I = C\frac{dV}{dt}$$

$$I(s) = C[sV(s) - V(0^-)]$$

$$\frac{I(s)}{sC} + \frac{V(0^-)}{s} = V(s)$$



Let the voltage be V_o at node X and applying KCL at node X

$$I(s) = \frac{\left(\frac{2}{s} - V_0\right)}{2}$$

$$* \quad \frac{\frac{2}{s} - V_0}{2} + 4\left[\frac{\frac{2}{s} - V_0}{2}\right] = \frac{V_0 - 1/s}{(1 + 1/s)}$$

$$3\left[\frac{\frac{2}{s} - V_0}{2}\right] = \frac{V_0 - 1/s}{(1 + 1/s)}$$

$$\left(\frac{6}{s} - 3V_0\right)\left(1 + \frac{1}{s}\right) = \left(V_0 - \frac{1}{s}\right)$$

$$\frac{6}{s} + \frac{6}{s^2} - 3V_0 - \frac{3V_0}{s} = V_0 - \frac{1}{s}$$

$$\left(\frac{7}{s} + \frac{6}{s^2}\right) \Rightarrow \Rightarrow \left(4V_0 + \frac{3V_0}{s}\right)$$

$$\left(\frac{7s+6}{s^2}\right) = \frac{(4s+3)V_0}{s}$$

$$\frac{5}{s} - \frac{5}{(s+1/3)} = \frac{5s - 5s + 5/3}{s(s+1/3)}$$

$$V_0 = \frac{(7s+6)}{s(4s+3)}$$

Applying the KVL in outer loop,

$$\frac{2}{s} = 2I(s) + I(s) + \frac{I(s)}{s} + \frac{1}{s}$$

$$\frac{1}{s} = 3I(s) + \frac{I(s)}{s}$$

$$\frac{1}{s} = I(s)\left[\frac{3s+1}{s}\right]$$

current calculation done here

$$I(s) = \left(\frac{1}{3s+1}\right)$$

$$V_c(s) = \left[5I(s) \times \frac{1}{s}\right] = \left[\frac{5}{(3s+1)s}\right] = \frac{5/3}{(s+1/3)(s)}$$

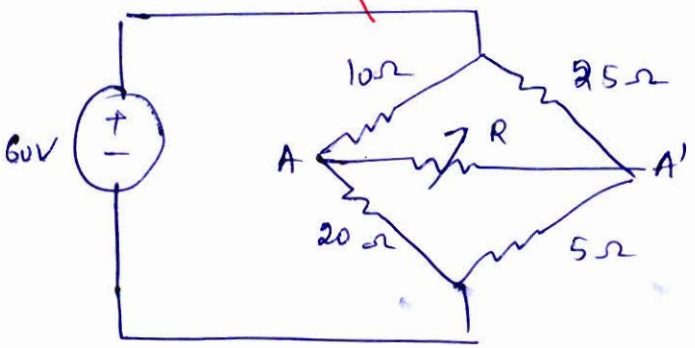
$$V_c(s) = \frac{A}{s} + \frac{B}{(s+1/3)} \Rightarrow A = (5)$$

$$B = (-5)$$

$V(s) = \left(\frac{5}{s} - \frac{5}{s+1/3}\right)$

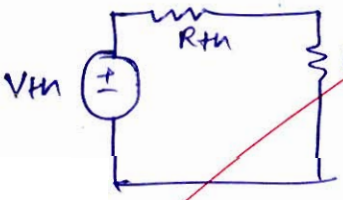
$v(t) = \mathcal{L}^{-1}[V(s)] = \boxed{V(t) = 5\left[1 - e^{-t/3}\right]u(t) \text{ volts}}$

(ii)



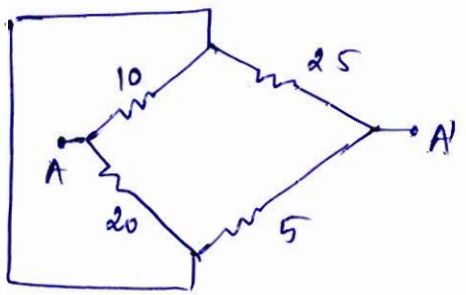
* Maximum power transfer theorem states that the maximum power will be delivered by the source to the load, if the value of the load ~~impedance~~ resistance = source resistance (for DC circuits)

* Therefore applying the Thevenin's theorem across the terminals (AA'), the simplified ckt will be



1) Calculation of R_{th}

-for the calculation of R_{th}, deactivate all the independent source and calculate the resistance across the terminals AA' by removing the load R.



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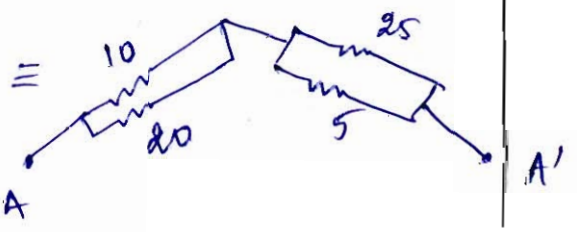


→ $10||20 = \frac{10\times20}{30} = \frac{20}{3}\Omega = \left(\frac{40}{6}\right)\Omega$

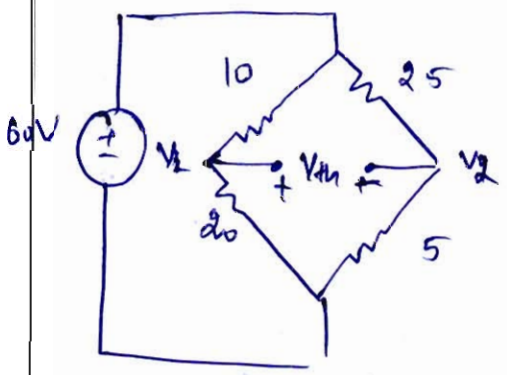
→ $5||25 = \frac{5\times25}{30} 6 \Rightarrow \left(\frac{12.5}{3}\right)\Omega = \frac{25}{6}\Omega$

$R_{th} = \left(\frac{20}{3} + \frac{25}{6}\right) = \left(\frac{40+25}{6}\right) = \frac{65}{6} = (10.833\,\Omega)$

* Hence the value of R for max^m power transfer
$= 10.833\,\Omega$

→ Calculation of V_{th}

for the calculation of V_{th}, calculate the open circuit voltage across the terminals AA'.



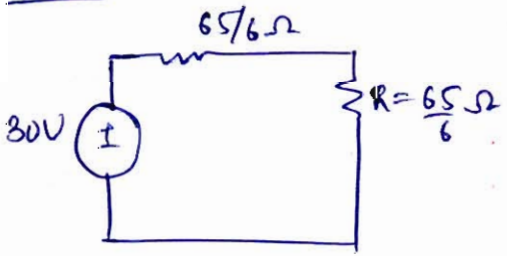
$V_{th} = (V_1 - V_2)$

$V_1 = \frac{60}{30}\times 20 \Rightarrow 40V$

$V_2 = \frac{60^2}{30}\times 5 = 10V$

$V_{th} = 30V$.

Hence



* Max^m power that can be delivered =

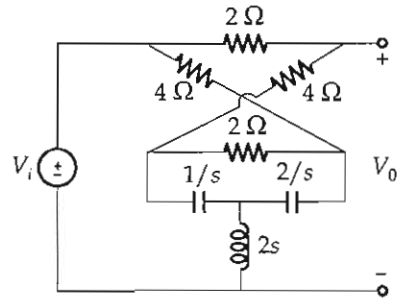
$P_{max} = \left(\frac{V_{th}^2}{4R_L}\right)$

$\Rightarrow \left[\frac{30^2\times 6}{4\times 65}\right]$

Max^m power delivered

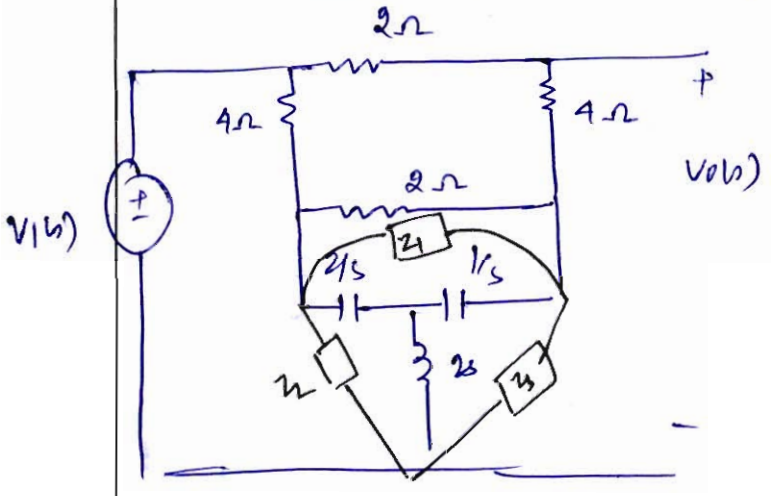
$P_{max} = 20.7692$ Watts

Q.4 (b) For the network shown in the figure below, find the voltage gain V_0 / V_i.

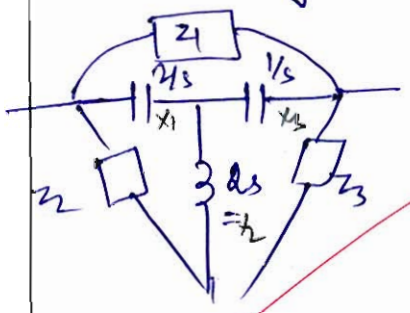


[15 marks]

* This ckt can be redrawn as,



* converting the given star to Delta,



$$Z_1 = \frac{X_1X_3 + X_1X_2 + X_2X_3}{X_2}$$

$$Z_1 = \frac{\left[\frac{2}{s} \times 1 + \frac{1}{s} \times 2s + \frac{1}{s} \times 2s\right]}{2s}$$

$$Z_1 = \frac{\left[\frac{2}{s^2} + (2+4)\right]}{2s} \Rightarrow \frac{(2+6s^2)}{2s^3} = \frac{(1+3s^2)}{s^3}$$

$$Z_2 = \frac{2/s^2 + 6}{1/s} = \frac{2+6s^2}{s^2 \times 1/s} = \frac{2+6s^2}{s}$$

$$Z_3 = \frac{2/s^2 + 6}{2/s} = \frac{2+6s^2}{s^2 \times 2/s} \Rightarrow \frac{(1+3s^2)}{s}$$

$\frac{(1/s \times 1/s)^3}{1/s}$

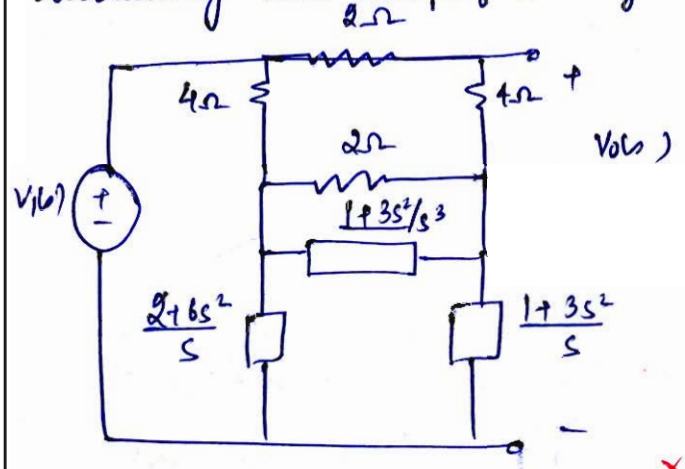
2Ω (1)

$\frac{2}{s^2} + (2+4)$

$\frac{2s}{}$

$\Rightarrow \frac{2+6s^2}{2s^3}$

Redrawing the simplified diagram,



Complete solution

Q.4 (c) (i) Explain different addressing modes of 8086 microprocessor for sequential control flow instructions, with an example for each addressing mode.

(ii) Write a short note on the flag register of 8086 microprocessor.

[12 + 8 marks]

* The different addressing modes of the 8086 microprocessor are as follows:-

I) Direct Addressing Mode

↳ In the case of direct addressing mode, the addres of the instruction from where the data is to be fetched is itself present in the instruction. LDA , (3000)H

II) Register Addressing Mode

In the case of register addressig mode, Both the source and the destination are register & the data itself is present in the ~~instruction~~ register

Eg. MOV A, B.

III) Implicit Addressig Mode,

In this, the data itself is implicitly present in the instruction. No need to specify it

Eg. ~~CMA~~, HLT, RET.

IV) Immediate Addressing Mode

In the case of immediate addressig mode, the data itself is present in the instruction.

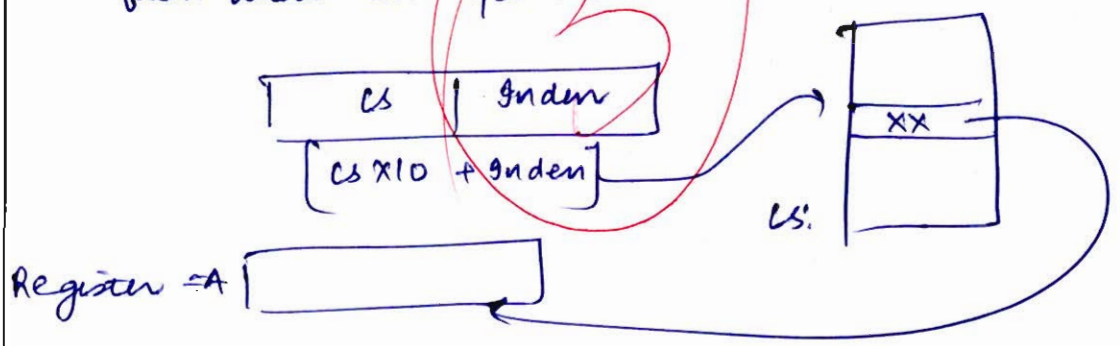
* Register Indirect Addressing mode.

* In this case, the effective address Location is

⇒ [Source Reg] X10 + (Base Register) content
↓
offset

1) Index Addressing Mode,

In this case index register contains the offset value of the address and the next at the next address location the data is present from where it's fetched

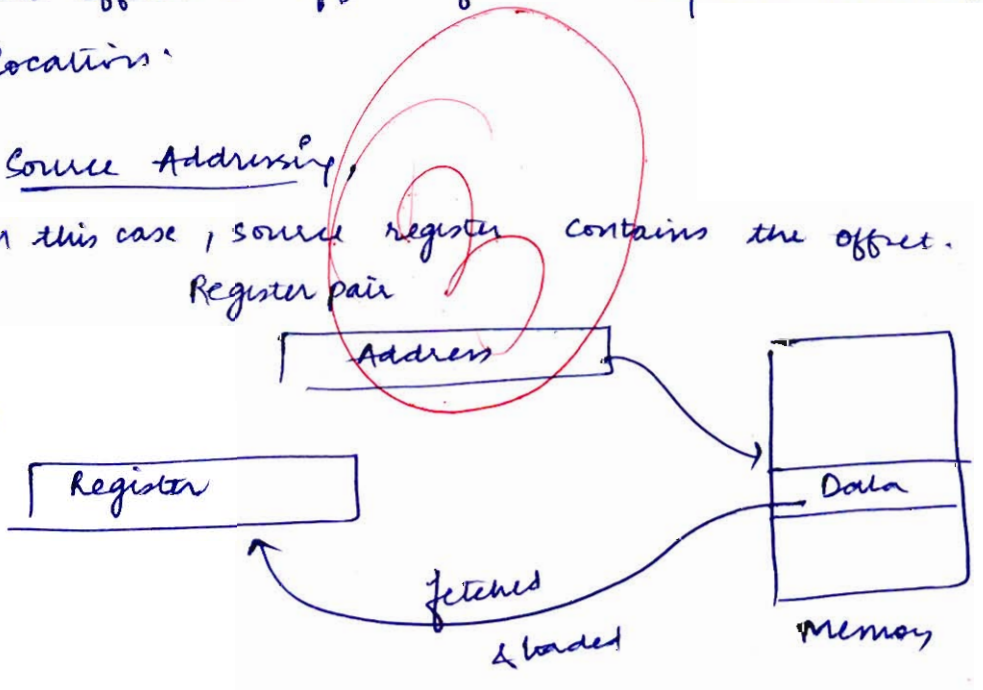


II) (Base + Index Addressing Mode)

* In this case Base + Index register contains the effective offset of the required address locations.

III) Source Addressing,

In this case, source register contains the offset.



11) Flag register of 8086

The flag register of 8086 is a 16 bit register & contains

It contains a total of 9 flags

where i) O = Overflow flag whose value sets when overflow occurs.

ii) D = direction flag. (which defines in which direction memory exceeds

iii) I = Interrupt flag

iv) T = Trap flag (If this is set, then the value is executed after each cycle)

v) Zero flag (set if result is zero)

vi) Sign flag

1 = Negative

0 = +ve

vii) AC = Auxiliary Carry (Carry of Nibble)

viii) Parity ⇒ 1 = Even parity

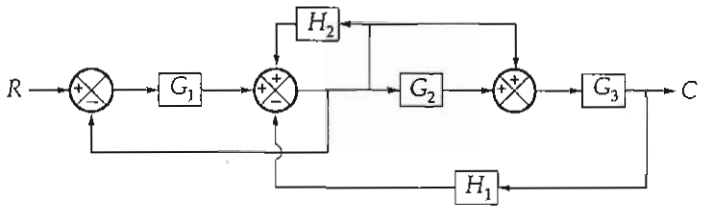
0 = Odd parity

C = Carry = 1 if Carry

Explain clearly

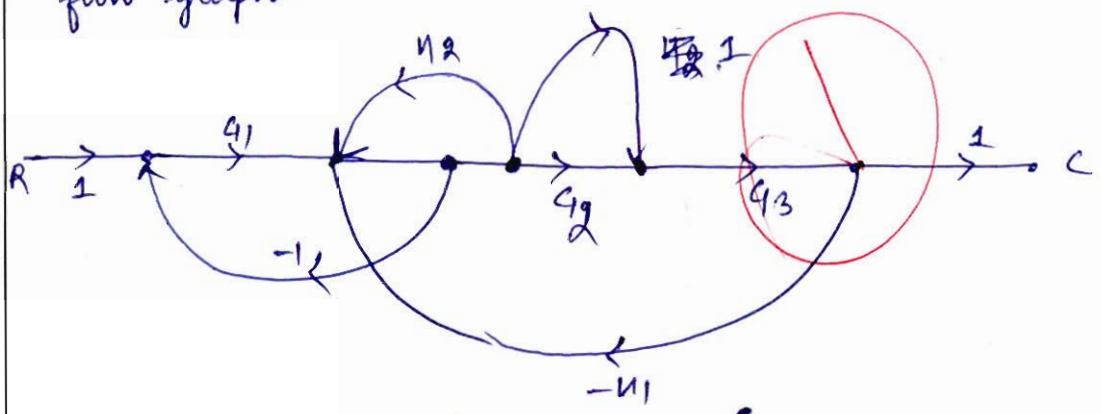
Section B : Digital Circuits-1 + Control Systems-1

Q.5 (a) Find transfer function for the block diagram shown in the figure below:

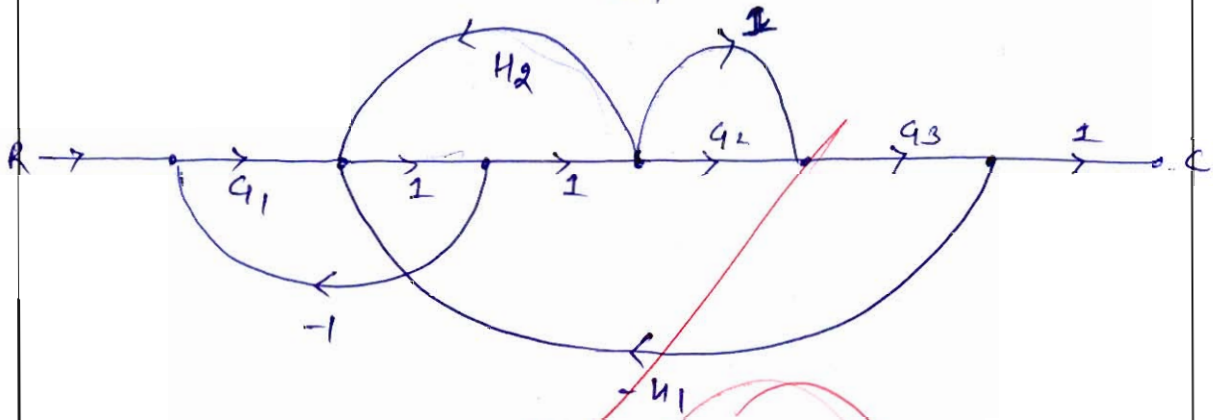


[12 marks]

* In order to find out the transfer function of the given block diagram, draw its equivalent signal flow graph.



⇒



* Applying the Mason gain formula,

$$\frac{C(s)}{R(s)} = \sum_{i=1}^{N} \frac{P_i \Delta_i}{\Delta}$$

N = No. of forward path

P_i = gain of the i^{th} forward path

Δ = 1 − (sum of all loop gains) + [sum of product of 2 non touching loop gain] − − −

Δ_i = 1 − (sum of loop gains that are non touching to i^{th} forward path) + (sum of non touching loop gains

that are non touching to the kth forward path.

$P_1 = G_1 G_2 G_3$.

$P_2 = G_1 G_3$.

loops.

$l_1 = -H_2$

$l_2 = G_1$

$l_3 = -G_2 G_3 H_1$

$l_4 = -G_3 H_1$

$$\Rightarrow \frac{C(s)}{R(s)} = \frac{G_1 G_2 G_3 (1-0) + G_1 G_3 (1-0)}{1 - [-H_2 + G_1 - G_2 G_3 H_1 - G_3 H_1] + 0}$$

$$\Rightarrow \frac{C(s)}{R(s)} = \frac{G_1 G_2 G_3 + G_1 G_3}{1 + H_2 - G_1 + G_2 G_3 H_1 + G_3 H_1}$$

$$\frac{C(s)}{R(s)} \Rightarrow \frac{G_1 G_3 [1 + G_2]}{1 + H_2 - G_1 + G_3 H_1 [1 + G_2]}$$

↳ Transfer fn of the given Block diagram.

8

Q.5 (b) The transfer function of a first order control system is $T(s)=\frac{K}{(s+a)}$. When a step input is applied, the system response reaches 50% of its steady state value in 5 sec. Find the time required by the same response to reach 90% of steady state value.

[12 marks]

Soln.

$$\frac{C(s)}{R(s)} = T(s)$$

Given the transfer function

$$T(s) = \left(\frac{K}{s+a}\right)$$

$$C(s) = \left(\frac{K}{s+a}\right) R(s)$$

$\Rightarrow$ where $R(s) = \left(\frac{1}{s}\right)$ (Unit step fn)

$$C(s) = \left[\frac{K}{(s+a)} \times \frac{1}{s}\right]$$

$$C(s) = \left(\frac{A}{s} + \frac{B}{s+a}\right)$$

$$C(s) = \frac{K/a}{s} + \frac{-K/a}{(s+a)}$$

$$C(s) = K/a\left[\frac{1}{s} - \frac{1}{s+a}\right]$$

$$c(t) \Rightarrow \frac{K}{a}\left[1 - e^{-at}\right] u(t)$$

* Steady state value is the value when $t \to \infty$

$\Rightarrow c(t \to \infty) = \left(\frac{K}{a}\right)$

* Given = The system reaches to 50% of steady state value in (5 sec).

$$c(t=5) = \frac{K\alpha}{2\alpha} = \frac{K}{\alpha}\left[1 - e^{-at}\right]$$

$$\frac{1}{2} = 1 - e^{-at}$$

$$\left(\frac{1}{2} = e^{-at}\right)$$

$$(0.693 = at)$$

$$t = 5 \text{ sec (given)} = \underline{(a = 0.13862)\ \text{sec}^{-1}}$$

* Time required to reach 90% of steady state value

$$c(t) = \left(0.9\frac{K}{a}\right)$$

$$0.9\frac{K}{a} = \frac{K}{a}\left[1 - e^{-at}\right]$$

$$0.9 = 1 - e^{-at}$$

$$e^{-at} = 0.1$$

$$at = 2.302$$

$$t = \left(\frac{2.302}{a}\right)$$

$$t = \frac{2.302}{0.13862} = 16.61 \text{ seconds}$$

Ans. Hence the time reqd to reach 90% of the steady state value by the system

$$= t = 16.61 \text{ seconds.}$$

Q.5 (c) (i) Implement the following multiple output combinational logic circuit using 4-line to 16-line decoder.

$f_1 = \Sigma m(1, 2, 4, 7, 8, 11, 12, 13)$
$f_2 = \Sigma m(2, 3, 9, 11)$
$f_3 = \Sigma m(10, 12, 13, 14)$
$f_4 = \Sigma m(2, 4, 8)$

(ii) Implement $f(A, B, C) = \Sigma m(0, 1, 4, 6, 7)$ using a 4 × 1 MUX by connecting A and B to its select lines.

[6 + 6 marks]

(ii) $f(A,B,C) = \Sigma m(0,1,4,6,7)$

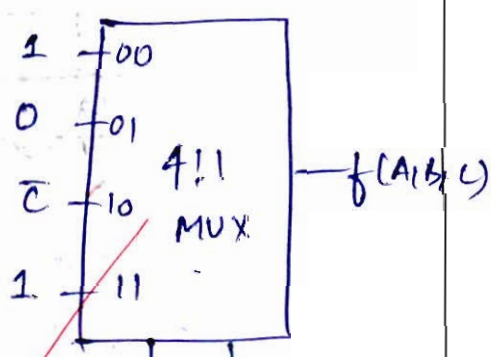
Truth Table,

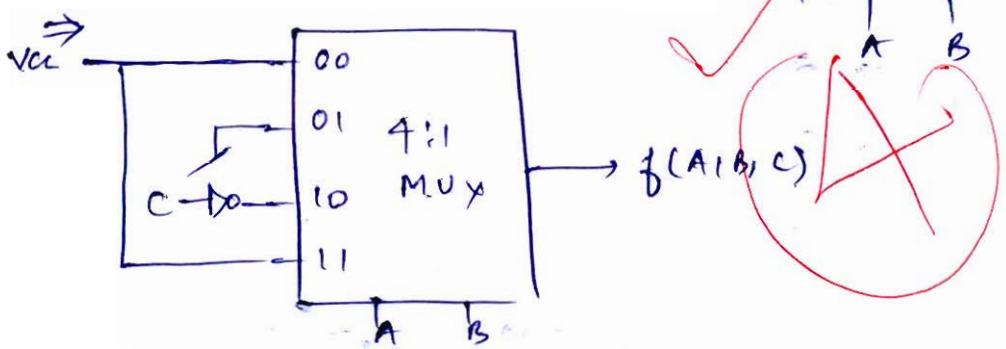
A	B	C	f	
0	0	0	1	1
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	$\bar{C}$
1	0	1	0	
1	1	0	1	1
1	1	1	1	

* with A & B as select lines, the reduced truth table is,

A	B	f
0	0	1
0	1	0
1	0	$\bar{C}$
1	1	1

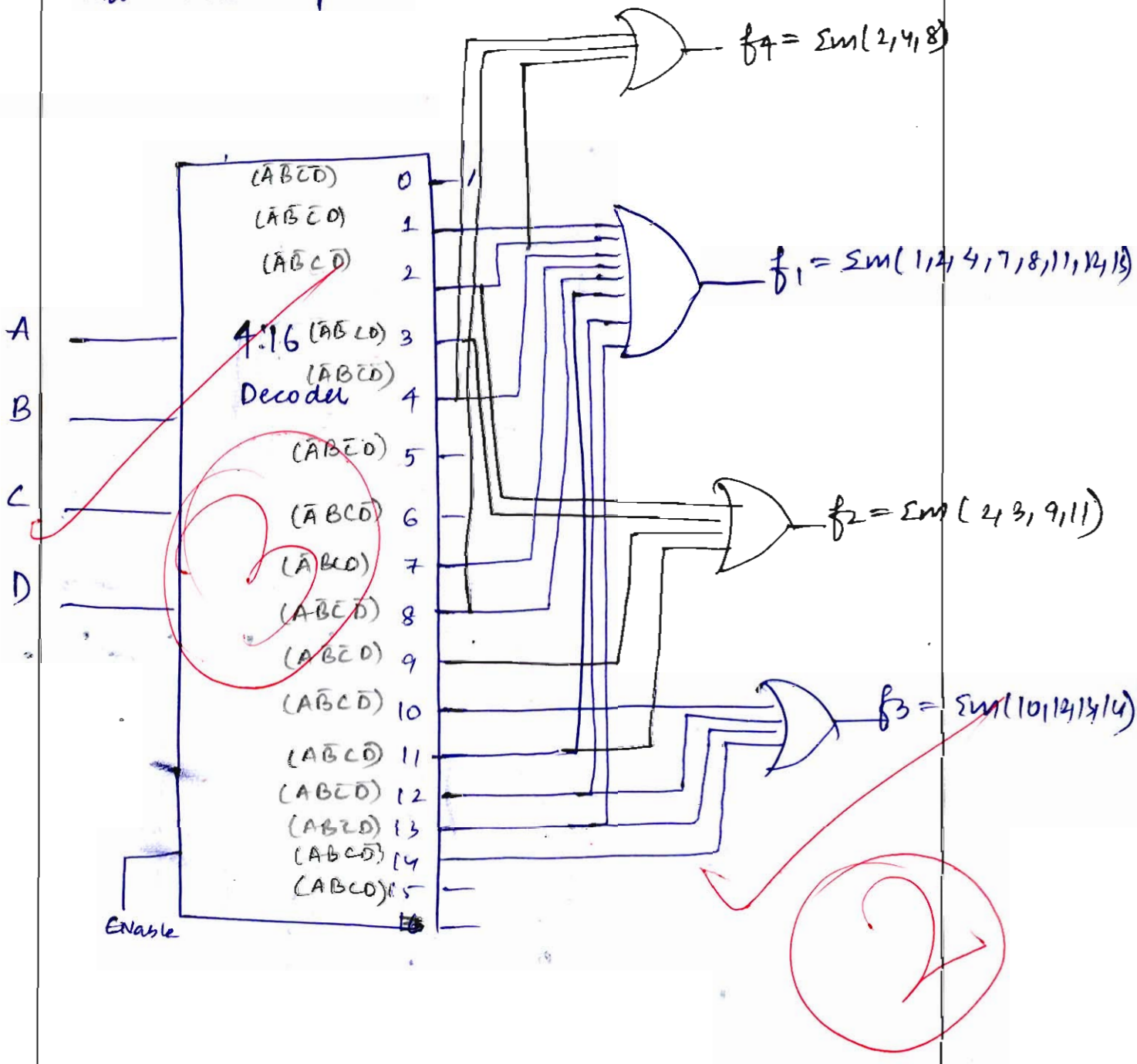
* The MUX representation is





(i) Implementation of the logic using 4:16 line decoder.

* The given fns can be implemented by doing the logical OR of the respective minterms which will make the output = 1



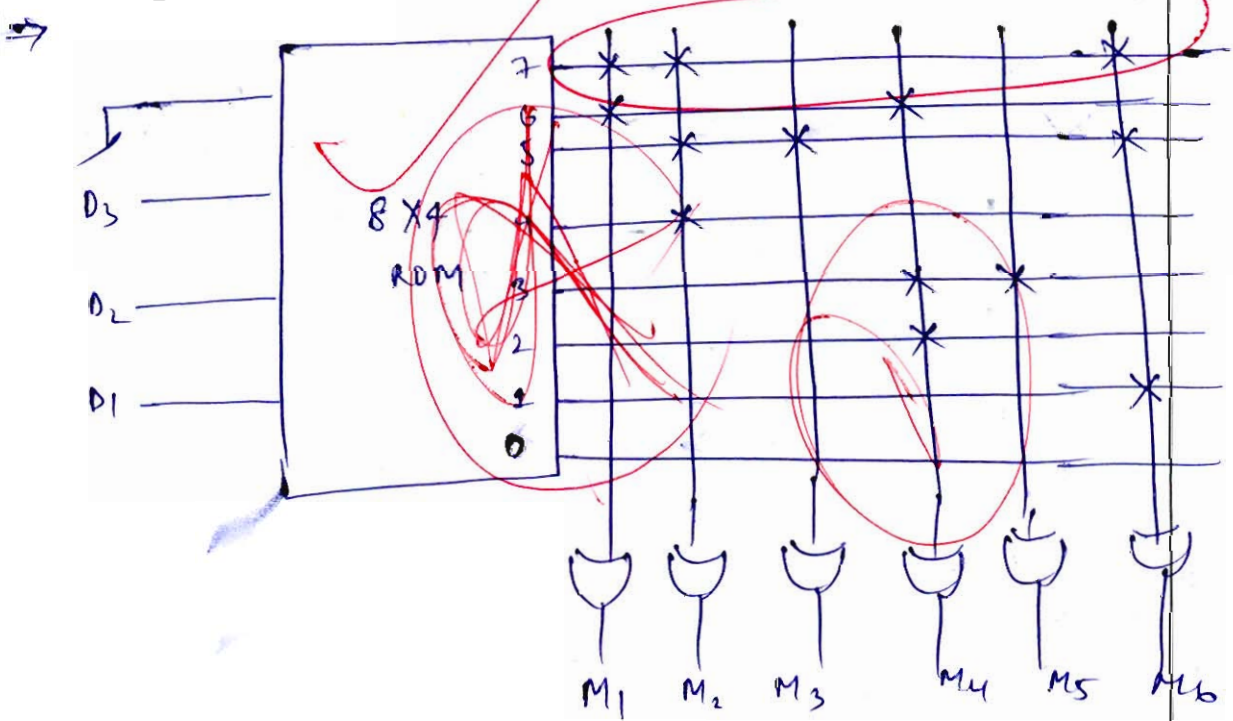
Q.5 (d) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number using a 8 × 4 ROM circuit. **[12 marks]**

3 bit No

D_1	D_2	D_3		square M_1	M_2	M_3	M_4	M_5	M_6
0	0	0		0	0	0	0	0	0
0	0	1		0	0	0	0	0	1
0	1	0		0	0	0	1	0	0
0	1	1	= 6	0	0	0	1	1	0
1	0	0	= 16	0	1	0	0	0	0
1	0	1	= 25	0	1	1	0	0	1
1	1	0	= 36	1	0	0	1	0	0
1	1	1	= 49	1	1	0	0	0	1

It's asked to design with 8×4 ROM

Implementation using ROM ckt



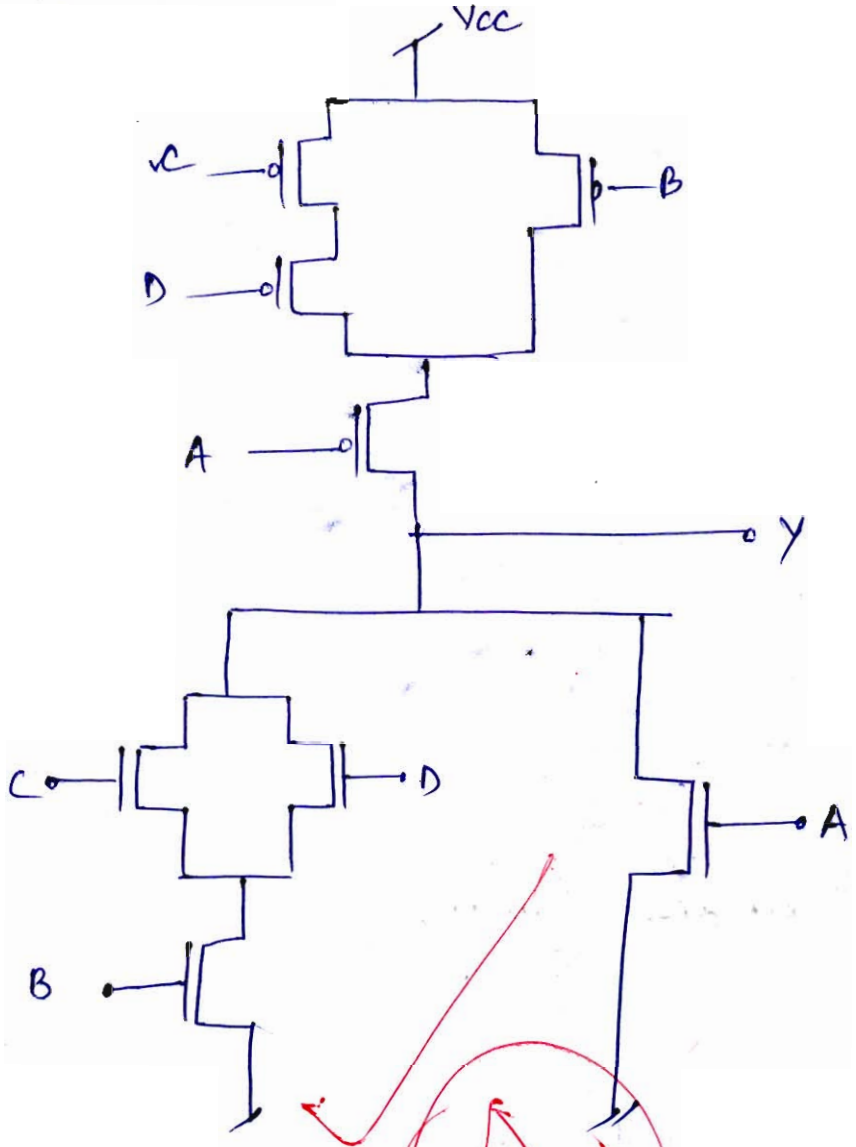
Q.5 (e) Design CMOS logic circuits to implement the following expressions:

(i) $Y = \overline{A + B(\overline{C + D})}$

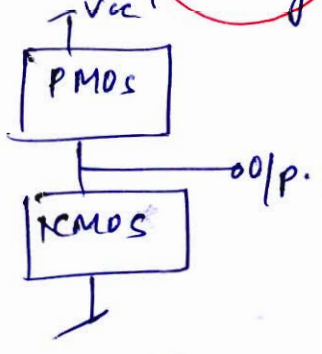
(ii) $Y = \overline{A} + \overline{B} + (\overline{C + D})$

[6 + 6 marks]

⇒ 1) $Y = \overline{A + B(C+D)}$

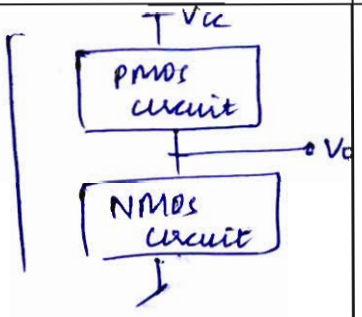


* Any ckt can be implemented as a combination of NMOS & PMOS forming CMOS ie.



11) $Y = (\overline{A} + \overline{B} + \overline{C+D})$

⇒ General implementation ⇒



The given Y can be written as

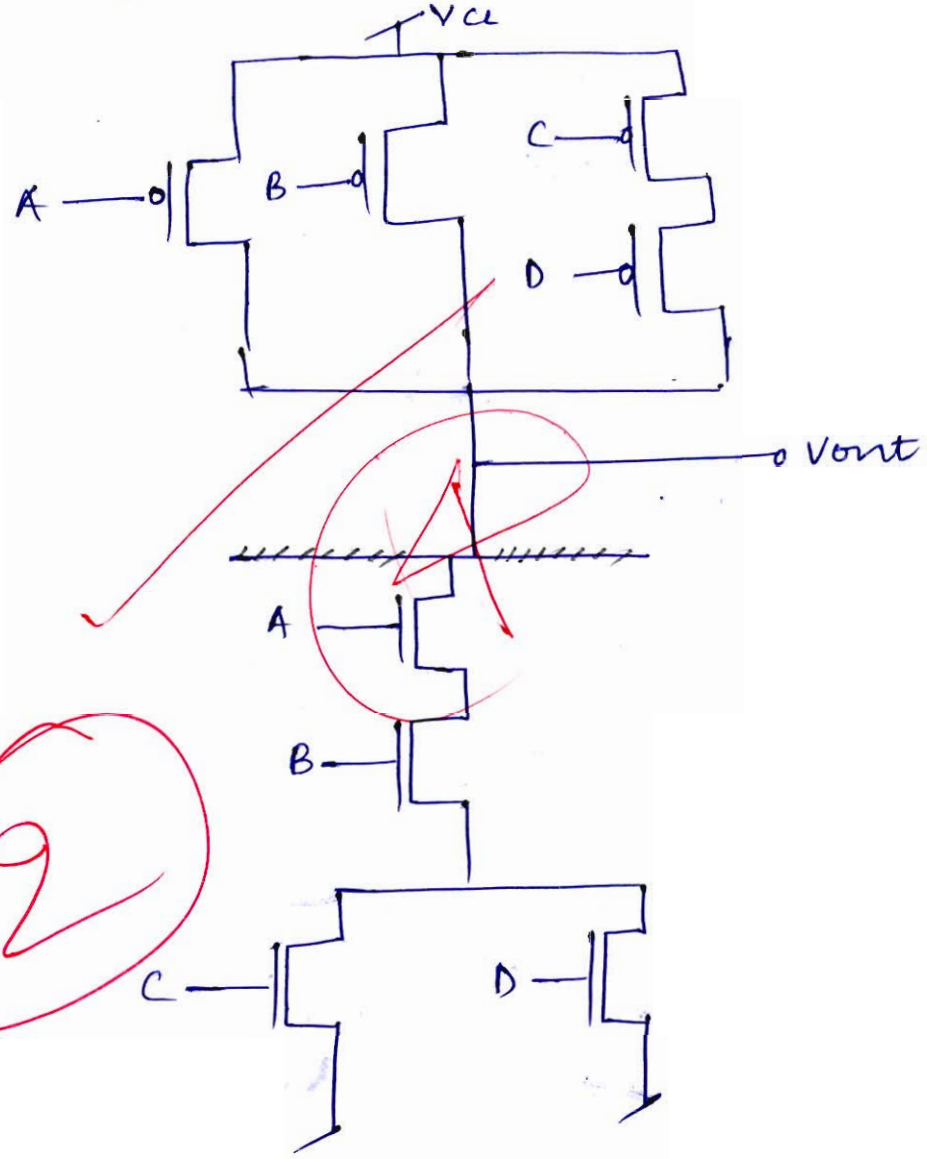
$Y \Rightarrow (\overline{AB} + \overline{C+D})$

$= \overline{(AB)(C+D)} \Rightarrow \overline{AB} + \overline{C+D}$

$= (\overline{A} + \overline{B} + \overline{(C+D)})$

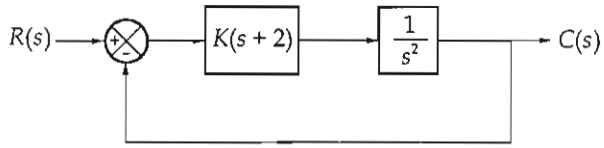
hence $Y = \overline{(AB)(C+D)}$

⇒



2

Q.6 (a) **(i)** Consider the block diagram shown below:



Determine the value of K such that the phase margin of the system is 50°.

(ii) A negative feedback control system has open loop transfer function,

$$G(s)H(s) = \frac{K(s+2)}{s(s-1)}$$

Find the value of system gain K so that the damping ratio of the system is $\frac{1}{\sqrt{2}}$.

[12 + 8 marks]

→ *i) The open loop transfer fn of the given block diagram is

$$g(s) = \left[\frac{K(s+2)}{s^2}\right]$$

* The phase margin of the system is calculated at gain cross over frequency

⇒ $180° - [\text{phase of the system}]_{\text{at } \omega_{gc}} = \text{phase margin}$

$$\text{phase } \angle G(s) = \tan^{-1}\left(\frac{\omega_{gc}}{2}\right) - (180°)$$

Phase Margin $= \left(180° + \tan^{-1}\frac{\omega_{gc}}{2} - 180°\right) = 50°$

$$\Rightarrow \tan^{-1}\left[\frac{\omega_{gc}}{2}\right] = 50°$$

$$\frac{\omega_{gc}}{2} = 1.191$$

$$\omega_{gc} = 2.383 \text{ rad/sec}$$

* for ω_{gc}, the value of

$$|G(j\omega)| = 1$$

Hence for (ω_{gc}) to lie on $G(j\omega)$

$$\left| \frac{K(s+2)}{s^2} \right|_{s=j\omega_{gc}} = 1$$

$$\frac{K\sqrt{4+(\omega_{gc})^2}}{(\omega_{gc})^2} = 1$$

$$K = \frac{(\omega_{gc})^2}{\sqrt{4+(\omega_{gc})^2}}$$

$$= \frac{(\omega_{gc})^2}{3.111}$$

$$\boxed{(K = 1.826)}$$

$\frac{3.111}{5.678}$

hence the value of gain K, for phase margin of the system = 60°,

$$\underline{(k = 1.826)}.$$

(ii) $G(s) = \frac{K(s+2)}{s(s-1)}$

Closed loop transfer function of the system will be

$$T(s) = \frac{C(s)}{R(s)} = \frac{G(s)}{1+G(s)}$$

$$T(s) = \frac{\frac{K(s+2)}{s(s-1)}}{1+\frac{K(s+2)}{s(s-1)}} = \frac{K(s+2)}{s^2-s+K(s+2)}$$

hence the characteristic eqn of the given transfer fn is;

$$s^2-s+K(s+2) = \boxed{s^2+(k-1)s+2k=0}$$

* comparing it with the general characteristic eqn,

$(s^2+2\xi\omega_n s+\omega_n^2=0)$

$$\omega_n^2 = 2k$$

$$\omega_n = (\sqrt{2k})$$

$$2\xi\omega_n = (k-1)$$

given $\xi = (1/\sqrt{2})$

$$\frac{2 \times \sqrt{2k}}{\sqrt{2}} = (k-1)$$

$$2\sqrt{k} \Rightarrow (k-1)$$

$$\Rightarrow 4k = k^2+1-2k$$

$$\Rightarrow (k^2-6k+1=0)$$

hence $\boxed{(k=5.828,\ k=0.1715)}$

for $k = (0.1715)$

$(2\xi\omega_n < 1)$ hence not acceptable,

$\therefore \boxed{k = (5.828)}$

Ans = gain $k = 5.828$

Q.6 (b) In a power plant, three digital signals: drum level (D), water flow (W) and steam temperature (S) are used to control a particular system by a feedback signal (F) that comes from the field to the control room.

(i) Find the minimised logic expression that generates a high feedback signal (F) whenever any one of the conditions is satisfied.

C_1 : All the levels are at zero.

C_2 : Level D and S set to zero.

C_3 : Level W and S set to zero.

C_4 : Level D set to zero.

C_5 : All the levels are high.

(ii) Draw the logic circuit using the expression obtained in part (i) that generates a high feedback (F), using only two-input NAND gates.

[15 + 5 marks]

D	W	S	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

0 → OFF

1 = ON

$F = \Sigma m(0, 1, 2, 3, 4, 7)$

	$\bar{W}\bar{S}$	$\bar{W}S$	WS	$W\bar{S}$
$\bar{D}$	1	1	1	1
D	1	0	1	0

0 1 3 2

4 5 7 6

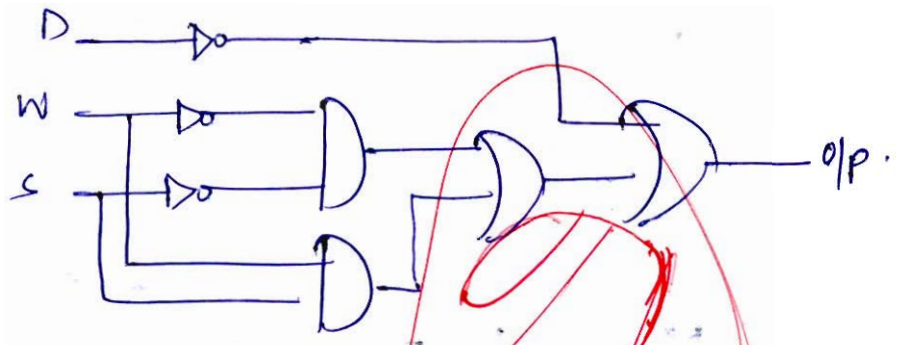
$F = [\bar{D} + \bar{W}\bar{S} + WS]$

↓

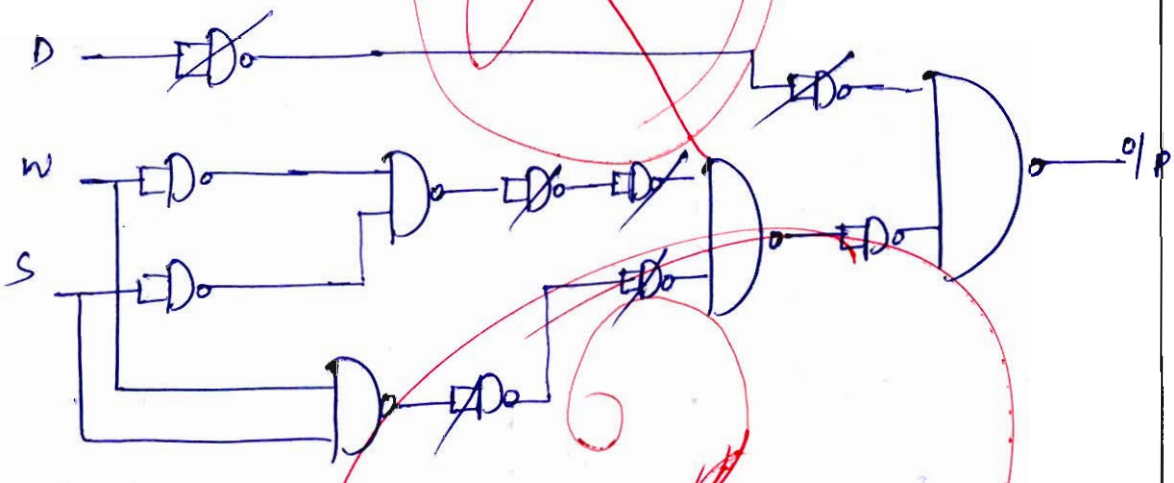
minimised logic expression

11) (*) Logic implementation

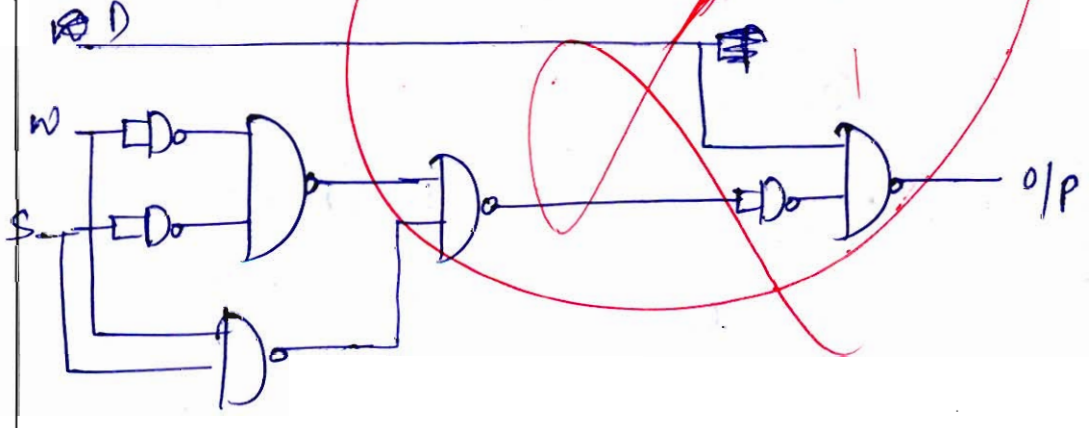
$F = \bar{D} + \bar{W}\bar{S} + WS$



using NAND gates



⇒



Q.6 (c) Using Nyquist criterion investigate the closed-loop stability of the system whose open-loop transfer function is,

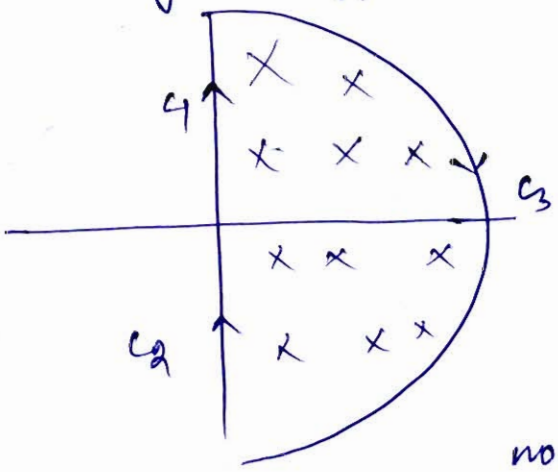
$$G(s)\,H(s) = \frac{K(s+1)}{(s+0.5)(s-2)}$$

For **(i)** $K = 1.25$ and **(ii)** $K = 2.5$

(iii) Also determine the limiting value of K for stability.

[20 marks]

* Drawing the Nyquist Contour,



* Since the given system contains 1 pole (open loop) in the right side of the s plane,

∴ By Nyquist stability criteria the no. of encirclements of (-1,0) should be (-1) in anticlockwise direction for the system to be stable.

* Along C_1.

$s = j\omega$ where $\omega = (0 \to \infty)$.

ω	M	φ
0	K	-180°
∞	0	-90°

$$\varphi = \tan^{-1}(\omega) - \tan^{-1}\left(\frac{\omega}{0.5}\right) - \left[\tan^{-1}\left(\frac{\omega}{-2}\right)\right]$$

$$= \tan^{-1}(\omega) - \tan^{-1}(2\omega) - \left[180^\circ - \tan^{-1}\left(\frac{\omega}{2}\right)\right]$$

$$\varphi = \tan^{-1}(\omega) - \tan^{-1}(2\omega) - 180^\circ + \tan^{-1}(\omega/2)$$

$s^2 - 2s + 0.5s - 1 + 1.5s +$

$s^2 - 2s + 0.5s - 1$

$Ks + K$

$s^2 + (k - 1.5)s + (k+1)$

$k+1$

$s^2 \quad 1 \quad (k+1)$

$s^1 \quad (k-1.5) \quad (k+1)$

so

$\frac{ks+1}{(s+k_2)(s-2)}$

$\Rightarrow$ ①

$\varphi = \tan^{-1}(\omega)$

$-\tan^{-1}(2\omega)$

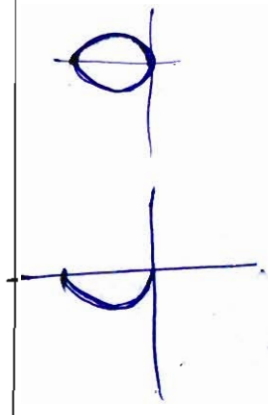
$-180 + \tan^{-1}(\omega/2)$

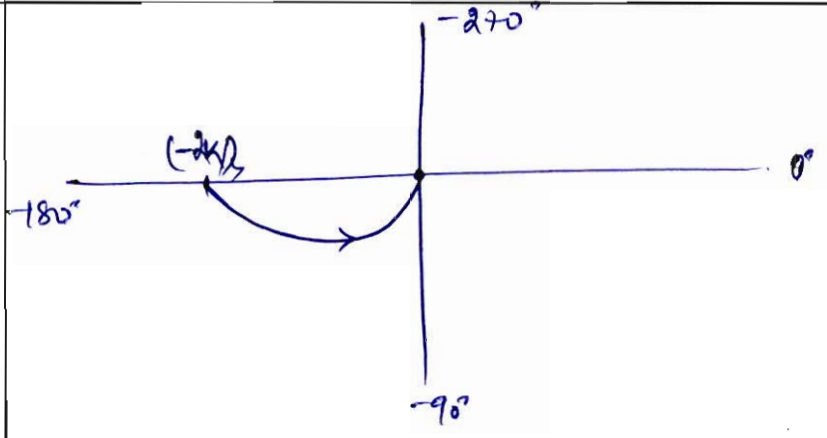
$\frac{k(1)}{0.5 \times 1}$

2

$\varphi =$

$+180 \quad -180^\circ -$





* Along ($j\omega$)

$s = j\omega$ where $0 < \omega < \infty$

ω	M	φ
0	K	$-180°$
∞	0	

$$\varphi = \tan^{-1}(\omega) - \tan^{-1}\left(\frac{\omega}{0.5}\right) - \left[\tan^{-1}\left(\frac{\omega}{-2}\right)\right]$$ (3rd quad)

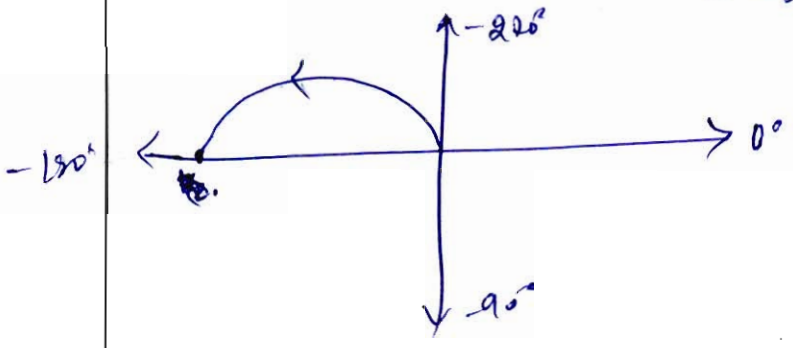
$$\overset{(\omega = -\omega)}{=} -\tan^{-1}(\omega) + \tan^{-1}\left(\frac{\omega}{0.5}\right) - \left[180° + \tan^{-1}\left(\frac{\omega}{2}\right)\right]$$

$$\Rightarrow -\tan^{-1}(\omega) + \tan^{-1}(2\omega) - \tan^{-1}(\omega/2) - 180°$$

at $(\omega = 0)$ $\varphi = (-180°)$

$\omega = (\infty) \Rightarrow \varphi = -90° + 90° - 90° - 180°$

$= -270°$ or $+90°$



ω	M	φ
$-\infty$	0	$-270°$
0	2K	$-180°$

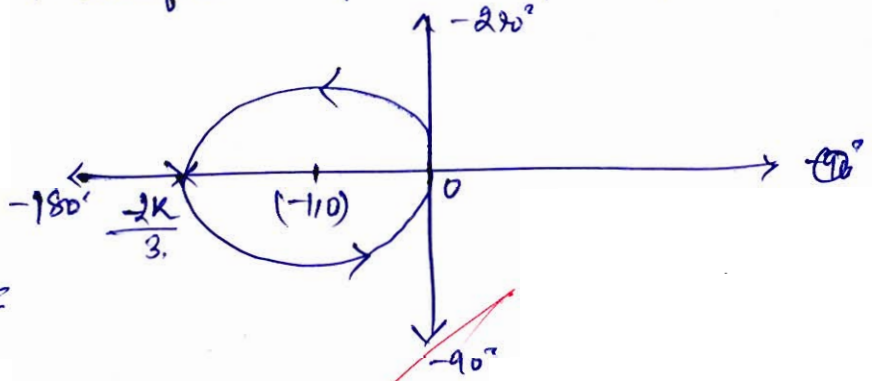
Along C_3 $\Rightarrow (Re^{j\theta})$ $\left(\frac{\pi}{2} < \theta < -\frac{3\pi}{2}\right)$

$\lim_{R \to \infty}$

$\Rightarrow \dfrac{K(Re^{j\theta}+1)}{(Re^{j\theta}+1/2)(Re^{j\theta}-2)}$

$\rightarrow$ at $R \to \infty$ $\quad G(s) = 0$.

* Therefore complete Nyquist plot is



(1)

i) for $K = (1.25)$

ii) Since there is only 1 encirclement, hence the system is stable,

at $K = (1.25)$, cutting pt $= \dfrac{-2 \times 1.25}{3} = (-0.833)$

iii) Hence no encirclements = Unstable

(2) $K = (2.8)$ cutting pt $= \dfrac{-2 \times 2.5}{3} = -1.66$

Hence 1 encirclement = stable

(3) Limiting value

$\dfrac{-2K}{3} \leq -1$

$\boxed{(K \geq 3/2)}$

Q.7 (a) A unity feedback control system has an open loop transfer function,

$$G(s)=\frac{K\left(s+\frac{4}{3}\right)}{s^2(s+12)}$$

Sketch the complete root locus. Also, find the value of K for which all roots are equal, what is the value of these roots?

[20 marks]

Sol^n *

1) No. of poles = 3 at $(s=0,0,-12)$

No. of zeros = 1 at $(s=-4/3)$

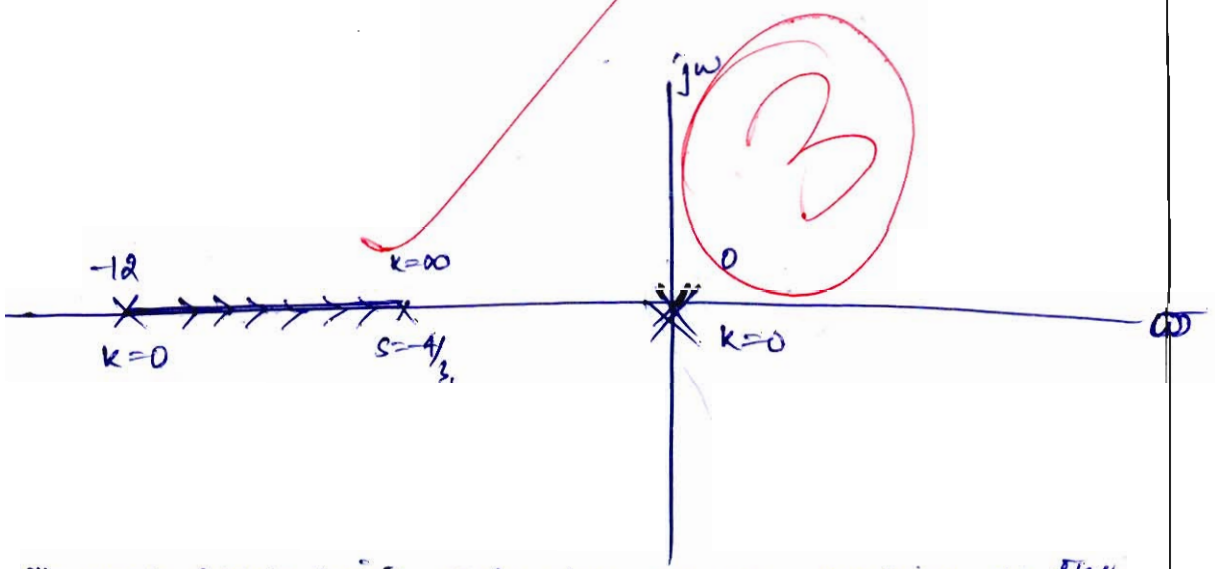
→ No. of Branches of root locus = $(p=3)$.

→ No. of asymptotes of root locus = $(p-z) = 2$

→ Centroid = $\frac{\Sigma(\text{real } p) - \Sigma \text{real}(z)}{(p-z)} = \left(\frac{-12+4/3}{2}\right)$

$= \left(\frac{-32}{6}\right)$.

→ Angle of asymptotes = $\frac{(2k+1)180^\circ}{2} = 90^\circ, 270^\circ$.



* root locus exists only for those portions on the real axis where the no of poles and zeros are odd to the right of the point.

→ The point where root locus cuts the jω axis, can be calculated by RH criteria

$$q(s) = \left(s^3 + 12s^2 + 4s + \frac{4K}{3}\right)$$

s^3	1	K
s^2	12	$4K/3$
s^1	$\frac{12K - 4K/3}{12}$	
s^0	$4K/3$	

The point where cuts jω axis

coeff of $s^1 = 0$

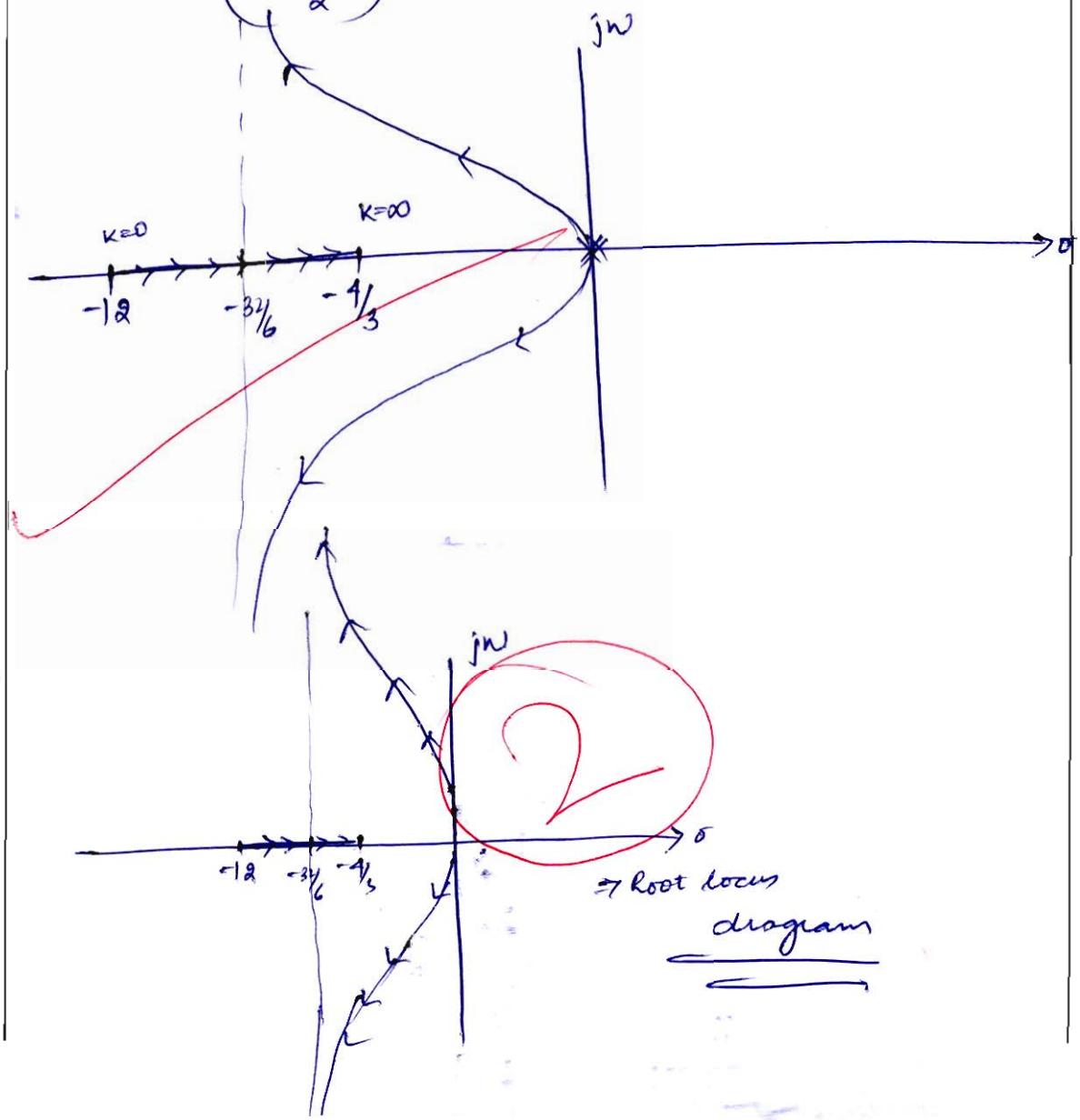
$\Rightarrow \therefore (K = 0)$.

$s^3 + 12s^2 + 4s + \frac{4K}{3}$

s^3	1	K
s^2	12	$4K/3$
s^1		
s^0		

* Centroid

$\Rightarrow \left(\frac{-12 + 4/3}{2}\right) = -5.33.$



⇒ Root locus diagram

✱. The value of k for which are the roots are equal)

Hence $\left(s^3 + 12s^2 + ks + \frac{4k}{3}\right)$

↓

This should be a perfect cube.

$(s+a)^3 = s^3 + a^3 + 3as(a+s)$

$= s^3 + a^3 + 3a^2s + 3as^2$

↓

Comparing with $\left(s^3 + 12s^2 + ks + 4k/3\right)$

$\Rightarrow$ • $(3a^2 = k)$

$3as^2 = 12s^2$

$a = (4)$.

$\frac{4k}{3} = (a^3)$

64

$\frac{4 \times 48}{3}$

$(3a^2 = k)$

$(3 \times 16) \Rightarrow 48$.

Hence the value of k for which all the roots are equal $= \boxed{k = 48}$

Ans $= (k = 48)$

$(s = -4)$.

Q.7 (b) A switching circuit has two control inputs (C_1 and C_2), two data inputs (X_1 and X_2) and one output (Z). The circuit performs one of the logic functions AND, OR, XOR, XNOR depending upon the control inputs. The output is equal to $X_1 + X_2$ for $C_1C_2 = 00$; $X_1 \oplus X_2$ for $C_1C_2 = 01$; X_1X_2 for $C_1C_2 = 10$; and $X_1 \odot X_2$ for $C_1C_2 = 11$. Find all the possible minimal expressions for logic function Z.

[20 marks]

⇒

C_1	C_2	X_1	X_2	Z	
0	0	0	0	0	$(X_1 + X_2)$
0	0	0	1	1	
0	0	1	0	1	
0	0	1	1	1	
0	1	0	0	0	$X_1 \oplus X_2$
0	1	0	1	1	
0	1	1	0	1	
0	1	1	1	0	
1	0	0	0	0	X_1X_2
1	0	0	1	0	
1	0	1	0	0	
1	0	1	1	1	
1	1	0	0	1	$X_1 \odot X_2$ (XNOR)
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	1	

* The overall minimal expression of the logic function z is.

$$z = \Sigma m(1,2,3,5,6,11,12,15)$$

C_1C_2 \ X_1X_2	$\bar{X}_1\bar{X}_2$	$\bar{X}_1X_2$	X_1X_2	$X_1\bar{X}_2$
$\bar{C}_1\bar{C}_2$	0	1	1	1
$\bar{C}_1C_2$	0	1	0	1
$C_1\bar{C}_2$	1	0	1	0
C_1C_2	0	0	1	0

0 1 3 2
4 5 7 6
12 13 15 14
8 9 11 10

$$\Rightarrow \boxed{z = \bar{C}_1(\bar{X}_1X_2) + \bar{C}_1(X_1\bar{X}_2) + C_1C_2\bar{X}_1\bar{X}_2 + C_1(X_1X_2)} + (\bar{C}_1\bar{C}_2X_1)$$

overall minimal expression for z.

* In terms of single expressions

$$z = z_1 + z_2 + z_3 + z_4$$

where

$$z_1 = \bar{C}_1\bar{C}_2(X_1 + X_2)$$

$$z_2 = \bar{C}_1C_2(X_1 \oplus X_2)$$

$$z_3 = C_1\bar{C}_2[X_1X_2]$$

$$z_4 = C_1C_2[X_1 \odot X_2]$$

Q.7 (c) Design combinational circuits for the following Boolean functions as instructed.

(i) Implement $F = \bar{A}\bar{B}\bar{D} + \bar{A}BD + ABC\bar{D} + A\bar{B}CD$ using 8 × 1 MUX and a NOT gate.

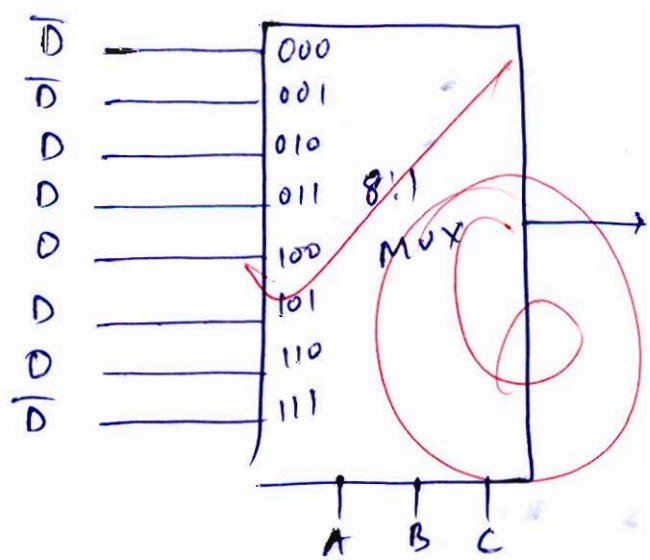
(ii) Implement $F = (A_0 \oplus A_2) + (A_1 \odot A_3)$ using only 2 × 1 MUX circuits and basic inputs A_0, A_1, A_2, A_3, 0 and 1.

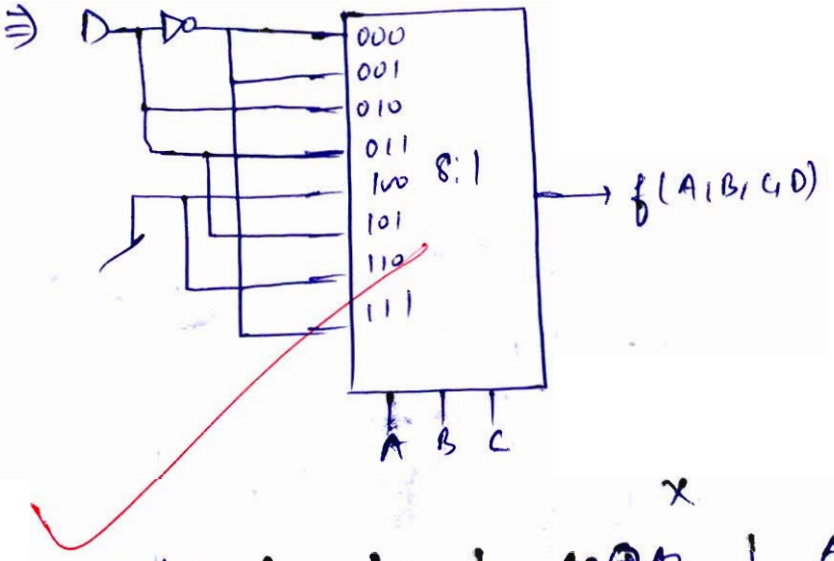
[10 + 10 marks]

1)

A	B	C	D	f	
0	0	0	0	1	$\bar{D}$
0	0	0	1	0	
0	0	1	0	1	$\bar{D}$
0	0	1	1	0	
0	1	0	0	0	D
0	1	0	1	1	
0	1	1	0	0	D
0	1	1	1	1	
1	0	0	0	0	0
1	0	0	1	0	
1	0	1	0	0	D
1	0	1	1	1	
1	1	0	0	0	0
1	1	0	1	0	
1	1	1	0	1	$\bar{D}$
1	1	1	1	0	

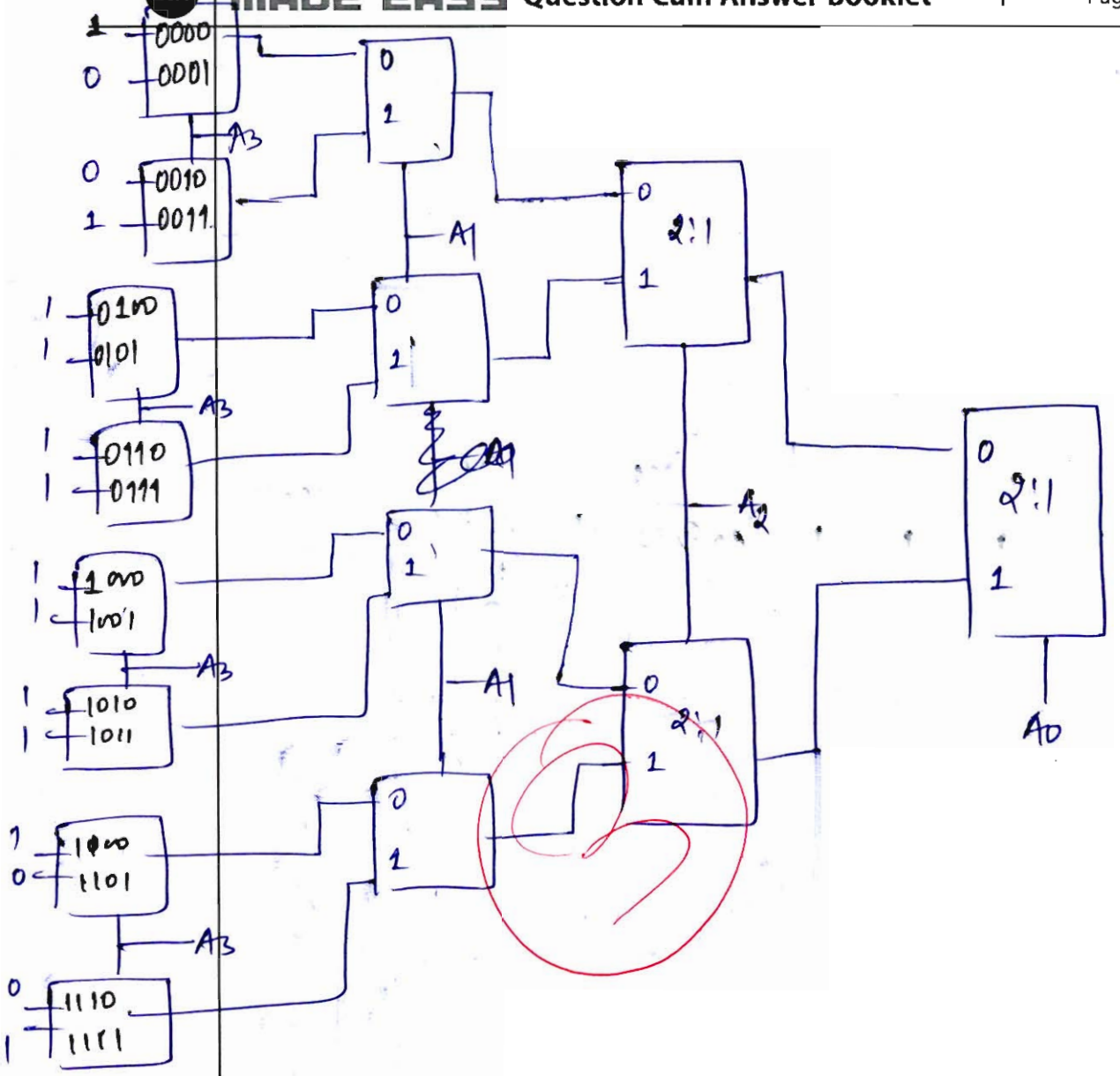
$F = \Sigma m(\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + AB\bar{C}\bar{D} + A\bar{B}CD)$





(ii)

A_0	A_2	A_1	A_3	$A_0 \oplus A_2$ (x)	$A_1 \odot A_3$ (y)	x + y
0	0	0	0	0	1	1
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	1	1	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	1	1
1	0	0	0	1	1	1
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	1	1



2:1 MUX implementation

Q.8 (a) A control system with unity negative feedback has an open loop transfer function,

$G(s) = \dfrac{K}{s(s+1)(0.1s+1)}$ and input, $r(t) = 10tu(t)$.

(i) Determine the steady state error (e_{ss}) for $K = 2$.

(ii) Find the minimum value of K for which, $e_{ss} \leq 0.1$ for a unit ramp input.

(iii) For the value of K obtained in part (ii), obtain the closed loop transfer function of the system and thereby find the stability of system using *R-H* criteria.

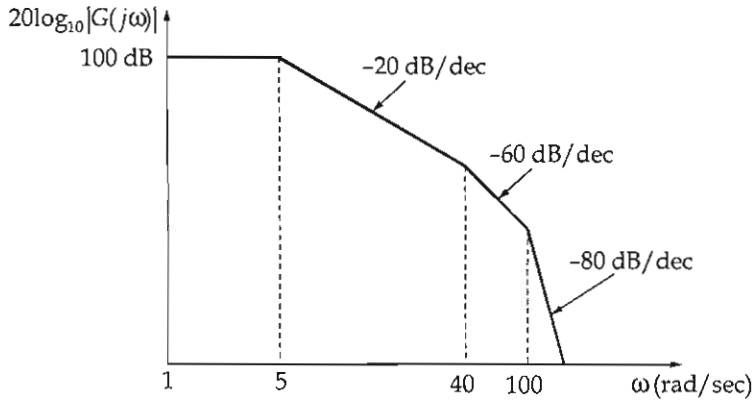
[8 + 4 + 8 marks]

Q.8 (b) Define the terms: Minimum-phase system, Non-minimum phase system and all-pass system.

The magnitude plot of the open loop transfer function $G(s)$ of a certain system is shown in the figure below:

(i) Determine $G(s)$ if it is known that the system is of Minimum phase type.

(ii) Estimate the phase of $G(j\omega)$ at each of the corner frequencies.



[20 marks]

Q.8 (c) (i) What are the Hazards that occur while designing a combinational circuit? Discuss different types of Hazards.

(ii) Design a square wave generator of output frequency (f_s) using a single 2 × 1 MUX circuit which suffers from a propagation delay of 10 ns. Also draw its output waveform and calculate the value of frequency (f_s).

[10 + 10 marks]

OOOO

Space for Rough Work

Space for Rough Work

Space for Rough Work

1
000 1
001
010
011
100 1
101
110
111

$180° - (\text{phase}) \Rightarrow 50°$

$=$

$(130°)$.

$\left(\frac{s^2 - 2s + 5/9 - 1 + Ks + K}{s^2 - \frac{3}{9}s + Ks + K - 1}\right) \tan^{-1}(w/2) - 2\tan^{-1}\left(\frac{1w}{0}\right) \tan^{-1}(w/2) - 180°$

$s^2 + \left(K - \frac{3}{2}\right)s + K - 1$

$(s+0.5)(s-2) + K(s+1)$

$s^2 - 2s + \frac{5}{2} - 1 + K(s) + K$

$\Rightarrow s^2 + \left(K - \frac{3}{2}\right)s + (K-1)$

$\left(s^3 + 12s^2 + Ks + 4K/3\right)$ perfect cube

$(s+a)^3 = s^3 + a^3 + 3as(a+s)$

$\Rightarrow a^3 = 4K/3$

$(3as^2)$

$\Rightarrow (4)$

$a = (4)$.

s^2	1	
s^1	$(K+1.5)$	
s^0	$(K-1)$	

$K + 1.5$

0 1 3 2
4 5 7 6

$\overline{D}$ 4

$s^3 + 12s^2 + Ks + 4K/3 = 0$

$(a = 4)$

D W S

000	1
001	1
010	1
011	1
100	1
101	
110	
111	1

$\lim_{s \to 0} \frac{K \times 8}{8(s(a))}$

$s^2 + 0 - 0.25s + 0.25$

s^2	1	$K-1$
s^1	$K - 3/2$	
s^0		

$\left(\frac{K(s+2)}{s^2}\right)$

$\left(K = 3/2\right)$

$\left(\frac{\omega^2 + 1}{\left(\omega^2 + 1/4\right)\left(\omega^2 + 4\right)}\right)$ $= (K)$.

$\varphi = \tan^{-1}(\omega) - \tan^{-1}(2\omega) - \left[\tan^{-1}\left(\frac{\omega}{-2}\right)\right]$

$\tan^{-1}(\omega) - \tan^{-1}(2\omega) - \left(180° - \tan^{-1}\left(\frac{\omega}{2}\right)\right)$

$2\tan^{-1}(\omega) + \tan^{-1}(\omega/2) - \tan^{-1}(2\omega) - 180°$

$2(-180°)$

$(K = 1)$

$K = \frac{1}{2}\left(\frac{2}{3}\right)$.

$\left(\frac{K \times 3/2}{2/3} = 1\right)$