ESE 2024

Main Exam Detailed Solutions

Electronics & Telecom. Engineering

PAPER-II

EXAM DATE : 23-06-2024 | 2:00 PM to 5:00 PM

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ANALYSIS

Electronics and Telecom. Engineering Paper-II
ESE 2024 Main Examination

Sl.	Subjects	Marks
1.	Analog and Digital Communication Systems	70
2.	Control Systems	80
3.	Microprocessors and Microcontrollers	30
4.	Electromagnetics	90
5.	Signals and Systems	16
6.	Computer Organization and Architecture	80
7.	Advanced Communication	80
8.	Advanced Electronics	34
	Total	**480**

Scroll down for detailed solutions

Section-A

Q.1 (a) An angle-modulated signal has the form

$$u(t) = 100\cos(2\pi f_c t + 4\sin 2000\pi t]$$

Where $f_c = 10$ MHz.

(i) Determine the average transmitted power.

[4 marks : 2024]

(ii) Determine the peak phase and frequency deviation.

[4 marks : 2024]

(iii) Is this FM or PM signal? Explain.

[2 marks : 2024]

Solution:

$$u(t) = 100\cos[2\pi f_c t + 4\sin 2000\pi t]$$
$$f_c = 10 \text{ MHz}$$

(i) Average transmitted power, $P = \dfrac{A_c^2}{2R}$

$$= \frac{(100)^2}{2\times 1}; \quad \text{Default } R = 1\ \Omega$$
$$= 5 \text{ kW}$$

(ii)
$$u(t) = 100\cos[2\pi f_c t + 4\sin 2000\pi t]$$
$$S_{angle}(t) = A_c\cos[2\pi f_c t + \phi(t)]$$

Peak phase deviation, $\Delta\phi = |\phi(t)|_{max}$

$$= |4\sin 2000\pi t|_{max}$$
$$\Delta\phi = 4 \text{ rad}$$

Peak frequency deviation, $\Delta f = \left|\dfrac{1}{2\pi}\dfrac{d}{dt}\phi(t)\right|_{max}$

$$= \left|\frac{1}{2\pi}[4\times 2000\pi\cos 2000\pi t]\right|_{max}$$
$$= |4000\cos 200\pi t|_{max}$$
$$\Delta f = 4000 \text{ Hz} = 4 \text{ kHz}$$

(iii) It can be visualised as both FM and PM signals.

$$S_{PM}(t) = A_c\cos[2\pi f_c t + k_p m(t)]$$
$$k_p m(t) = 4\sin 2000\pi t$$

It can be visualised as PM signal, with

$$k_p = 4\frac{\text{rad}}{\text{volt}} \text{ and } m(t) = \sin 2000\pi t$$

$$s_{Fm}(t) = A_c\cos\left[2\pi f_c t + 2\pi k_f\int_{-\infty}^{t} m(t)dt\right]$$

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$$2\pi k_f \int_{-\infty}^{t} m(t)dt = 4 \sin 2000\,\pi t$$

$$2\pi k_f m(t) = 4 \times 2000\pi \cos 2000\pi t$$

$$k_f m(t) = 4 \times 1000 \cos 2000\pi t$$

It can be visualised as FM signal,
with $k_f = 4000$ Hz/Volt and $m(t) = \cos 2000\pi t$

End of Solution

Q.1 (b) A unity feedback control system has the open-loop transfer function

$$G(s) = \frac{K}{s(Ts+1)}$$

The system is critically damped and the steady-state error is 0.5 when unit ramp input is applied. Find out the natural frequency of the system.

[10 marks : 2024]

Solution:

$$G(s) = \frac{K}{s(1+sT)}$$

System is critically damped $\Rightarrow \xi = 1$

$$e_{ss} = 0.5$$

input applied is ramp

$$\omega_n = ?$$

Characteristic equation is $1 + G(s) = 0$

$$1 + G(s) = 1+\frac{K}{s(1+sT)} = 0$$

Characteristic equation becomes $s^2 + \frac{s}{T} + \frac{K}{T}$

On comparing with standard second order equation $s^2 + 2\xi\omega_n s + \omega_n^2$

We get,

$$2\xi\omega_n = \frac{1}{T}$$

$$\omega_n^2 = \frac{K}{T}$$

$$\omega_n = \sqrt{\frac{K}{T}} \text{ rad/sec}$$

$$2 \times 1 \times \omega_n = \frac{1}{T} \quad \text{...(1)}$$

$$\omega_n = \sqrt{\frac{K}{T}} \quad \text{...(2)}$$

From (1) and (2), we get

$$\omega_n = \frac{1}{2T} = \sqrt{\frac{K}{T}}$$

$$\frac{1}{2T} = \sqrt{\frac{K}{T}}$$

$$\frac{1}{4T^2} = \frac{K}{T}$$

$$T = 4KT^2$$

$$\frac{1}{4K} = T \qquad \therefore \quad T = \frac{1}{4K} \qquad ...(3)$$

$$K_V = \underset{s\to 0}{lt}\ sGH(s)$$

$$K_V = \underset{s\to 0}{lt}\ s\frac{K}{s(1+sT)}$$

$$K_V = \frac{K}{1} = K$$

$$e_{ss} = \underset{s\to 0}{lt}\frac{A}{K_v} = \underset{s\to 0}{lt}\frac{1}{K}$$

$$\frac{0.5}{10} = \frac{1}{K} \qquad \therefore \quad K = 2$$

∴ from equation (3), we get

$$T = \frac{1}{4\times 2} = \frac{1}{8}$$

Now, from equation (2)

$$\omega_n = \sqrt{\frac{K}{T}}$$

$$\omega_n = \sqrt{\frac{2}{\left(\frac{1}{8}\right)}} = \sqrt{2\times 8}$$

$$\omega_n = 4 \text{ rad/sec}$$

End of Solution

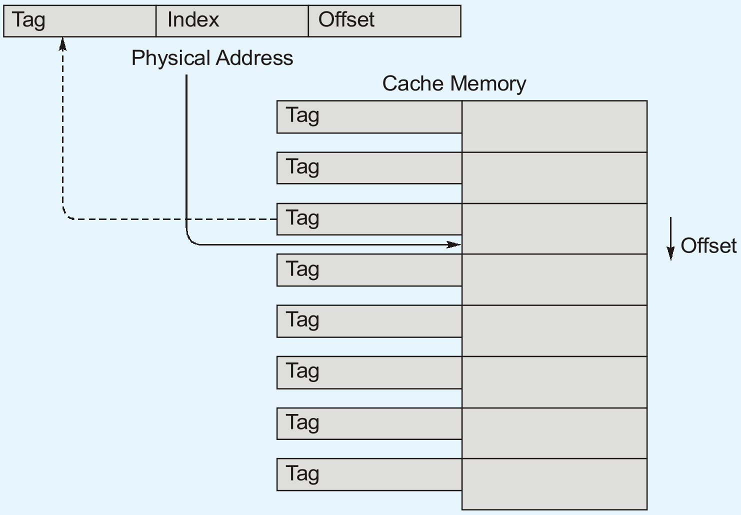
Q.1 (c) With respect to cache memory organization, describe the importance of cache addressing models, considering physical address cache, virtual address cache and aliasing problem. Write a block schematic depicting memory hierarchy for a shared memory multiprocessor.

[10 marks : 2024]

Solution:

Importance of cache addressing models:

When a CPU generates physical address, the access to main memory precedes with access to cache. Data is checked in cache by using the tag and index/set bits as shown in the below diagram. Such cache where the tag and index bits are generated from physical address is called as a Physically Indexed and Physically Tagged (PIPT) cache. When there is a cache hit, the memory access time is reduced significantly.



Average Memory Access Time = Hit Time + Miss Rate× Miss Penalty

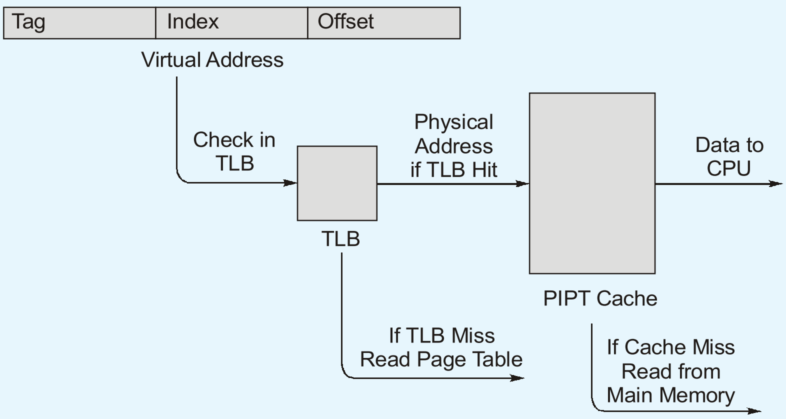
Here, Hit Time= Cache Hit Time= Time it takes to access a memory location in the cache

Miss Penalty= time it takes to load a cache line from main memory into cache.

In today's systems, CPU generates a logical address (also called virtual address) for a process. When using a PIPT cache, the logical address needs to be converted to its corresponding physical address before the PIPT cache can be searched for data. This conversion from logical address to physical address includes the following steps:

1. Check the logical address in the TLB (translation look aside buffer) If it is present in TLB, get the physical address of page from the TLB.
2. If it is not present, access the page table from physical memory and then use the page table to obtain the physical address.

All this time adds to the hit time. Hence, hit time = TLB latency + cache latency



Limitations of PIPT Cache

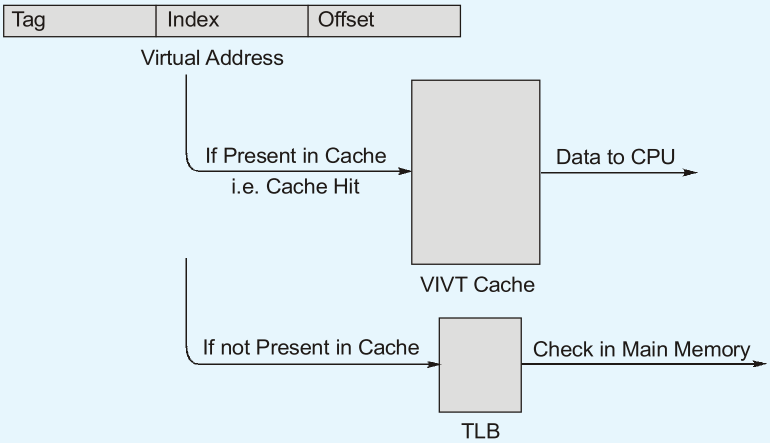
1. This process is quite sequential hence high hit time.
2. Not ideal for inner level caches.
3. Data cache is accessed frequently by any system and TLB access for data every time will slow the system significantly.

Virtually Indexed Virtually Tagged Cache:

An immediate solution appears to be a Virtually Indexed Virtually Tagged (VIVT) cache. VIVT cache directly checks the data in cache and fetch it without translating it to physical address reducing the hit time significantly.

In such a cache, the tag and index will be a part of the logical/virtual address generated by CPU. Now the address generated directly by the CPU can be used to fetch the data reducing the hit time significantly.

Only if the data is not present in cache, TLB will be checked and finally after converting to physical address, the data will be brought into the VIVT cache. Hence, hit time for VIVT = cache hit time.

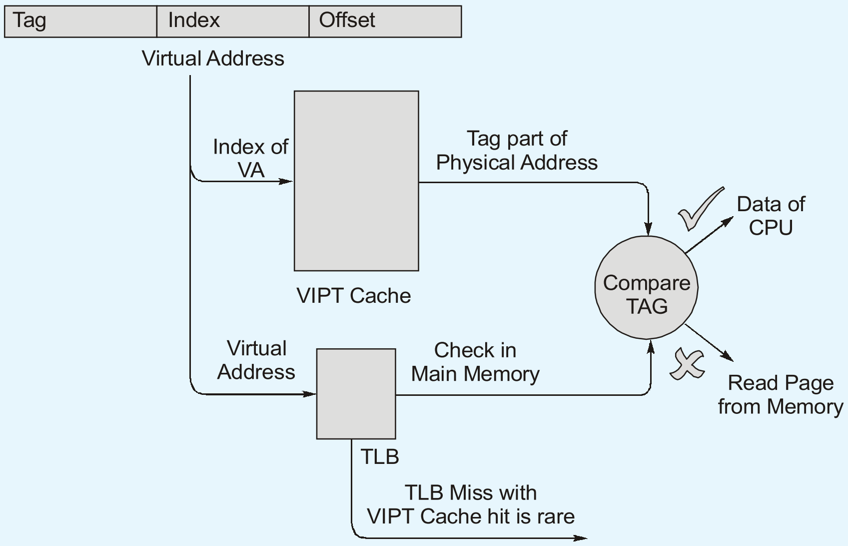


Limitations of VIVT Cache:

1. The TLB contains important flags like the dirty bit and invalid bit so even with VIVT cache, TLB needs to be checked anyways.
2. **Lots of cache misses on context switch:** Since the cache is specific to logical address and each process has its own logical address space, two process can use the same address but refer to different data.

Virtually Indexed Physically Tagged Cache (VIPT)

The VIPT cache uses tag bits from physical address and index as index from logical/ virtual address. The cache is searched using the virtual address and tag part of physical address is obtained. The TLB is searched with virtual address, and physical address is obtained. Finally, the tag part of physical address obtained from the VIPT cache is compared with physical address's tag obtained from TLB. If they both are same, then it is a cache hit else a cache miss.



Since TLB is smaller in size than cache, TLB's access time will be lesser than Cache's access time. Hence, hit time= cache hit time.

VIPT cache takes same time as VIVT cache during a hit and solves the problem VIVT cache:

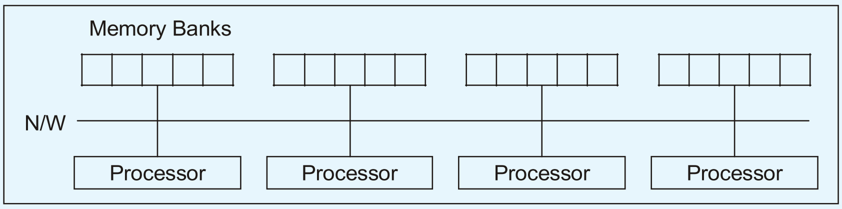
1. Since the TLB is also accessed in parallel the flags can be checked at the same time.
2. The VIPT cache uses part of physical address as index and since every memory access in the system will correspond to a unique physical address, data for multiple processes can exist in the cache and hence no need to flush data for every context switch.

Remember that this is the same reason for having a page table for every process. This means that for every context switch, the cache needs to be flushed and every context switch follows with a lot of cache misses both of which is time-consuming and adds to the hit time.

A solution to these problems is Virtually Indexed Physically Tagged Cache (VIPT Cache). The next sections in the article covers VIPT Cache, challenge in VIPT Cache and some solutions

Shared memory multiprocessor may be symmetric multiprocessor (SMP) processors, in which the access to a word of memory takes the same time no matter which processor accesses it (or) which word is accessed and the nonuniform memory access multiprocessors which does not have the equal access characteristics.

A shared memory multiprocessor is an architecture consisting of a modest number of processors, all of which have direct (H/w) access to all the main memory in the system.



This permits any of the system processors to access data that any of the other processors has created (or) will use.

The key to this form of multiprocessor Architecture is the interconnection network that directly connects all the processors to the memories.

This is complicated by the need to retain cache coherence across all caches of all processors in the system.

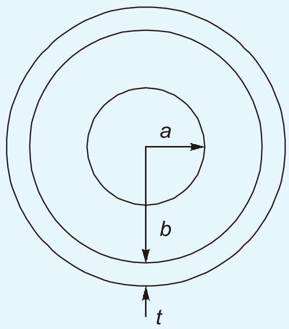
End of Solution

Q.1 (d) For an air-filled coaxial transmission line, the outer radius of the inner conductor is 1 mm and the inner radius of the outer conductor is 4 mm. The outer conductor thickness is 0.6 mm and all conductors have conductivity $\sigma = 1.6 \times 10^7$ S/m. Find the inductance L and capacitance C per unit length. What will be the resistance per unit length at an operating frequency of 2.5 GHz? The value of $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m and $\mu_0 = 4\pi \times 10^{-7}$ H/m.

[10 marks : 2024]

Solution:

Given data: $a = 1$ mm ; $b = 4$ mm ; $t = 0.6$ mm ; $\sigma = 1.6 \times 10^7$ S/m



(a) Inductance per unit length L:

$$L = \frac{\mu}{2\pi} \ln\left[\frac{b}{a}\right]$$

$$\Rightarrow \quad L = \frac{4\pi \times 10^{-7}}{2\pi} \ln\left[\frac{4}{1}\right] = 0.277\ \mu\text{H/m}$$

(b) Capacitance per unit length, C:

$$C = \frac{2\pi\epsilon}{\ln\left(\frac{b}{a}\right)}$$

$$\Rightarrow \quad C = \frac{2\pi \times 4\pi \times 10^{-7}}{\ln\left[\frac{4}{1}\right]} = 5.70\ \mu\text{F/m}$$

(c) Resistance per unit length, R:

$$R = \frac{1}{2\pi\delta\sigma_c}\left[\frac{1}{a} + \frac{1}{b}\right]; \quad \delta = \frac{1}{\sqrt{\pi f \mu\sigma}} = 2.52\ \mu\text{m}$$

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$$R = \frac{10^3}{2\pi \times 2.52 \times 10^{-6} \times 1.6 \times 10^7}\left[1 + \frac{1}{4}\right]$$

$$R = 4.93\ \Omega/\text{m}$$

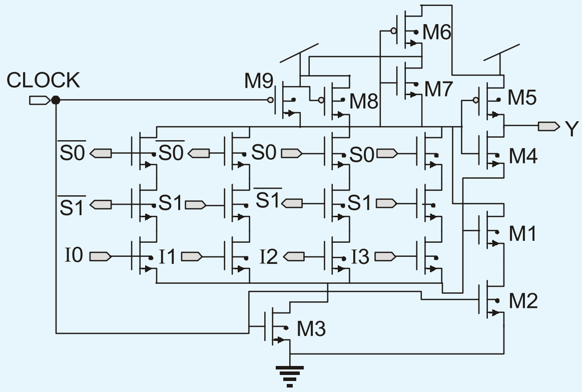
End of Solution

Q.1 (e) Design 4-to-1 multiplexer using domino logic.

[10 marks : 2024]

Solution:

4-to-1 multiplexer using domino logic:



End of Solution

Q.1 (f) A silicon p-i-n photodiode in an optical receiver receives a peak optical power at 1300 nm. The diode has a quantum efficiency of 50% and delivers electrical power to a load of 8 kΩ. If the diode receives a peak power of –30 dBm, calculate the thermal noise and shot noise if the bandwidth of operation is 8 MHz. The dark current value = 5 nA.

[$e = 1.6 \times 10^{-19}$ C, $h = 6.63 \times 10^{-34}$ *J-s*, $c = 3 \times 10^8$ m/s, $k_B = 1.38 \times 10^{-23}$ J/K]

[10 marks : 2024]

Solution:

Given that

$$\lambda = 1300\text{ nm}$$
$$\eta_Q = 50\% = 0.5$$
$$R_L = 8\text{ kW}$$
$$P_{in} = -30\text{ dBm}$$
$$B = 8\text{ MHz}$$
$$I_d = 5\text{ nA}$$
$$P_{in} = -30\text{ dBm}$$

$$-30\text{ dBM} = 10\log\left(\frac{P_{in}}{1 \times 10^{-3}}\right)$$

$$10^{-3} = \frac{P_{in}}{1 \times 10^{-3}}$$

$$P_{in} = 1 \times 10^{-6}\ \text{W}$$
$$T = 20°\text{C} = 290°\text{K (Room temperature considered)}$$

The thermal noise in the load resistor is given

$$i_t^2 = \frac{4kTB}{R_L} = \frac{4 \times 1.38 \times 10^{-23} J/K \times 290K \times 8 \times 10^6}{8 \times 10^3}$$

$$i_t^2 = 1.6008 \times 10^{-17}\ \text{A}^2$$

The total shot noise is

$$i_s^2 = 2eB(I_d + I_o)$$

$$I_o = \frac{\eta_Q P_{in} e}{h \times f} = \frac{\eta_Q P_{in} \times e \times \lambda}{h \times c}$$

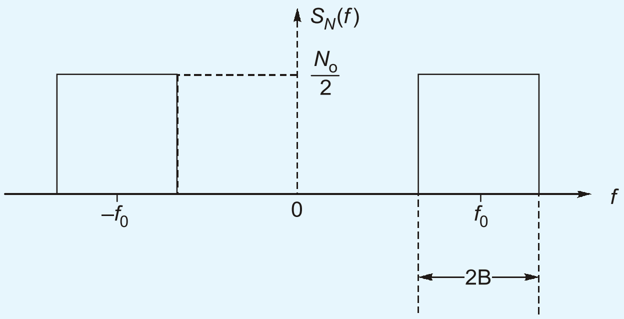
$$= \frac{0.5 \times 1.6 \times 10^{-9} \times 1300 \times 10^{-9} \times 10^{-6}}{6.63 \times 10^{-34} \times 3 \times 10^8}$$

$$= 5.228 \times 10^{-7}\text{A}$$

$$i_s^2 = 2eB(I_d + I_o)$$
$$= 2 \times 1.6 \times 10^{-19} \times 8 \times 10^6 (5 \times 10^{-9} + 5.228 \times 10^{-7})$$
$$i_s^2 = 1.351 \times 10^{-18}\ \text{A}^2$$

End of Solution

Q.2 (a) A zero Gaussian noise $n(t)$ has power spectral density $S_N(f)$ as shown below:



(i) Plot the power spectral density of in-phase and quadrature components of $n(t)$.

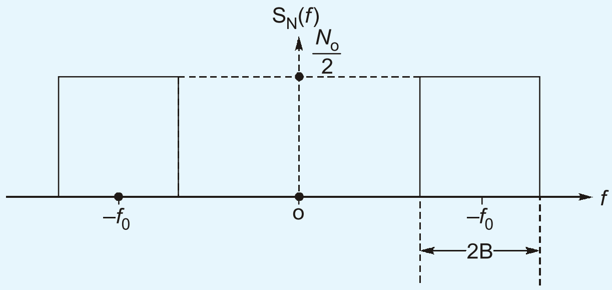
[10 marks : 2024]

(ii) Find the probability density function of the envelope of $n(t)$.

[10 marks : 2024]

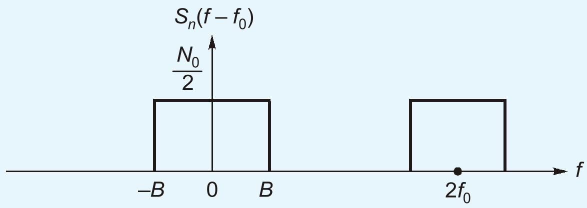
Solution:

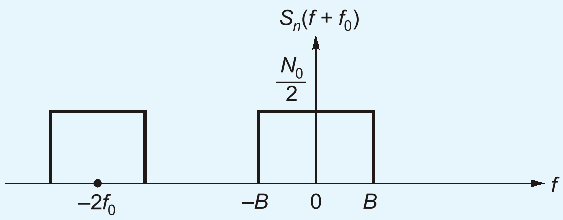
(i) Power spectral density of zero mean Gaussian noise $n(t)$ given below:

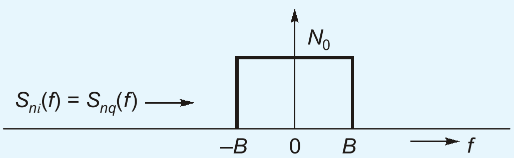


PSD of its inphase and quadrature components will be

$$S_{ni}(f) = S_{nq}(f) = S_n(f - f_0) + S_n(f + f_0); \; -B \le f \le B$$
$$0 \qquad ; \quad \text{otherwise}$$







(ii) Gaussian noise $n(t)$ can be expressed interms of its inphase and quadrature components as

$$n(t) = n_1(t)\cos 2\pi f_c t - n_q(t)\sin 2\pi f_c t$$

The envelope of $n(t)$ is $\quad r(t) = \sqrt{n_I^2(t) + n_q^2(t)}$

Probability density function of

$$r(t) \text{ is } f_R(r) = \begin{cases} \frac{r}{\sigma^2} e^{-r^2/2\sigma^2}; & r \geq 0 \\ 0 & ; \text{otherwise} \end{cases}$$

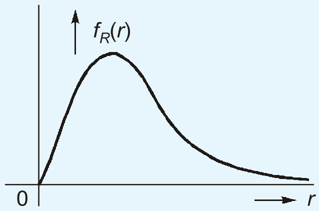
Since mean of $n(t)$ is zero,

Mean of $n_I(t)$ and $n_q(t)$ also zero.

So that $\sigma^2 = MSQ = 2N_0B$

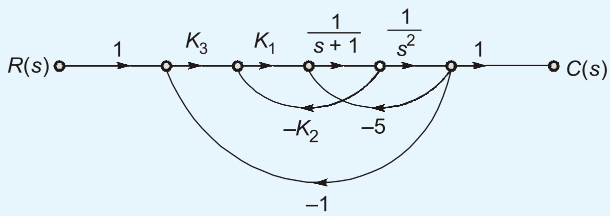
Therefore,
$$f_R(r) = \begin{cases} \frac{r}{2N_0B} e^{\frac{-r^2}{4N_0B}}; & r \geq 0 \\ 0 & ; \text{ otherwise} \end{cases}$$

Probability density function of $r(t)$ is Rayleigh density function.



End of Solution

Q.2 (b) A control system is represented by the signal flow graph shown below.



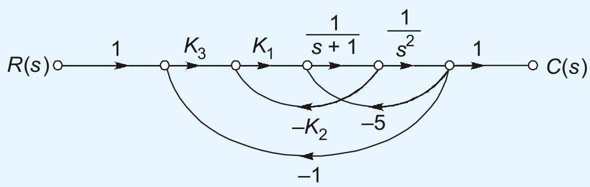
(i) Determine the overall system gain $\frac{C(s)}{R(s)}$, if $K_1 = 1$, $K_2 = 5$ and $K_3 = 5$.

[10 marks : 2024]

(ii) Find the sensitivity of the system to changes in K_1 for $\omega = 0$.

[10 marks : 2024]

Solution:



(i) $\frac{C(s)}{R(s)} = ?$ if $K_1 = 1$, $K_2 = 5$ and $K_3 = 5$

Forward path $\frac{K_3K_1}{s^2(s+1)}$

$$\text{Loops } L_1 = \frac{-K_3K_1}{s^2(s+1)}$$

$$L_2 = \frac{-K_1K_2}{(s+1)}$$

$$L_3 = \frac{-5}{s^2(s+1)}$$

Number of non touching loops = 0

$$\frac{C(s)}{R(s)} = \frac{\frac{K_3K_1}{s^2(s+1)}}{1-\left[\frac{-K_3K_1}{s^2(s+1)} - \frac{K_1K_2}{(s+1)} - \frac{5}{s^2(s+1)}\right]}$$

$$\frac{C(s)}{R(s)} = \frac{\frac{K_3K_1}{s^2(s+1)}}{\frac{s^2(s+1)+K_3K_1+K_1K_2s^2+5\times 1}{s^2(s+1)}}$$

$$\frac{C(s)}{R(s)} = \frac{K_3K_1}{s^2(s+1)+s^2K_1K_2+(5+K_1K_3)}$$

$$\frac{C(s)}{R(s)} = \frac{5\times 1}{s^2(s+1)+s^2\times 5\times 1+(5+1\times 5)}$$

$$\frac{C(s)}{R(s)} = \frac{5}{s^2(s+1)+5s^2+10}$$

$$\frac{C(s)}{R(s)} = \frac{5}{s^3+6s^2+10}$$

(ii) Sensitivity $S_{K_1}^{T}\Big|_{\omega=0} = ?$

$$\frac{C(s)}{R(s)} = \frac{5K_1}{s^2(s+1)+s^2K_1+5+(5+K_1\times 5)}$$

$$\frac{C(s)}{R(s)} = \frac{5K_1}{s^2(s+1)+5K_1s^2+5+5K_1}$$

$$T(s) = \frac{5K_1}{s^3+s^2+5K_1s^2+(5+5K_1)}$$

$$T(s) = \frac{5K_1}{s^3+s^2(1++5K_1)+(5+5K_1)}$$

$$s_{K_1}^T = \frac{\frac{\partial T}{T}}{\frac{\partial K_1}{K_1}} = \frac{\partial T}{T} \times \frac{K_1}{\partial K_1}$$

$$s_{K_1}^T = \frac{\partial T}{\partial K_1} \times \frac{K_1}{T}$$

$$T = \frac{5K_1}{s^3 + s^2(1+5K_1) + 5K_1 + 5}$$

at $s = 0 \quad \Rightarrow$
$$T = \frac{5K_1}{5K_1 + 5}$$

$$s_{K_1}^T = \frac{K_1}{T}\frac{\partial T}{\partial K} = \frac{5}{5K_1 + 5}$$

$\therefore$
$$s_{K_1}^T = \frac{5}{5+5} = \frac{5}{10} = 0.5$$

End of Solution

Q.2 (c) Explain the following terms associated with virtual memory:

(i) Address spaces

[5 marks : 2024]

(ii) Address mapping

[5 marks : 2024]

(iii) Private virtual memory

[5 marks : 2024]

(iv) Shared virtual memory

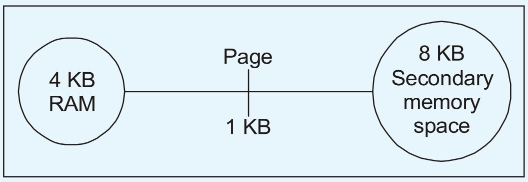
[5 marks : 2024]

Solution:

(i) Address spaces:

- Virtual memory gives the illusion to the programmer that execute the large application programs on a small main memory space.
- This concept states, use the secondary memory space to store the application program when the program site is greater than the main memory space.
- Main memory address space is named as physical address space.
- Secondary memory address space is named as logical address space.

e.g.



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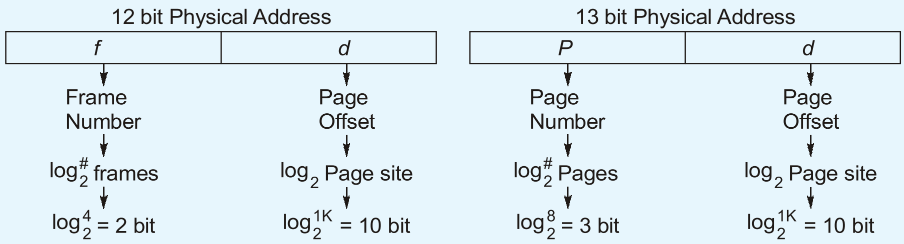
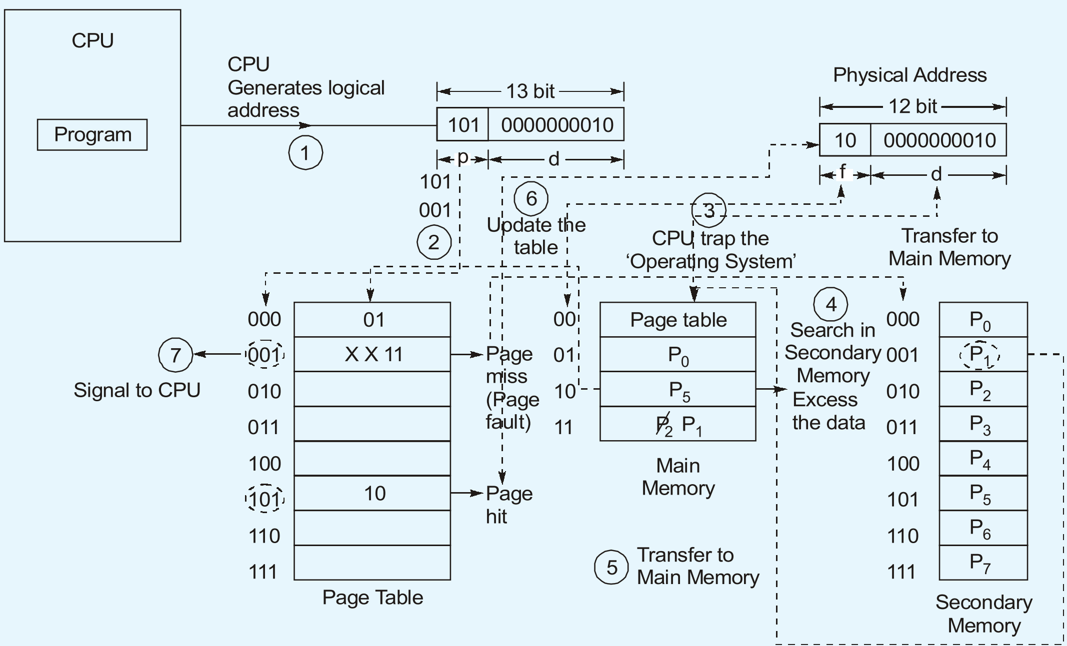
- 4 KB RAM space is named as physical address space.
- 8 KB Secondary space is named as logical (or) virtual address space.
- Frames in main memory = $\frac{4\text{KB}}{1\text{ KB}} = 4$
- Pages in Secondary memory = $\frac{8\text{ KB}}{1\text{ KB}} = 8$



(ii)



1. CPU generates logical address while executing the application program.
2. Logical address will be interpreted into a P, –d format.
   P l d format
3. Based on the P value, the respective entry will be enabled into the page table.
4. When the entry contain frame no. then operation became Page Hit so, physical address will be formed by <w> frame no. from the page table.
5. Physical address will be interpreted into a fld format.
6. Based on the 'f' value, the corresponding frame is enabled in the main memory later access the data from main memory based on 'd' value (page offset).
7. Otherwise, (entry is empty) operation is 'Page Miss'. Page miss is called as 'Page fault'.

8. When page fault occur then (PU trap to 'OS'.
9. 'OS' identify the page in the secondary memory, transfer the page into a main memory by using replacement policies when the main memory is full.
10. Page replacement policies are:
    a. FIFO (First In-first out)
    b. LRU (Least recently used)
    c. Optimal replacement

(iii) **Private virtual memory:** Private memory can not be used by other work processes. After releasing the assigned memory. The operating system still considers the virtual memory as being occupied by the allocating work process.

(iv) **Shared Virtual memory:** Real memory related to physical memory (RAM). Virtual memory is how much fake memory is allocated to the process, means memory that is allocated on the permanent storage medium (Hard drive, SSD etc.) for that process. Shared memory is physical memory that can be shared with other process.

End of Solution

Q.3 (a) An AM signal has a form

$u(t) = [20 + 2\cos 3000\,\pi t + 10\cos 6000\,\pi t)\cos 2\pi f_c t$

where $f_c = 10^5$ Hz.

(i) Sketch the voltage spectrum of $u(t)$.

[4 marks : 2024]

(ii) Determine the power in each of the frequency components.

[4 marks : 2024]

(iii) Determine the modulation index.

[4 marks : 2024]

(iv) Determine the sideband power and total power.

[4 marks : 2024]

(v) Determine the transmission efficiency.

[4 marks : 2024]

Solution:

AM signal given by

$$u(t) = [20 + 2\cos 3000\pi t + 10\cos 6000\pi t]\cos 2\pi f_c t$$

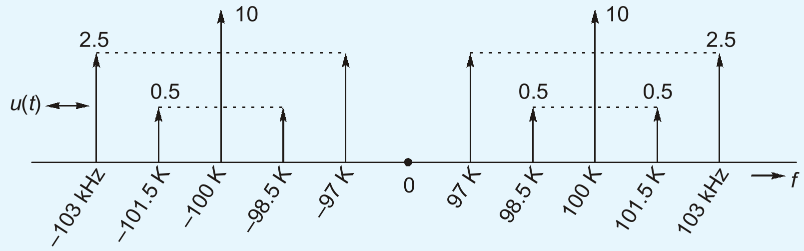
Given

$$f_c = 10^5 \text{ Hz}$$

(i)

$$u(t) = 20\cos 2\pi\times 10^5 t + 2\cos 2\pi\times 10^5 t\cos 2\pi\times 1500t + 10\cos 2\pi\times 10^5 t\cos 2\pi\times 3000t$$

$$= 20\cos 2\pi\times 10^5 t + \cos 2\pi(101.5\times 10^3)t + \cos 2\pi(98.5\times 10^3)t + 5\cos 2\pi(103\times 10^3)t + 5\cos 2\pi(97\times 10^3)t$$



(ii) Power in 100 kHz frequency component,

$$P_{100\text{ kHz}} = \frac{(20)^2}{2} = 200\text{ W}$$

$$P_{101.5\text{ K}} = P_{98.5\text{ kHz}} = \frac{(1)^2}{2} = 0.5\text{ W}$$

$$P_{103\text{ K}} = P_{97\text{ kHz}} = \frac{(5)^2}{2} = 12.5\text{ W}$$

(iii)

$$u(t) = 20[1 + 0.1\cos 3000\pi t + 0.5\cos 600\,\pi t]\cos 2\pi f_c t$$

$$S_{AM}(t) = A_c[1 + \mu_1 \cos 2\pi f_{m1} t + \mu_2 \cos 2\pi f_{m2} t]\cos 2\pi f_c t$$

Total modulation index, $\mu_t = \sqrt{\mu_1^2 + \mu_2^2}$

$$= \sqrt{(0.1)^1 + (0.5)^2} = 0.509$$

(iv) Sideband power, $P_{SB} = \frac{P_c \mu_t^2}{2}$

$$P_c = \frac{A_c^2}{2} = \frac{(20)^2}{2} = 200\text{ W}$$

$$P_{SB} = \frac{200 \times 0.26}{2} = 26\text{ W}$$

Total power, $P_t = P_c\left[1 + \frac{\mu_t^2}{2}\right]$

$$= 200\left[1 + \frac{0.26}{2}\right] = 226\text{ W}$$

(v) Transmission efficiency; $\eta = \frac{\mu_t^2}{2 + \mu_t^2}$

$$= \frac{0.26}{2 + 0.26} = 0.115$$

$$\eta = 11.5\%$$

End of Solution

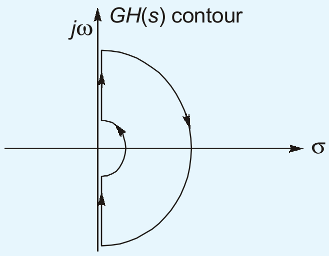
Q.3 (b) Sketch the Nyquist plot and conclude on closed-loop stability of the following open-loop transfer function of unity feedback control system:

$$G(s) = \frac{K}{s\left(s^2+s+4\right)}$$

[20 marks : 2024]

Solution:

$$G(s) = \frac{K}{s(s^2+s+4)}$$



$$G(j\omega) = \frac{K}{(j\omega)\left[\left((j\omega)^2+j\omega+4\right)\right]}$$

$$G(j0^+) = \frac{K}{(j0^+)\left[(j0^+)^2+(j0^+)+4\right]}$$

$$= \angle -90^\circ$$

$$G(j\infty^+) = \frac{K}{(j\infty^+)\left[(j\infty)^2+(j\infty)+4\right]}$$

$$= 0\angle -270^\circ$$

$$G(j\omega) = \frac{K}{(j\omega)\left[-\omega^2+j\omega+4\right]}$$

$$G(j\omega) = \frac{K}{(j\omega)\left[(4-\omega^2)+j\omega\right]}$$

$$G(j\omega) = \frac{K\left[(4-\omega^2)-j\omega\right]}{j\omega\left[(4-\omega^2)+j\omega\right]\left[(4-\omega^2)-j\omega\right]}$$

$$G(j\omega) = \frac{K\left[(4-\omega^2)-j\omega\right]}{j\omega\left[(4-\omega^2)^2+\omega^2\right]}$$

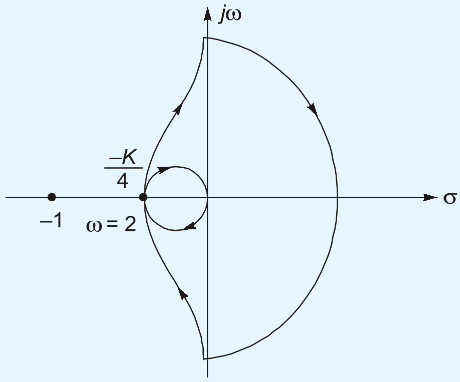
$$G(j\omega) = \frac{-jK\left[(4-\omega^2)-j\omega\right]}{\omega\left[(4-\omega^2)^2+\omega^2\right]}$$

$$G(j\omega) = \frac{-jK(4-\omega^2)-K\omega}{\omega\left[(4-\omega^2)^2+\omega^2\right]}$$

$$G(j\omega) = \frac{-K\omega}{\omega\left[(4-\omega^2)^2+\omega^2\right]} - \frac{jK(4-\omega^2)}{\omega\left[(4-\omega^2)^2+\omega^2\right]}$$

$\omega = 0^+$	–ve	–ve	IIIrd quad
$\omega = \infty^+$	–ve	+ve	IInd quad

For $img = 0$ $\qquad \omega = 2$ rad/sec



for $-\frac{\pi}{2}$ to $\frac{\pi}{2}$ $\underset{R\to 0}{lt}\, Re^{j\theta}$

$$G(j\omega) = \underset{R\to 0}{lt}\frac{K}{(Re^{j\theta})\left[(Re^{j\theta})^2+(Re^{j\theta})+4\right]}$$

$$G(j\omega) = \infty e^{-j\theta}$$

$$\theta = \frac{-\pi}{2} \text{ to } \frac{\pi}{2} \quad \text{(ACW)}$$

$$-\theta = \frac{\pi}{2} \text{ to } \frac{-\pi}{2} \quad \text{(CW)}$$

$\underset{R\to\infty}{lt}\, Re^{j\theta}$

$$G(j\omega) = \underset{R\to\infty}{lt}\frac{K}{(Re^{j\theta})\left[(Re^{j\theta})^2+(Re^{j\theta})+4\right]}$$

$$= 0\angle -270^\circ$$

Stable: $N = P = 0$

$\therefore \qquad \frac{-K}{4} > -1 \Rightarrow 0 < K < 4$

Marginally stable: N is undefined

$\therefore \qquad \frac{-K}{4} = -1 \Rightarrow K = 4$

Unstable : $N \neq P$

$\therefore \qquad \frac{-K}{4} < -1 \Rightarrow 4 < K < \infty$

End of Solution

Q.3 (c) (i) Define and differentiate between the following types of databases:

(1) Relational databases

(2) Object-oriented databases

(3) NoSQL databases

Discuss the key characteristics of each database type, highlighting their strength and weaknesses.

[10 marks : 2024]

(ii) Over the years, several protocol standards for I/O have emerged, with USB becoming most popular. Give at least five reasons to justify this statement. With the help of a block schematic, explain the working of a DMA controller.

[10 marks : 2024]

Solution:

(i) RDBMS:

A relational database is a type of database that organizes data into one or more tables, each consisting of rows and columns. In a relational database, data is structured for efficient storage, retrieval, and manipulation of information.

The tables in a relational database are related based on common fields or keys. For example, in a database for a store, the customer table might have a common field with the order table, linking each order to the customer who placed it.

Relational databases use a SQL to access and manipulate data. SQL allows users to insert, update, delete, and retrieve data from the database.

Features of RDBMS

1. SQL DB is table based DB.
2. Data store in rows and columns.
3. Each row contain a unique instance of data for the categories defined by the columns.
4. Provide facility primary key to uniquely identity the rows.

Limitations of RDBMS

1. Scalability
2. Complexity

OO DBMS:

Object-oriented is another type of database available among the various types of databases. An object-oriented database (OODB) is a type of database management system (DBMS). It stores data in the form of objects rather than in tables like relational databases. In an OODB, each object is an instance of a class, which defines the attributes and behaviours of that object.

The use of objects allows for more complex data structures and relationships that can be easily modelled in a relational database. For example, an object in an OODB can have attributes that are themselves objects, allowing for creating more complex data structures.

In addition, OODBs can support complex relationships between objects, such as inheritance and polymorphism. It allows for more flexible and extensible data models.

Advantages

1. Complex data sets can be saved and retrieved quickly and easily.
2. Object IDs are assigned automatically.
3. Works well with object-oriented programming languages.

Limitations

1. Object databases are not widely adopted.
2. In some situations, the high complexity can cause performance problems.

NoSQL Database:

NoSQL database, also known as a "non- relational" database, is a type of database that stores and retrieves data in a way that is different from traditional relational databases. Unlike relational databases, NoSQL databases are not based on tables with strict schemes and relationships between them. Instead, NoSQL databases use various data models, such as document-oriented, key-value, graph- based, or column-oriented, to store and manage data.

Features of NoSQL DB

1. NoSQL commonly referred to as NOT only SQL with NoSQL.
2. Less data can be stored in multiple collections and nodes.
3. It doesn't require fixed table schemes.
4. It supports limited join queries and we scale it horizontally.

Benefits of NoSQL

1. Highly and easily scalable.
2. Maintaining NoSQL servers is less expensive.
3. Lesser server cost and open source.
4. No schema (or) filed model.
5. Support integrated caching.

Limitation of NoSQL

1. NoSQL data base is open source.
2. No stored procedures in MongoDB (NoSQL data base).
3. GUI mode tools to access the data base is not flexibly available in market.
4. Too difficult to finding NoSQL experts.

(ii) USB : The USB (Universal Serial Bus) port became popular for several reasons:

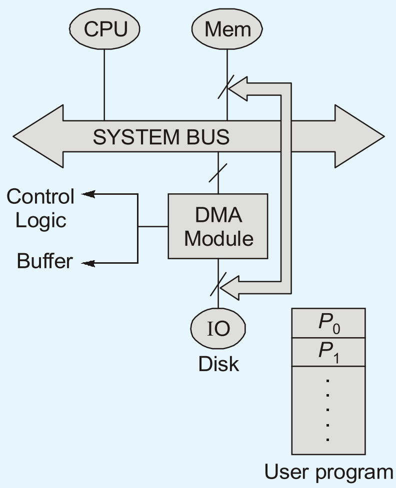
1. **Versatility:** USB ports are versatile and can be used for a wide range of devices, including keyboards, mice, printers, external hard drives, cameras, smartphones, and more. This versatility made them a convenient choice for connecting various peripherals to a computer.
2. **Ease of Use:** USB ports are "hot- swappable," meaning devices can be connected and disconnected without needing to restart the computer. This ease of use made USB ports more convenient than older connection types like serial or parallel ports.

3. **Faster Data Transfer:** USB ports provided faster data transfer speeds compared to older connection types. As technology advanced and the need for faster data transfer rates grew, USB ports became more attractive.
4. **Standardization:** USB became a standardized connection type across various devices and manufacturers. This standardization made it easier for consumers to use USB devices across different computers and platforms.
5. **Power Supply:** USB ports can also provide power to connected devices, eliminating the need for separate power adapters for many peripherals. This feature added to the convenience and appeal of USB ports.
6. **Compact Size:** USB ports are relatively small and can be integrated into various devices without taking up much space. This compact size made them suitable for laptops, tablets, and other portable devices.
7. **Backward Compatibility:** USB ports are backward compatible, meaning newer USB devices can be used with older USB ports, albeit at lower speeds. This backward compatibility ensured that older devices could still be used with newer computers.

Overall, the combination of versatility, ease of use, speed, standardization, power supply capabilities, compact size, and backward compatibility contributed to the widespread adoption and popularity of USB ports in the computing industry.

DMA: In this mode, bulk amount of data will be transferred from 10 to main M/M w/o involvement of CPU.

- To implement virtual m/m concept. DMA is used because it involves transfer of bulk data.
- When the user program size is greater than the main M/M capacity than virtual M/M concept is used to increase the address space. This concept state that use the secondary M/M to store the user program.
- Secondary M/M is a kind of 10 device, interfaced to system bus via DMA module, therefore, during the execution of a program, there is a need of transferring the bulk amount of data from 10 to main M/M via DMA w/o involvement of CPU.



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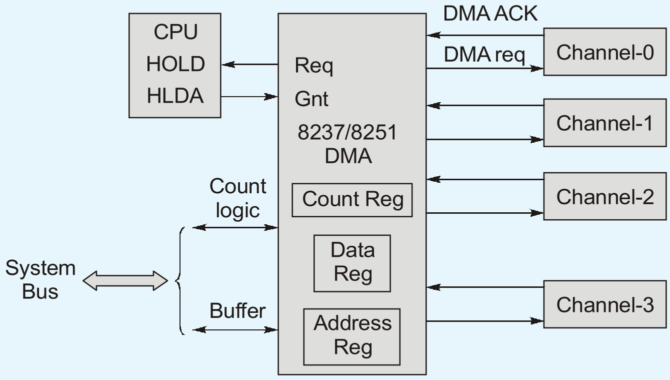
- CPU initializes the DMA module to transmit the data with control signal. Add register with M/M address where data is to be copied and count register to specify number of bits to be transferred and port number to activate the port.
- When device is ready with the data, it will send DMA REQ to DMA.
- When DMA receives DMA REQ, the CPU send signal to Hold (during previous time, CPU was busy). CPU grants the system bus to IO and get blocked and then DMA ACK sent to port and device start transmitting via data register through bus directly. After completion of data transfer, CPU again get the control over bus when count = 0.



Accessing sequence:

1. CPU initializes the 10 interface (DMA Module) along with 10 command, later, busy with other useful task.
2. 10 command contains the information about port address, M/M address, control signals and count value.
3. DMA control logic enables the IO port for the operation. 10 port consume the time to prepare the data later enables the DMA REQ signal.
4. After receiving this signals, DMA module enables hold signal to CPU and waiting for HLDA signal.
5. After receiving the HLDA signal, DMA module enables the DMA ACK signal . When the 10 device receiving this signal than, it starts transmission of data to main M/M via DMA until count becomes zero.
6. After the DMA operation bus connection will be restablished into CPU. (by the DMA)

Note: In the DMA operation, CPU is in two states:

1. Busy state (until 10 device prepares the data)
2. Blocked state (Hold state) until transfer the data to main M/M)

Let X is preparation time, Y is the transfer time.

$$\% \text{ time CPU busy} = \frac{X}{X+Y} * 100$$

$$\% \text{ time CPU blocked} = \frac{Y}{X+Y} * 100$$

End of Solution

Q.4 (a) (i) Analog voice frequency signal band-limited to 4 kHz is sampled at 1.25 times the Nyquist rate. The samples are quantized and encoded using N-bit PCM. Find the minimum N to have an average signal to quantization noise of at least 40 dB. What is the minimum storage capacity needed to accommodate the digitized signal if the total duration of the voice frequency signal is 10 seconds? Also find the information rate of the source if all the quantization levels are equally likely and statistically independent.

[10 marks : 2024]

(ii) Obtain and draw the PSK signal constellations for the value of $M = 2$, 4 and 8, if all have same transmitted signal energy E_s. Determine the minimum distance between the adjacent signal points. For $M = 8$, determine by how many dB the transmitted signal energy E_s must be increased to achieve the same d_{min} as $M = 4$.

[10 marks : 2024]

Solution:

(i) Given that

$$f_m = 4 \text{ kHz}$$

$$f_s = 1.25 \text{ NR}$$

$$= 1.25[2f_m] = 2.5 f_m$$

$$= 10 \text{ kHz}$$

$$\text{SQNR} \geq 40 \text{ dB}$$

$$1.76 + 6.02 N \geq 40$$

$$N \geq 6.35$$

$$N_{\text{min}} = 7$$

$$\text{Bit rate, } R_b = Nf_s$$

$$= 7 \times 10\text{k}$$

$$= 70 \text{ kbps}$$

$$= 70{,}000 \text{ bits/sec}$$

Storage capacity required to accommodate the digitized signal for a duration of 10 sec is 70000 × 10

$$= 700 \times 10^3 \text{ bits}$$

$$\text{Information Rate, } R = H \times f_s$$

Number of quantization levels,

$$L = 2^N = 128$$

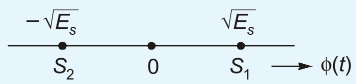
Given that all quantization levels are equally likely

$$H = \log_2 128 = 7 \frac{\text{bits}}{\text{sample}}$$

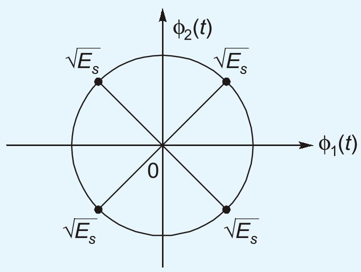
$$R = 7 \times 10$$

$$= 70 \text{ kbps}$$

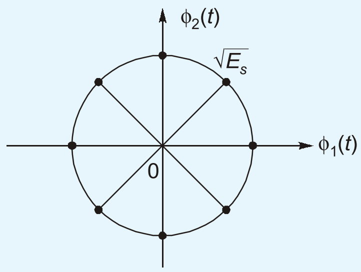
(ii) Constellation diagram for 2-ary PSK



4-ary PSK:



8-ary PSK:



d_{min} for M-ary PSK, $d_{min} = 2\sqrt{E_s}\sin\frac{\pi}{M}$

For $M = 2 \rightarrow$ $\quad d_{min} = 2\sqrt{E_s}\sin\frac{\pi}{2} = 2\sqrt{E_s}$

$M = 4 \rightarrow$ $\quad d_{min} = 2\sqrt{E_s}\sin\frac{\pi}{4} = \sqrt{2E_s}$

$M = 8 \rightarrow$ $\quad d_{min} = 2\sqrt{E_s}\sin\frac{\pi}{8} = 0.38\sqrt{E_s}$

Given that $\quad (d_{min})_{M=8} = (d_{min})_{M=4}$

$$2\sqrt{E_{s1}}\sin\frac{\pi}{8} = 2\sqrt{E_{s2}}\sin\frac{\pi}{4}$$

$$\frac{E_{s1}}{E_{s2}} = \left(\frac{\sin\frac{\pi}{4}}{\sin\frac{\pi}{8}}\right)^2$$

$$\frac{E_{s1}}{E_{s2}} = 3.414$$

$$10\log E_{s1} - 10\log E_{s2} = 10\log 3.414$$

$$(E_{s1})_{dB} - (E_{s2})_{dB} = 5.33 \text{ dB}$$

$$(E_{s1})_{dB} = (E_{s2})_{dB} + 5.33 \text{ dB}$$

To get same d_{min} as $M = 4$, 5.33 dB of additional transmitted energy should be added for $M = 8$.

End of Solution

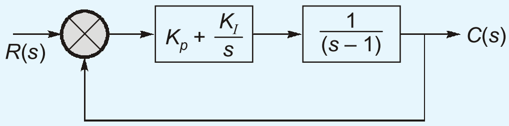
Q.4 (b) Design a proportional plus integral (PI) controller so that the system having transfer function

$$G(s)H(s) = \frac{1}{s-1}$$

will have closed-loop poles at $s = -0.5$ and -1.

[20 marks : 2024]

Solution:



$$\text{Transfer function, T.F} = \frac{\left(K_p + \frac{K_I}{s}\right)\left(\frac{1}{s-1}\right)}{1+\left(K_p + \frac{K_I}{s}\right)\left(\frac{1}{s-1}\right)}$$

$$\text{T.F} = \frac{\frac{K_p}{s-1} + \frac{K_I}{s(s-1)}}{1+\frac{K_p}{s-1} + \frac{K_I}{s(s-1)}}$$

$$\text{T.F} = \frac{sK_p + K_I}{s(s-1) + sK_p + K_I} = \frac{sK_p + K_I}{s^2 + s(K_p - 1) + K_I}$$

Now for given poles, characteristics equation is given as

$$(s + 0.5)(s + 1) = 0$$

$$s^2 + s + 0.5s + 0.5 = 0$$

$$s^2 + s(1.5) + 0.5 = 0$$

On comparing, we get

$$K_p - 1 = 1.5; \quad K_I = 0.5$$

$$K_p = 2.5$$

End of Solution

Q.4 (c) (i) Explain the following terms associated with computer security:

Breach fo confidentiality, breach of integrity, breach of availability, theft of service and denial of service.

[10 marks : 2024]

(ii) If an instruction set architecture is to prevail, it must be designed to survive rapid changes in computer technology. An architect must plan for technology changes that can increase the lifetime of successful computer.

With respect to this, discuss and analyze the following trends:

(1) Implementation technologies.

(2) Performance trends, bandwidth and latency

(3) Power and energy in integrated circuits

[10 marks : 2024]

Solution:

(i)
- A data breach can be categorized into 3 parts. These are confidentiality, availability and integrity.
- In the confidentiality breach technique the unauthorized (or) accidental access and personal information has happened.
- In the availability breach technique, the destruction of data has happened and because of that the loss of access to personal information takes place.
- In the integrity breach technique, the unauthorised (or) accidental alteration of personal information has happened.

Denial-of-Service (DoS)

- A denial of service is a form of cyber attack that prevents legitimate users from accessing a computer (or) Network.
- In a Denial-of-service attack, rapid and continuous online requests are sent to a target server to overload the server's bandwidth.
- Distributed denial-of-service attacks leverage a wide web of computers (or) devices infected with malware to launch a co-ordinated barrage of meaningless online requests, blocking legitimate access.

Theft-of-Service

- Theft of services is when someone uses a service without paying for it.
- This violation involves the unauthorized use of resources.
- There are various methods to commit theft of service without even recognizing it, this is a prevalent offense among those with no lengthy criminal backgrounds.

  Eg: Unauthorized use of resources such as,

  1. Theft of CPU cycles
  2. Installation of daemons running an unauthorized file server.
  3. Tapping into the target's telephone (or) networking services.

(ii) Compared to the first generation of the computers modern-day computers are faster, smarter, stronger, cheaper and can store a huge amount of data.

Due to vast development and huge improvement of the modern computer, the work of mankind has been made much easier than ever before with the development of high speed and advanced.

Computer Generations	Timeline	Hardware
First generation computer	1940-1956	Vacuum tubes
Second generation computer	1956-1963	Transistor
Third generation computer	1964-1971	Integrated circuit
Fourth generation computer	1971-1989	Microprocessor
Fifth generation computer	1980-till now	Artificial Intelligence

Technologies over time:

Year	Technology used in computers	Relative performance/Unit cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit	900
1995	Very large scale integrated circuit	2,400,000
2013	Ultra large scale integrated circuit	250,000,000,000

Transistors → on/off switch controlled by electric signal.

Integrated circuit → Many transistors in a single chip.

VLSI/ULSI → Containing thousands/millions/billions of transistors.

Computer performances:

- Computer performance is the amount of useful work accomplished by a computer system.
- Computer performance is estimated in terms of accuracy, efficiency and speed of executing computer program instructions.
- One (or) more of the following factors might be involved in the high performance of a computer i.e.
  1. Short response time for a given piece of work.
  2. High through put (rate of processing work).
  3. Low utilization of computer resources.
  4. High availability of the computing system (or) application.
  5. High bandwidth.
  6. Short data transmission time.

Computer performance matrices are:

- Availability
- Response time
- Channel capacity

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- Latency
- Completion time
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- Relative efficiency
- Scalability
- Performance per watt
- Compression ratio
- Instruction path length
- Speed up
- Performance of a CPU $\propto \frac{1}{\text{Execution time}}$
- Execution time = $\Sigma(IC_i \times CPI_i)$ Cycle time
- Speed up $(s) = \frac{\text{Performance X}}{\text{Performance Y}} = \frac{ET_y}{ET_x} = n$

  Sys 'X' runs 'n' times faster than Sys 'y' iff n > 1.

For implementation of an instruction set, architects must be aware of important trends in both the technology and the use of computers, as such trends affect not only the future cost but also the longevity of an architecture.

1. **Implementation Technologies:** An architect must plan for technology changes that can increase the lifetime of a successful computer. The designer must be aware of rapid changes in implementation technology. Five implementation technologies, which change at a dramatic pace, are critical to modern implementations:

(a) **Integrated circuit logic technology:** Transistor density increases by about 35% per year, quadrupling somewhat over four years. Increases in die size are less predictable and slower, ranging from 10% to 20% per year. The combined effect is growth rate in transistor count on a chip of about 40% to 55% per year, or doubling every 18 to 24 months, also popularly known as Moore's law.

(b) **Semiconductor DRAM (dynamic random-access memory):** Now that most DRAM chips are primarily shipped in DIMM modules, it is harder to track chip capacity, as DRAM manufacturers typically offer several capacity products at the same time to match DIMM capacity. Capacity per DRAM chip has increased by about 25% to 40% per year recently, doubling roughly every two to three years. There is even concern as whether the growth rate will stop in the middle of this decade due to the increasing difficulty of efficiently manufacturing even smaller DRAM cells.

(c) **Semiconductor Flash (electrically erasable programmable read-only memory):** This nonvolatile semiconductor memory is the standard storage device in PMDs, and its rapidly increasing popularity has fueled its rapid growth rate in capacity.

Capacity per Flash chip has increased by about 50% to 60% per year recently, doubling roughly every two years. In 2011, Flash memory is 15 to 20 times cheaper per bit than DRAM.

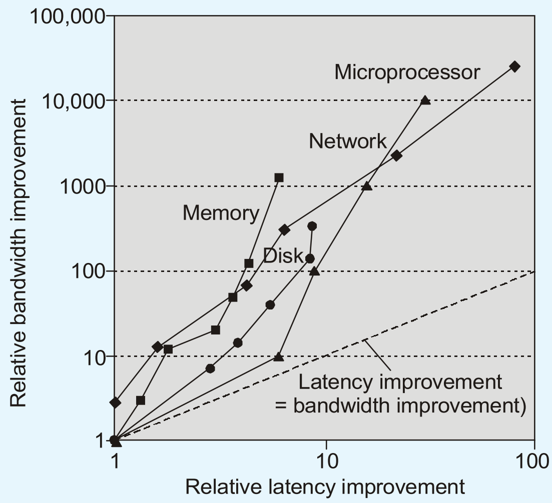
(d) **Magnetic disk technology:** Prior to 1990, density increased by about 30% per year, doubling in three years. It rose to 60% per year thereafter, and increased to 100% per year in 1996. Since 2004, it has dropped back to about 40% per year, or doubled every three years. Disks are 15 to 25 times cheaper per bit than Flash. Given the slowed growth rate of DRAM, disks are now 300 to 500 times cheaper per bit than DRAM. This technology is central to server and warehouse scale storage.

(e) **Network technology:** Network performance depends both on the performance of switches and on the performance of the transmission system.

These rapidly changing technologies shape the design of a computer that, with speed and technology enhancements, may have a lifetime of three to five years. Key technologies such as DRAM, Flash, and disk change sufficiently that the designer must plan for these changes. Indeed, designers often design for the next technology, knowing that when a product begins shipping in volume that the next technology may be the most cost-effective or may have performance advantages. Traditionally, cost has decreased at about the rate at which density increases.

2. **Performance Trends: Bandwidth over Latency:**

Bandwidth or throughput is the total amount of work done in a given time, such as megabytes per second for a disk transfer. In contrast, latency or response time is the time between the start and the completion of an event, such as milliseconds for a disk access. The below figure shows the relative improvement in bandwidth and latency for technology milestones for microprocessors, memory, networks, and disks.



Clearly, bandwidth has outpaced latency across these technologies and will likely continue to do so. A simple rule of thumb is that bandwidth grows by at least the square of the improvement in latency. Computer designers should plan accordingly.

3. Power and Energy in Integrated Circuits:

For CMOS chips, the traditional primary energy consumption has been in switching transistors, also called dynamic energy. The energy required per transistor is proportional to the product of the capacitive load driven by the transistor and the square of the voltage:

$$\text{Energy dynamic} \propto 1/2 \text{ Capacitive load} \times \text{Voltage}^2$$

The power required per transistor is just the product of the energy of a transition multiplied by the frequency of transitions:

$\text{Power}_{\text{dynamic}} \propto 1/2 \times \text{Capacitive load voltage}^2 \times \text{Frequency switched}$

For a fixed task, slowing clock rate reduces power, but not energy. Clearly, dynamic power and energy are greatly reduced by lowering the voltage, so voltages have dropped from 5 V to just under 1 V in 20 years. The capacitive load is a function of the number of transistors connected to an output and the technology, which determines the capacitance of the wires and the transistors.

As we move from one process to the next, the increase in the number of transistors switching and the frequency with which they switch dominate the decrease in load capacitance and voltage, leading to an overall growth in power consumption and energy. The first microprocessors consumed less than a watt and the first 32-bit microprocessors (like the Intel 80386) used about 2 watts, while a 3.3 GHz Intel Core i7 consumes 130 watts. Given that this heat must be dissipated from a chip that is about 1.5 cm on a side, we have reached the limit of what can be cooled by air. Given the equation above, the clock frequency growth is expected to slow down if we can't reduce voltage or increase power per chip.

End of Solution

Section-B

Q.5 (a) A parabolic index profile graded index fiber has a core diameter of 62.5 μm, numerical aperture of 0.275. Determine its normalized frequency at a wavelength of 850 nm and calculate the number of guided modes that can propagate through this optical fiber.

[10 marks : 2024]

Solution:

Given that: For parabolic profile, $\alpha = 2$;

$$2a = 6.25\ \mu\text{m}$$
$$NA = 0.275$$
$$\lambda = 850\ \text{nm}$$
$$V = ?$$
$$M_n = ?$$

Normalized frequency, $V = \frac{2\pi a}{\lambda} NA$

$$V = \frac{\pi \times 62.5 \times 10^{-6} \times 0.275}{850 \times 10^{-9}} = 63.524$$

$$\text{Number of modes, } M_n = \frac{V^2}{4} \quad [\text{for parabolic profile } \alpha = 2]$$

$$= \frac{(63.524)^2}{4} = 1008.85$$

$$= 1008 \text{ [Complete number of modes]}$$

End of Solution

Q.5 (b) The characteristic equation of a closed-loop control system is given by

$$s^6 + s^5 + 3s^4 + 3s^3 + 3s^2 + 2s + 1 = 0$$

Determine the number of right-half s-plane roots, left-half s-plane roots and roots on the imaginary axis.

[10 marks : 2024]

Solution:

$$q(s) = s^6 + s^5 + 3s^4 + 3s^3 + 3s^2 + 2s + 1 = 0$$

$\lim_{x \to 0}$

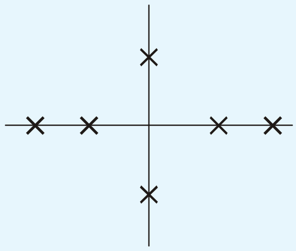
s^6	1	3	3	1
s^5	1	3	2	
s^4	$\phi = x$	1	1	
s^3	$\frac{3x-1}{x}$	$\frac{2x-1}{x}$		
s^2	$\frac{4x-1-2x^2}{3x-1}$	1		
s^1	$\frac{4x^3+x^2}{-2x^3+4x^2-x}$			
s^0	1			

Upon substituting $\lim_{x \to 0}$

s^6	1	3	3	1
s^5	1	3	2	
s^4	0	1	1	
s^3	$-\infty$	$-\infty$		
s^2	1	1		
s^1	2			
s^0	1			

$$A(s) = s^2 + 1$$

$$\frac{d}{ds}A(s) = 2s^1$$



Number of poles in left side of $j\omega$ axis, $L = 2$
Number of poles in right side of $j\omega$ axis, $R = 2$
Number of poles on imaginary axis = 2

End of Solution

Q.5 (c) (i) Calculate the number of memory chips needed to design 8K-byte memory if the memory chip size is 1024 × 1.

[5 marks : 2024]

(ii) The memory address of the last location of an 8K-byte memory chip is FFFF in hexadecimal system. Find the starting address.

[5 marks : 2024]

Solution:

(i) Number of 1024 × 1 memory chips needed to design 8 K bytes memory

$$\Rightarrow \frac{\text{Memory to be designed}}{\text{Available capacity}}$$

$$\Rightarrow \frac{8\text{ kB}}{1024 \times 1} \Rightarrow \frac{8(1024 \times 8)}{1024 \times 1} = 8 \times 8 = 64 \text{ chips}$$

Since, 1 kB $\Rightarrow$ $\boxed{1024 \times 8}$

(ii) Last address location of an 8 kB memory chip is given as $(\text{FFFF})_H$.

$$8\text{K} = 8 \times 1024 = (8192)_{10} = (2000)_H$$

Final address – Starting address + 1 = Capacity of memory

$$(\text{FFFF})_H - x + 1 = (2000)_H$$

$$\therefore \quad x = (\text{FFFF})_H - (2000)_H + 1 = (\text{E000})_H$$

$$\therefore \quad \text{Starting address} = (\text{E000})_H$$

End of Solution

Q.5 (d) A dipole antenna of length 0.02λ has a linear current distribution with peak current I_0 occurring at the center of the dipole. Determine I_0 required to provide a radiation field amplitude of 100 microvolts per meter at a distance of 500 m at $\theta = \frac{\pi}{2}$. What will be the total average power radiated at this current?

[10 marks : 2024]

Solution:

Given data: $dl = 0.02\lambda$; $E = 0.02\lambda$; $E = 100$ µV/m ; $r = 500$ m ; $\theta = \pi/2$

(a) Here, $dl = \frac{\lambda}{50}$, and current is linear

Hence, it is a short dipole

$$\therefore \quad E = \frac{\eta I_o l \beta \sin\theta}{8\pi r} = \frac{120\pi \times I_o \times 0.02\lambda \times \frac{2\pi}{\lambda} \times \sin 90^\circ}{8\pi \times 500}$$

$$E = 0.00377 I_o$$

$$\Rightarrow \quad I_o = \frac{100 \times 10^{-6}}{0.00377} = 0.0265\text{ A} = 26.5\text{ mA}$$

(b) P_{rad}:

$$P_{rad} = I_o^2 \times 10\pi^2 \left[\frac{dl}{\lambda}\right]^2$$

$$\Rightarrow \quad P_{rad} = (0.0265)^2 \times 10 \times \pi^2 \times (0.02)^2$$

$$\Rightarrow \quad P_{rad} = 27.8\ \mu\text{W}$$

End of Solution

Q.5 (e) An analog filter is characterized as

$$H(s) = \frac{4}{(s+2)^2}$$

Design the corresponding IIR filter if the sampling frequency is 10 Hz, using impulse invariance method.

[10 marks : 2024]

Solution:

The transfer function of analog filter as given as

$$H(s) = \frac{4}{(s+2)^2}$$

By applying the inverse Laplace transform,

$$h(t) = 4t \cdot e^{-2t} u(t)$$

Now, let us perform sampling at $t = nT_s = \frac{n}{f_s}$

$$h(n) = h(t)\Big|_{t=\frac{n}{f_s}} = 4\left(\frac{n}{f_s}\right) - e^{-2\left(\frac{n}{f_s}\right)} u(n)$$

$$= 4\left(\frac{n}{10}\right) \cdot e^{-2\left(\frac{n}{10}\right)} \cdot u(n) \qquad (\because f_s = 50\text{ Hz})$$

$$= 0.4n \cdot e^{-0.2n} \cdot u(n) = 0.4n(e^{-0.2})^n \cdot u(n)$$

By applying $2T$ on $h(n)$, we will obtain the transfer function of the desired IIR filter,

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$$H(z) = \frac{0.4e^{-0.2} \cdot z^{-1}}{(1-e^{0.2} \cdot z^{-1})^2}$$

$$\Rightarrow \quad H(z) = \frac{0.327 \cdot z^{-1}}{(1-0.818z^{-1})^2}$$

Note:

$$te^{-2t} \cdot u(t) \xrightleftharpoons{LT} \frac{1}{(s+2)^2}$$

$$n(e^{-0.2})^n \cdot u(n) \xrightleftharpoons{ZT} \frac{e^{-0.2} \cdot z^{-1}}{(1-e^{-0.2} \cdot z^{-1})^2}$$

End of Solution

Q.5 (f) (i) What is the purpose of using directional couplers in microwave communication systems? With the help of a schematic diagram, explain the working of a two-hole waveguide directional coupler.

[6 marks : 2024]

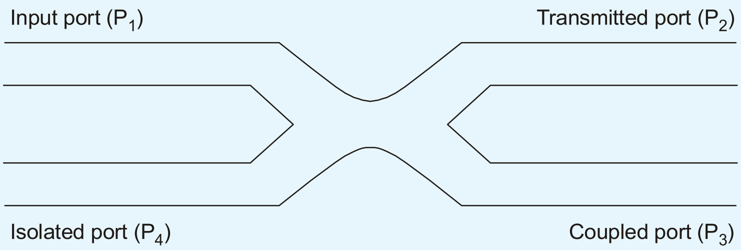
(ii) For a pyramidal horn antenna, define gain and beamwidth. If the operating frequency is 10 GHz and a horn antenna has a height of 10 cm and a width of 12 cm, calculate the beamwidth and gain, taking the value of k = 0.5.

[4 marks : 2024]

Solution:

(i) The purpose of using directional couplers in microwave communication systems are:

1. **Signal monitoring and power measurement:** Directional couplers allow for extracting a small sample of the signal power from the main line without significantly affecting the original signal.
   This enables monitoring signal strength and characteristics at various points in the microwave circuit.
2. **Isolation:** Directional couplers can provide isolation between different parts of a microwave system.
   A large portion of the signal travelling in one direction is prevented from passing through to the other direction and prevents unwanted leakages.
3. **Balanced mixer design:** Directional couplers used in mixers to convert a signal from one frequency to other.
4. **Beam forming in Antenna Arrays:** Directional couplers can be used to control the amplitude and phase distribution of the signals feeding individual antenna elements and shapes the radiation pattern.



This coupler type has four parts and symmetric design allowing forward and reverse signals to be sampled simultaneously.

Coupler factor: This indicates the fraction of the input power at P_1 that is delivered to the coupled part P_3.

$$\text{Coupling, } C = 10\log_{10}(P_1/P_3)$$

Directivity: This is a measure of the coupler's ability to separate waves propagating in forward and reverse directions as observed at the coupled (P_3) and isolated (P_4) parts.

$$\text{Directivity, } D = 10\log(P_3/P_4)$$

Isolation: It indicates the power delivered to the uncoupled load (P_4).

$$\text{Isolation } I = 10\log(P_1/P_4)$$

Insertion loss : It is the ratio for the input power (Pi) delivered to the transmitted (P_2) port.

$$\text{Insertion loss, } L = 10\log(P_1/P_2)$$

(ii) **Gain of pyramidal horn antenna:** The gain of a pyramidal horn antenna is defined as the ratio of the radiated power intensity along its beam axis to the intensity of an isotropic antenna with the same mathematically;

$$\boxed{G = n_{ap}\cdot\frac{4\pi}{\lambda^2}A}$$

$n_{ap} \rightarrow$ Aperture efficiency
$A \rightarrow$ Area of aperture

Beamwidth of pyramidal non antenna: A beamwidth is the angular span of the main lobe of the radiation per horn, which is the region of the pattern where most of the power is radiated. The beamwidth is measured at the angle between two points on either sides of main lobe also known as –3 dB point or half power point, where the power radiated drops to half of its maximum value.

Numerical:

Given data: $f = 10$ GHz ; $h = 10$ cm ; $W = 12$ cm ; $K = 0.5$

1. Beamwidth

(a) Vertical beamwidth, $\theta_E = \dfrac{56\lambda}{h} = \dfrac{56\cdot C}{hf} = \dfrac{56\times3\times10^8}{10\times10^{-2}\times10\times10^9} = 16.8°$

(a) Horizontal beamwidth, $\theta_H = \dfrac{67\lambda}{W} = \dfrac{67C}{hf} = \dfrac{67\times3\times10^8}{12\times10^{-2}\times10\times10^9} = 16.75°$

2. Gain, $G = 0.5\times\dfrac{4\pi}{(0.03)^2}\cdot(120\times10^{-4}) = 83.77 = 19.23\text{ dB}$

End of Solution

Q.6 (a) 60 MHz uniform plane wave is propagating in a lossless medium with ε_r = 9 and μ_r = 4.

(i) Determine the phase constant β, wavelength λ and phase velocity v_p for the wave.

[6 marks : 2024]

(ii) This wave is normally incident onto another medium having conductivity σ = 4 S/m, ε_r = 80 and μ_r=1. The second medium is assumed to be good conductor at 60 MHz. Determine the fractions of the incident power that are reflected and transmitted.

[14 marks : 2024]

Solution:

Given data: $f = 60$ MHz ; $\in_r = 9$; $\mu_r = 4$

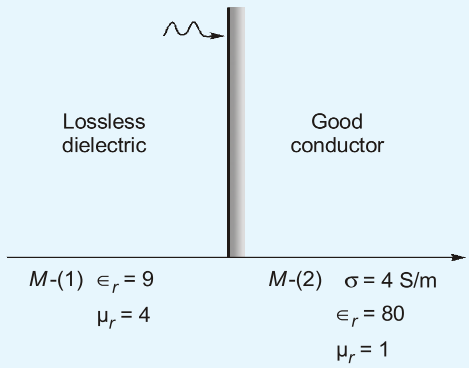
(i) β, λ, v_p ;

$$\beta = \frac{\omega}{c}\sqrt{\mu_r \in_r} \qquad \beta = \frac{2\pi}{\lambda} \qquad v_p = \frac{\omega}{\beta}$$

$$\Rightarrow \beta = \frac{2\pi \times 60 \times 10^6}{3 \times 10^8} \times 6 \qquad \Rightarrow \lambda = \frac{2\pi}{\beta} = \frac{2\pi}{7.54} \qquad \Rightarrow v_p = \frac{2\pi \times 60 \times 10^6}{7.54}$$

$$\Rightarrow \beta = 7.54 \text{ rad/m} \qquad \Rightarrow \lambda = 0.833 \text{ m} \qquad \Rightarrow v_p = 5 \times 10^7 \text{ m/s}$$

(ii)



$$\eta_1 = 120\pi\sqrt{\frac{\mu_r}{\in_r}} = 120\pi\sqrt{\frac{4}{9}} = 80\pi$$

$$\eta_2 = \sqrt{\frac{\omega\mu}{\sigma}}\angle 45^\circ = \sqrt{\frac{2\pi \times 60 \times 10^6 \times 4\pi \times 10^{-7}}{4}}\angle 45^\circ$$

$$\eta_2 = 10.88\angle 45^\circ$$

$$\therefore \quad \Gamma = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1} = \frac{10.88\angle 45^\circ - 251.32\angle 0^\circ}{10.88\angle 45^\circ + 251.32\angle 0^\circ} = 0.94\angle 176.5^\circ$$

$$\Rightarrow \quad \tau = 1 + \Gamma = 1 + 0.94\angle 176.5^\circ = 0.84\angle 42.90^\circ$$

Now,
$$\frac{P_{ref}}{P_{inc}} = -|\Gamma|^2 = -(0.94)^2 = -0.8836$$

$$\frac{P_{trans}}{P_{inc}} = \tau^2\left[\frac{\eta_1}{\eta_2}\right] = (0.084)^2\left[\frac{80\pi}{10.88}\right] = 0.163$$

End of Solution

Q.6 (b) Write an 8085 A program to exchange the higher and lower nibble of ten 8-bit numbers stored from location 2200H. Make use of subroutine and explain parameter passing using pointer and stack techniques.

[20 marks : 2024]

Solution:

Given data of 10 bytes from 2200 H. Required program → To exchange higher and lower nibbles of these 10 bytes.

Algorithm:

1. Initialize memory pointer using 'HL' pair to 2200 H and 'SP' to F004 H (considered).
2. Load a count of 10 into register B.
3. Call a subroutine to exchange lower and higher nibbles of byte using rotate left instruction.
4. Repeat the same operation till the 10 bytes are completed.

∗ When 'CALL' instruction is executed

Step1: Next instruction address or 'PC' value is pushed onto stack.

Step2: Program control is transferred to the subroutine address.

After 'CALL', i.e. final value

But before this → $[[SP-1]] \leftarrow [PC_H]$

$[SP-2] \leftarrow [PC_L]$

$\therefore$ $SP \leftarrow [SP]-2$;

∗ When 'RET' instruction is executed in the subroutine.

Step1: The value @ top of stake i.e. 2B are accessed into PC.

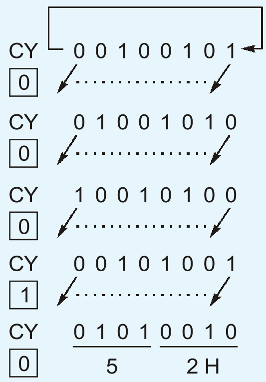
Step2: The program control is transferred to the 16-bit address i.e. in 'PC'.

$\therefore$ $SP \leftarrow [SP]+2$

```
        LXI SP, F004 H   ;   Initialize stack pointer
        LXI H, 2200 H    ;   Initialize memory pointer @ 2200H
        MVI B, 0A H      ;   Count of 10 into register-B
NEXT:   CALL EXNG        ;   CALL subroutine EXNG
        INX H            ;   Increment memory pointer
        DCR B            ;   Decrement count in 'B'
        JNZ NEXT         ;   If Z = 0 ? then go to NEXT else Halt
        HLT              ;   Stop
        ; Subroutine for exchanging nibbles.
```

EXNG:	MVI C, 04 H	;	Load count of 4 into Register-C
	MOV A, M	;	Move data byte into 'ACC' from memory
Rpt:	RLC	;	Rotate 'ACC' left for 1-bit without carry, to exchange lower and higher nibble
	DCR C	;	Check count in Register-C by [C] – 1
	MOV M, A	;	
	JNZ Rpt	;	If Z = 0 ? then 'Rpt' else 'RET'
	RET	;	Return to main program

Example: If data byte @ 2200 H is 25 H i.e. $(00100101)_2$, then after rotating 4-times to left, it would be $(\underbrace{0101}_{5}\,\underbrace{0010}_{2H})_2$



End of Solution

Q.6 (c) (i) Receiving antenna and input RF amplifier are the most crucial areas of a ground receiver in a satellite communication system. Write a typical block diagram considering the receive-only TV (ROTV) converter and indicate the various aspects with typical numerical values of frequencies.

[10 marks : 2024]

(ii) Highlight the importance of power budget and rise-time budget in the design of optical communication systems. What are the three factors that limit the transmission distance, when the link lengths are long or data transmission rates are high?

Show how maximum link length is determined for RZ coding and NRZ coding, considering material dispersion.

[10 marks : 2024]

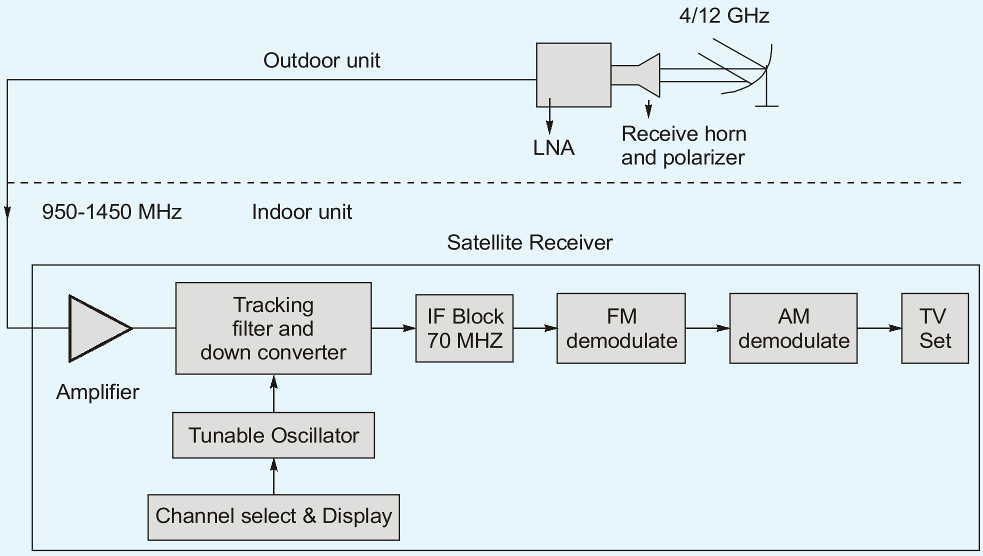
Solution:

(i) The Receive-only Home TV systems in satellite communication consists of two units :

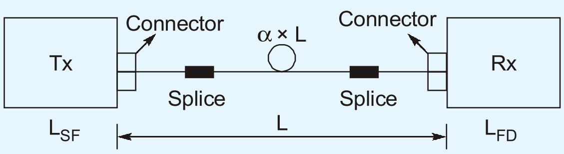
1. Indoor unit 2. Outdoor unit

1. **Indoor Unit :** The single mesh type reflector may be used which focuses the signals into a dual feed-horn, which has two separate outputs, one for the c-band signals and one for the KU-band signals.

2. Outdoor unit:
   (a) This consists of a receiving antenna feeding directly into a low noise amplifier combination.
   (b) The receiver antenna is a parabolic reflector with downlink frequency band of 12.2 to 12.7 GHz have range of 500 MHz which accommodates 32 TV/FM channels each of which is 24 MHz wide.
   (c) The signal fed to the indoor unit is normally a wide band signal covering the range 950 to 1450 MHz. This is amplified and passed to a tracking filter which selects the desired channel.
   (d) The selected channel is again down converted from 950 to 1450 MHz range to a fixed intermediate frequency of 70 MHz although VHF range are also used.
   (e) The IF carrier must be demodulated and the baseband information used to generate a VSB signal which is fed into one of the TV set.



(ii) Power budget :



1. The optical power budget in a fiber optic communication link is the allocation of available optical power among various loss producing mechanisms such as coupling loss, fibre loss, splice losses and connector loss to ensure that adequate signal strength at the receiver.
2. The power received is a function of
   (a) Power from light source P_t
   (b) Source to fibre loss L_{SF}.
   (c) Fibre loss depends on length $(\alpha \times L)$
   (d) Connector/ splice losses L_{Ca}
   (d) Fibre to detector loss L_{Fd}.

3. A system margin is incorporated into the optical power budget to allow for component ageing, temperature fluctuations and losses arising from components that may be added in future.

$$P_r = P_t - [L_{SF} + L_{splica} + L_{connector} + \alpha L + L_{coupler} + L_{FD}]$$

Rise time budget :

1. A rise time budget analysis is a convenient method for determining the dispersion limitation at an optical link.
2. The purpose of rise time budget is to ensure that the system operates properly at intended bit rate.
3. The total transition time degradation t_{sys} of a digital link should not exceed 70 percent of an NRZ bit period or 35 percent for RZ data.

$$t_{sys} = \sqrt{t_{r_{Tx}}^2 + t_{r_{Lx}}^2 + t_{r_{Fiber}}^2 + t_{r_{PD}}^2 + t_{r_{Rx}}^2}$$

$$= \frac{0.35}{BW}$$

The three factors that limit the transmission distance, when the link lengths are long or data rates are high are

1. Optical power 2. Loss and dispersion 3. Receiver sensitivity

Modulation formats: There are two major modulation formats in digital OFC are 1) NRZ (Non return to zero) 2) RZ (Return zero).

The RZ signal format displays performance advantages over that NRZ like higher peak power, greater noise immunity and better BER performance.

For an RZ pulse format, the bit rate R_b = B = 1/T (T = pulse duration).

$$T_{sys} = t_r = 0.35\ T$$

$$= \frac{0.35}{B} = \frac{0.35}{R_b}$$

$$R_b = \frac{0.35}{T_{sys}}$$

For an NRZ pulse format, the Bit rate

$$R_b = \frac{B}{2} = \frac{1}{2T}$$

The maximum Bit rate, $R_b = \dfrac{0.7}{T_{sys}}$

End of Solution

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Q.7 (a) A lossless transmission line of length 0.8λ and characteristic impedance $Z_0 = 75\ \Omega$ operating at 60 MHz has velocity on the line 3×10^8 m/s.

(i) If the line is short circuited at the load end, find the input impedance Z_{in}. At what distance closest to the short-circuited end is the impedance seen zero?

[10 marks : 2024]

(ii) If the short circuit is replaced by a load $Z_L = 60 - j40\ \Omega$, determine the input impedance Z_{in}, reflection coefficient Γ and standing wave ratio (SWR). Determine the power delivered to the load if a source of 10 volts r.m.s. with series impedance $Z_g = 75\ \Omega$ is connected at the input.

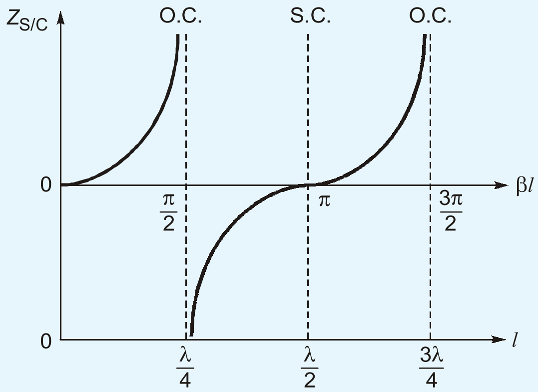
[10 marks : 2024]

Solution:

Given data: $l = 0.8\lambda$; $Z_o = 75\ \Omega$; $f = 60 \times 10^6$ Hz ; $v = 3 \times 10^8$ m/s

(i) $$Z_{S/C} = jZ_o \tan \beta l = j75\tan\left(\frac{2\pi}{\lambda} \times 0.8\lambda\right) = j7.5\tan(1.6\pi) = -j230.826\ \Omega$$

From the graph, impedance will become zero, at $\frac{\lambda}{2}$ distance.



$$\therefore \quad l = \frac{\lambda}{2} = \frac{v}{2f} = \frac{3 \times 10^8}{2 \times 60 \times 10^6} = 2.5\text{ m}$$

Alternatively:

For $Z_{S/C} = 0$

$$jZ_o \tan\beta l = 0$$

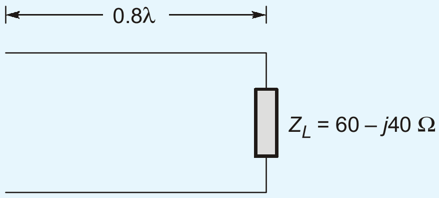
$$\Rightarrow \quad \tan\beta l = 0$$

$$\Rightarrow \quad \beta l = n\pi$$

$$\Rightarrow \quad l = \frac{n\pi}{\beta} = \frac{n\pi}{2\pi} \cdot \lambda = \frac{n\lambda}{2}$$

For $n = 1$, $l = \frac{\lambda}{2} = 2.5$ m

(ii) For Z_{in}, Γ, S



$$\beta l = \frac{2\pi}{\lambda} \times 0.8\lambda = 1.6\pi$$

$\Rightarrow$ $$\tan\beta l = \tan(1.6\pi) = -3.078$$

$\therefore$ $$Z_{in} = Z_o\left[\frac{Z_L + jZ_o \tan\beta l}{Z_0 + jZ_L \tan\beta l}\right]$$

$\Rightarrow$ $$Z_{in} = 75\left[\frac{60 - j40 - j230.826}{75 + j(60 - j40)(-3.078)}\right]$$

$\Rightarrow$ $$Z_{in} = 75\left[\frac{60 - j270.826}{-48.12 - j184.68}\right]$$

$\Rightarrow$ $$Z_{in} = 75 \times 1.453\angle 27.09^\circ$$

$\Rightarrow$ $$Z_{in} = 108.975\angle 27.09^\circ\ \Omega$$

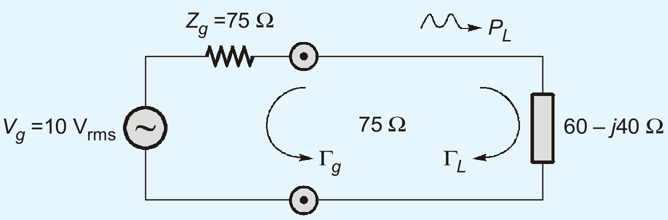
Γ:
$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{60 - j40 - 75}{60 - j40 + 75} = \frac{-15 - j40}{135 - j40} = 0.303\angle -94.05^\circ$$

$\therefore$ $$\Gamma = 0.303\angle -94.05^\circ$$

S:
$$S = \frac{1 + |\Gamma|}{1 - |\Gamma|} = \frac{1 + 0.303}{1 - 0.303} = 1.87$$

$\therefore$ $$S = 1.87$$

Power delivered to the load:



$$P_L = \left[1 - |\Gamma|^2\right] P_{inc}$$

$$P_{inc} = \frac{|V_0^+|^2}{2Z_o}$$

Here, $$V_0^+ = \frac{Z_o V_g}{Z_o + Z_g} \frac{e^{-j\beta l}}{1 - \Gamma_L \Gamma_g e^{-j2\beta l}}$$

$$\Rightarrow \quad V_0^+ = \frac{75\times 10\sqrt{2}}{75+75} e^{-j\frac{2\pi}{\lambda}\times 0.8\lambda}$$

$$\Rightarrow \quad V_0^+ = 7.07\, e^{-j1.6\pi}$$

$$\Rightarrow \quad V_0^+ = 7.07\angle -288^\circ = 7.07\,\angle 72^\circ$$

Hence, $$P_L = \frac{(7.07)^2}{2\times 75}\left[1-(0.303)^2\right]$$

$$\Rightarrow \quad P_L = 0.3026\text{ W}$$

End of Solution

Q.7 (b) What is essential hazard? Find the hazard-free realization circuit for the following function :

$$f(a, b, c, d) = \Sigma m(1, 5,7, 14, 15)$$

[10 marks : 2024]

Solution:

Essential hazard will occur in asynchronous sequential circuits is named as essential hazard. This type of hazard is causal by unequal delays along two or more paths that originate from an equivalent input.

An excessive delay through an inverter circuit as compared to the delay related to the feedback path may cause such a hazard.

Essential hazards can't be corrected by adding redundant gates as in static hazards.

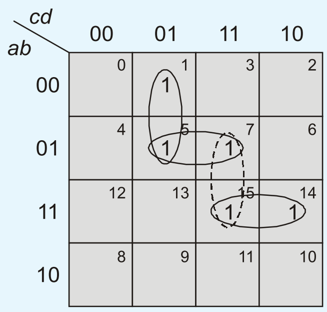
The problem that they impose is often corrected by adjusting the quantity of delay within the affected path.

To avoid essential hazards, each feedback circuit must be handled with individual care to make sure that the delay within the feedback path is long enough compared with delays of other signals that originate from the input terminals.

The hazard-free realization circuit for the following function:

$$f(a, b, c, d) = \Sigma m(1, 5, 7, 14, 15)$$

Using K-map



The hazard-free realization is,

$$f = \bar{a}bd + abc + bcd + \bar{a}\bar{c}d$$

End of Solution

Q.7 (c) (i) Suppose that a 1 MHz channel can support a 1 Mbps transmission rate. The channel is to be shared by 10 stations. Each station receives frames with an exponential inter arrival rate of $\lambda = 500$ frames/s and frames are of constant length L = *1000* bits. Compare the total frame delay of a system that uses FDMA to a system that uses TDMA.

Compare IS-54 and GSM in terms of their ability to handle speech and the effect on spectrum efficiency.

[20 marks : 2024]

(ii) What are the salient features of 802.11 wireless LAN standard? Write the architecture and protocol stack of 802.11 and highlight the major issues. Comment on the physical layer aspects of 802.11.

[10 marks : 2024]

Solution:

(i) Given that

$$Bw = 1 \text{ MHz}$$
$$R_b = 1 \text{ MbPs}$$
$$\text{Number of stations} = 10$$
$$\text{Frame rate, } \lambda = 500 \text{ frames/sec}$$
$$\text{Frame length, } L = 1000 \text{ bts}$$
$$\text{Total frame delay} = ?$$

FDMA: The total frame delay in FDMA is determining by the transmission time, propagation delay and queueing delay.

$$\text{Transmission time} = \frac{\text{Frame length}}{\text{Transmission rate}} = \frac{L}{R_b}$$
$$= \frac{1000}{1 \times 10^6} = 10^{-3} = 1 \text{ ms}$$
$$\text{Transmission time} = 1 \text{ ms}$$
$$\text{Propagation delay} = 0$$
$$\text{queing delay} = 0$$

Total frame delay in FDMA is 1 ms.

TDMA: In TDMA, each station is allocated a specific time slot to transmit its data. Since there are 10 stations, each station gets $1/10^{th}$ of the total available time.

$$\text{Transmission time} = \frac{\text{Frame length}}{\text{Transmission rate}} = \frac{L}{R_b} = \frac{1000}{1 \times 10^6} = 1 \text{ ms}$$
$$\text{Transmission time} = 1 \text{ ms}$$
$$\text{Propagation delay} = 0$$

queing delay=9 ms [Each station will have to wait for its allocated time slot which introduces an additional delay of 9 ms before it can transit its data for the other 9 stations.

Total frame delay in TDMA is 1 ms + 9 ms = 10 ms

FDMA has a lower total frame delay compared to TDMA.

IS-54 offers good efficiency with its 3-user TDMA and $\pi/4$ DQPSK/modulation QPSK. It was the first US digital cellular standard.

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GSM has a lower efficiency than IS-54 due to its 8-user TDMA and GMSK modulation. However, its global compatibility and wide spread adoption make it a significant standard. GSM provides higher a bit rate 22.8 kbps to a full-rate speech channel than IS-54 which only provides 16.2 kbps.

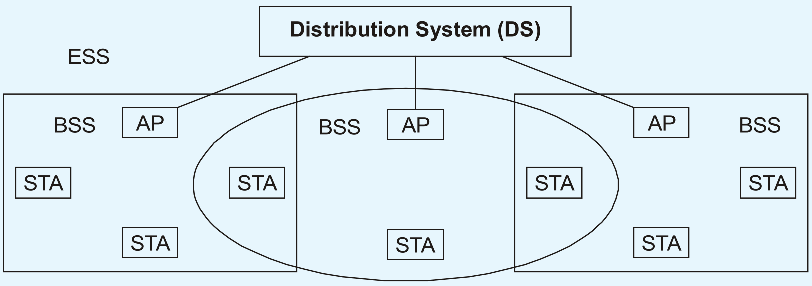
(ii) **IEEE 802.11:** Salient features are

1. IEEE 802.11 defines wireless local area networks (WiFi)
2. It uses CSMA/CA for media access and includes encryption.
3. Wireless networks can operate in ad-hoc mode with no base station or in infrastructure mode with an access point.
4. Infrastructure networks can connect multiple basic service sets to extend the network.

IEEE 802.11 Architecture:

The components of an IEEE 802.11 architecture are as follows:-

1. **Stations (STA):** Stations comprises of all devices and equipment that are connected to the wireless LAN.
   A station can be of two types:
   (a) Wireless access point (WAP) are generally wireless routers that form the base stations or access.
   (b) **Clients:** Clients are work stations, computers, laptop, smart phones etc.
2. **Basic service set (BSS):** A basic service set is a group of stations communicating at the physical layer level. BSS can be of two categories depending upon the mode of operation
   (a) **Infrastructure BSS:** Here the devices communicate with other devices through access points.
   (b) **Independent BSS:** Here the devices communicate in a peer-to-peer basis in an adhoc manner.
   (c) **Extended Service Set (ESS):** It is a set of all connected BSS.
   (d) **Distribution System (DS):** It connects access points in ESS.



End of Solution

Q.8 (a) An air-filled rectangular waveguide has dimensions a = 2.4 cm and b = 1.2 cm.

(i) Over what range of frequencies will this guide operate single mode?

[8 marks : 2024]

(ii) This air-filled waveguide is joined end-to-end with another waveguide of identical dimension. The second waveguide is filled with a lossless dielectric of relative permittivity ε_r. Find the maximum allowable value of ε_r such that single-mode operation can be simultaneously ensured in both waveguides. What will be the range of frequencies for single-mode operation if ε_r is chosen to be equal to half of the maximum allowable value?

[12 marks : 2024]

Solution:

Given data: $a = 2.4$ cm ; $b = 1.2$ cm

(i) Single mode of operation:

Assume, dominant mode of operation i.e. TE_{10}.

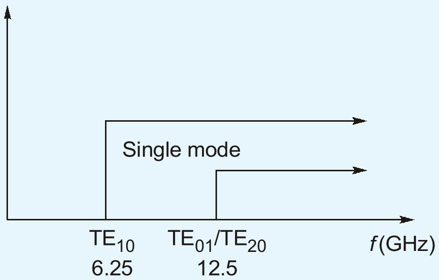
Here, $a > b$, $a = 2b$,

So, order of cut-off frequency,

$$f_C|_{TE_{10}} < f_C|_{TE_{01}} = f_C|_{TE_{20}}$$

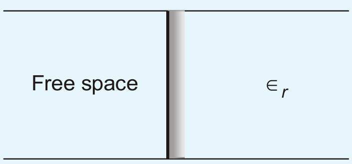
$$f_C|_{TE_{10}} = \frac{c}{2a} = \frac{3\times10^{10}}{2\times2.4} = 6.25 \text{ GHz}$$

$$f_C|_{TE_{01}} = \frac{c}{2b} = \frac{3\times10^{10}}{2\times1.2} = 12.5 \text{ GHz}$$



For single mode of operation, frequency range is 6.25 GHz < 12.5 GHz.

(ii) For $f_c = 6.25$ GHz



$$f_c = \frac{c}{2a\sqrt{\epsilon_r}}$$

$$\Rightarrow \quad \sqrt{\epsilon_r} = \frac{c}{2af_c} = \frac{3\times10^{10}}{2\times2.4\times6.25\times10^{9}} = 1$$

$$\therefore \quad \epsilon_r = 1$$

For $\in_r = 0.5$,
$$\frac{c}{2a\sqrt{\in_r}} < f_o < \frac{c}{2b\sqrt{\in_r}}$$
$$\Rightarrow \quad \frac{3\times10^{10}}{2\times2.4\times\sqrt{0.5}} < f_o < \frac{3\times10^{10}}{2\times1.2\times\sqrt{0.5}}$$
$$\Rightarrow \quad 8.84 \text{ GHz} < f_o < 17.7 \text{ GHz}$$

End of Solution

Q.8 (b) (i) In CMOS logic circuit, assume that V_{DD} = 1.8 V, load capacitance C_L = 0.1 pF, $L_n = L_p = 2\lambda$, $W_n = 18\lambda$ and $W_p = 42\lambda$. Using 0.18 μm parameters, $K'_n = 96\,\mu A/V^2$, $K'_p = 48\,\mu A/V^2$ and $V_{T_{on}} = |V_{T_{op}}| = 0.4$ V, find the propagation delays t_{PHL} and t_{PLH}.

[14 marks : 2024]

(ii) Find the z-transform of the following composite signal and determine the region of convergence :

$$x(n) = \left(\frac{1}{2}\right)^n u(n) + 4\left(\frac{-1}{3}\right)^{2n} u(n)$$

[6 marks : 2024]

Solution:

(i) We have,

$$V_{DD} = 1.8 \text{ V}$$
$$C_L = 0.1 \text{ pF}$$
$$L_n = L_p = 2\lambda$$
$$W_p = 42\lambda$$
$$W_n = 18\lambda$$
$$K'_n = 96\,\mu A/V^2$$
$$K'_p = 48\,\mu A/V^2$$
$$V_{Tn} = |V_{TP}| = 0.4 \text{ V}$$

The effective transconductance parameters K_n and K_p are given by

$$K_n = K'_n\frac{W_n}{L_n}$$
$$K_p = K'_p\frac{W_p}{L_p}$$

Substituting the values:

$$K_n = 96\frac{\mu A}{V^2}\times\frac{18\lambda}{2\lambda} = 864\,\mu A/V^2$$
$$K_p = 48\frac{\mu A}{V^2}\times\frac{42\lambda}{2\lambda} = 1008\,\mu A/V^2$$

The propagation delays are given by

$$t_{PHL} = \frac{0.69 C_L V_{DD}}{I_P}$$

$$t_{PLH} = \frac{0.69 \times C_L \times V_{DD}}{I_n}$$

Where, I_p and I_n are the peak currents for PMOS and NMOS during switching respectively. They are approximated as

$$I_n \simeq \frac{K_n}{2}(V_{DD} - V_{Tn})^2$$

$$I_p \simeq \frac{K_p}{2}(V_{DD} - |V_{TP}|)^2$$

Substituting the value:

$$I_n \simeq \frac{864}{2} \mu A/V^2 \, (1.8 - 0.4)^2$$

$$I_n \simeq 432 \, \mu A/V^2 \, (1.4)^2$$

$$I_n \simeq 846.72 \, \mu A$$

$$I_p \simeq \frac{1008}{2}(1.8 - 0.4)^2$$

$$I_p \simeq 504 \times 1.96$$

$$I_p \simeq 987.84 \, \mu A$$

Now, using these currents to find the delays:

$$t_{PHL} = \frac{0.69 \times 0.1 \times 1.8 \times 10^{-12}}{987.84 \, \mu A}$$

$$t_{PHL} \simeq \frac{0.1242}{987.84} \times 10^{-12}$$

$$t_{PHL} \simeq 0.1258 \text{ psec}$$

$$t_{PLH} = \frac{0.69 \times 0.1 \, pF \times 1.8}{846.72 \, \mu A}$$

$$t_{PLH} \simeq \frac{0.1242 \, pV - s}{846.72 \, \mu A}$$

$$t_{PLH} \simeq 0.1467 \text{ psec}$$

High to low propagation delay (t_{PHL}) is 0.1258 psec.

Low to high propagation delay (t_{PLH}) is 0.1467 psec.

(ii) Given signal is,

$$x(n) = \left(\frac{1}{2}\right)^n \cdot u(n) + 4\left(-\frac{1}{3}\right)^{2n} \cdot u(n)$$

$$= \left(\frac{1}{2}\right)^n \cdot u(n) + 4\left[\left(-\frac{1}{3}\right)^2\right]^n \cdot u(n)$$

$$= \left(\frac{1}{2}\right)^n \cdot u(n) + 4\left(\frac{1}{9}\right)^n \cdot u(n)$$

By appling Z-transform,

$$X(z) = \frac{1}{1-\frac{1}{2}z^{-1}} + \frac{4}{1-\frac{1}{9}z^{-1}}$$

Note: $a^n u(n) \overset{Z}{\rightleftharpoons} \frac{1}{1-az^{-1}}; \quad |z|>|a|$

For existence of ZT,

$$\sum_{n=-\infty}^{\infty} \left| x(n) \cdot r^{-n} \right| < \infty$$

$$\Rightarrow \quad \sum_{n=0}^{\infty}\left[\left(\frac{1}{2}\right)^n \cdot r^{-n} + 4\left(\frac{1}{9}\right)^n \cdot r^{-n}\right] < \infty$$

$$\Rightarrow \quad \sum_{n=0}^{\infty}\left[\left(\frac{1}{2r}\right)^n + 4\left(\frac{1}{9r}\right)^n\right] < \infty$$

$$\Rightarrow \quad \sum_{n=0}^{\infty}\left(\frac{1}{2r}\right)^n + 4\sum_{n=0}^{\infty}\left(\frac{1}{9r}\right)^n < \infty$$

To satisfy the above condition,

$$\frac{1}{2r} < 1 \quad \text{and} \quad \frac{1}{9r} < 1$$

$$\Rightarrow \quad r > \frac{1}{2} \quad \text{...(i)} \quad \text{and} \quad r > \frac{1}{9} \quad \text{...(ii)}$$

From equations (i) and (ii),

$$r > \frac{1}{2}$$

i.e. $$|Z| > \frac{1}{2}$$

So, the region of convergence for the given signal $x(n)$ is,

$$|Z| > \frac{1}{2}$$

End of Solution

Q.8 (c) (i) The main ingredients of a good routing algorithm depend on the objective function that one is trying to optimize. In this background, list and explain the goals that a routing algorithm should seek in general.

How are routing algorithms classified? Distinguish between link state routing and distance vector routing.

[10 marks : 2024]

(ii) What are application protocols with respect to TCP? Show schematically how file transfer occurs using FTP.

What are the three default specifications which must be supported in every FTP implementation?

[10 marks : 2024]

Solution:

(i) **Routing:** Routing is the process of forwarding of a packet in a network so that it reaches its destination.

The main goals of routing are:

1. **Correctness:** The routing should be done properly and correctly so that packets may reach their proper destination.
2. **Simplicity :** The routing should be done in a simple manner so that the overhead is as low as possible.
3. **Robustness:** The algorithms designed for routing should be robust enough to handle-hardware and software failures.
4. **Stability:** The routing algorithms should be stable under all possible circumstances.
5. **Fairness:** Every mode connected to the network should get a fair chance of transmitting their packets.
6. **Optimality:** The routing algorithms should be optimal interms of throughput and minimizing mean packet delays.

Classification of routing algorithms:

1. **Adaptive routing algorithm:** These algorithms change their routing decisions to reflect changes in the topology and in traffic as well. The optimization parameters are the distance, number of hops and estimated transit time.
   This can be further classified as follows:
   (i) Centralized (ii) Isolated (iii) Distributed
2. **Non-Adaptive Routing algorithm:** These algorithms do not base their routing decisions on measurements and estimates of the current traffic and topology.
   This can be classified as follows:
   (a) Flooding (sequence numbers, Hop count, spanning tree)
   (b) Random walk
3. **Delta routing:** It is a hybrid of the centralized and isolated routing algorithms.
4. **Multipath routing:** Instead of single best path, sometimes in order to improve the performance multiple paths between single pair of nodes are used.
5. **Hiearchical routing:** In this method of routing the nodes are divided into regions based on hierarchy.

Differences between link state and distance vector routing.

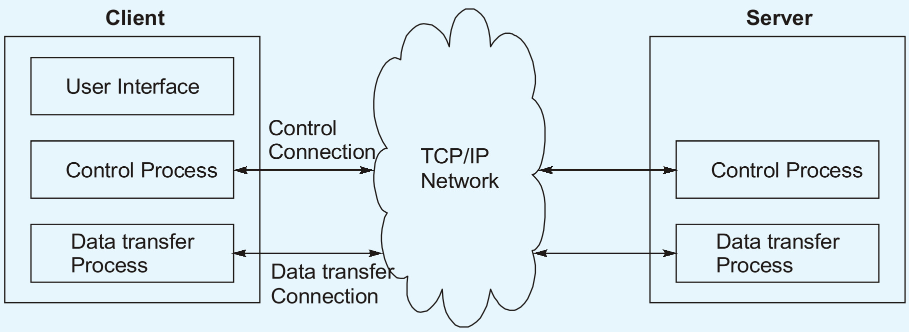
	Link State		Distance vector
1.	It is a dynamic routing algorithm which each router shares knowledge of its neighbours with every other router in the network.	(i)	It is a dynamic routing algorithm in which each router computes a distance between itself and each possible destination i.e. its immediate neighbours.

2. A router sends its information about its neighbors only to all the routers through flooding.	(ii) The router shares its knowledge about the whole network to its neighbours and accordingly updates the table based on its neighbours.
3. Information sharing takes place only whenever there is a change	(iii) The sharing of information with the neighbors takes place at regular intervals.
4. It makes use of DiJkstra's algorithm	(iv) It makes use of Bellman-ford algorithm
5. Heavy traffic due to flooding of packets.	(v) Count to infinity problem and loop will be there forever.

(ii) The protocols used in application layer for TCP are:

1. BOOTP (BOOT Strap Protocol)
2. DHCP (Dynamic Host Configuration Protocol)
3. DNS (Domain Name server)
4. FTP (File Transfer Protocol)
5. TELNET (Terminal Network)
6. SMTP (Simple Mail transfer Protocol)
7. SNMP (Simple Network Management Protocol)

FTP (File Transfer Protocol):



1. It is a standard mechanism provided by TCP/IP for copying a file from one host to another.
2. Transferring files from one computer to another is one of the most common tasks in networking.
3. FTP establishes two connection between the host.
4. One connection is used for data transfer and other for control information.
5. The data connection use very complex rules and control connection use simple rules.
6. The user have three components (i) use interface (ii) client process (iii) client data transfer process.
7. The server have two components:
   (i) Server control process (ii) Data transfer process
8. The control connection remains connected during the entire FTP session and data connection is opened/closed for each file transfer.

End of Solution

■■■■