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Detailed Solutions

ESE-2024 Mains Test Series

E & T Engineering Test No : 9

Section A : Digital Circuits + Analog Circuits

Q.1 (a) Solution:

Given,

Component	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
XOR	0.15 ns	2.1 ns	–	–
D_{REG}	0.1 ns	1.6 ns	0.4 ns	0.2 ns

(i) Minimum value of clock period can be determined using the setup time equation given by,

$$t_{clk} \geq t_{pd,\,REG} + 2 \times t_{pd,\,XOR} + t_{setup,\,REG}$$

$$\therefore \quad t_{clk\,min} = 1.6\text{ ns} + 2 \times 2.1\text{ ns} + 0.4\text{ ns}$$

$$\therefore \quad t_{clk(min)} = 6.2\text{ ns}$$

(ii) Setup time for IN with respect to clk (rising edge)

$$t_{setup(IN)} = 2 \times t_{pd,\,XOR} + t_{SETUP,\,REG}$$
$$= 2 \times (2.1\text{ ns}) + 0.4\text{ ns}$$
$$= 4.2\text{ ns} + 0.4\text{ ns}$$
$$= 4.6\text{ ns}$$

Hold time for IN with respect to rising edge of clk,

$$t_{HOLD(IN)} = t_{HOLD,\,REG} - t_{CD,\,XOR}$$
$$= 0.2\text{ ns} - 0.15\text{ ns} = 0.05\text{ ns}$$

(iii) Given a faster XOR' Gate,

$$t_{CD} = 0.05 \text{ ns}$$
$$t_{PD} = 0.7 \text{ ns}$$

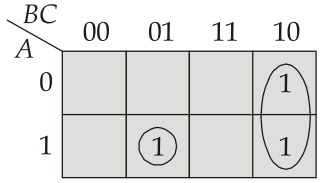
Minimum value for t_{clk} is not possible, because $t_{CD, REG} + t_{CD, XOR'} = 0.1 \text{ ns} + 0.05 \text{ ns} = 0.15 \text{ ns}$ which is less than the $t_{HOLD, REG} = 0.2 \text{ ns}$. Hence, hold-time constraints are not met.

Q.1 (b) Solution:

(i)

A	*B*	*C*	*F*(*A*, *B*, *C*)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

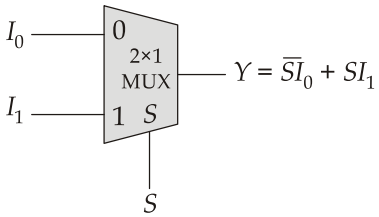
(ii) By using 3-Variable K-map,



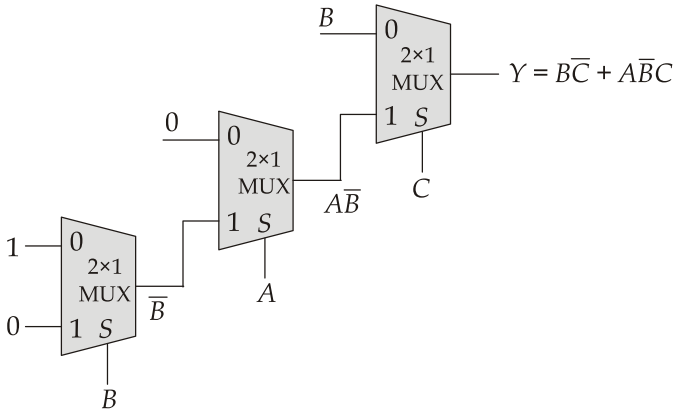
$$\therefore \quad F(A, B, C) = B\bar{C} + A\bar{B}C$$

(iii) $F(A, B, C) = B\bar{C} + A\bar{B}C$

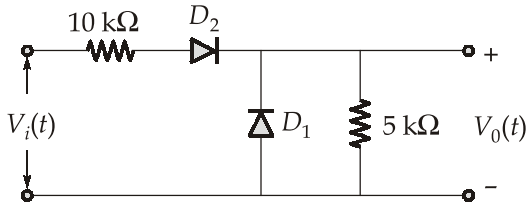
For a 2 × 1 MUX,



The boolean function F can be implemented using 2 × 1 MUX as below:



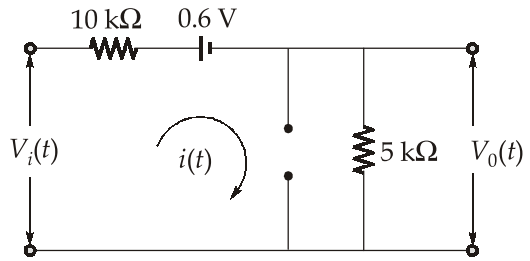
Q.1 (c) Solution:



Case-I:

$$V_i(t) > 0.6\ \text{V}$$

Diode D_2 is forward-biased and diode D_1 is reverse biased.



$$i(t) = \frac{V_i(t)-0.6}{(10+5)}\text{mA}$$

$$V_0(t) = (5\,\text{k}\Omega)i(t)$$

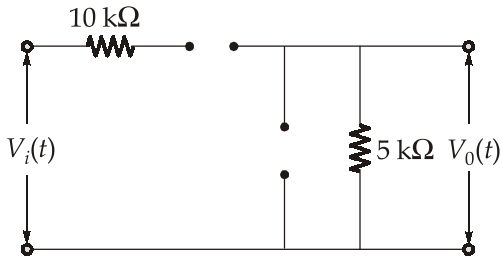
$$V_0(t) = \frac{5}{15}[V_i(t)-0.6]\text{V}$$

Case-II:

$$-0.6\ \text{V} < V_i(t) < 0.6\ \text{V}$$

Both the diodes D_1 and D_2 are reverse-biased.

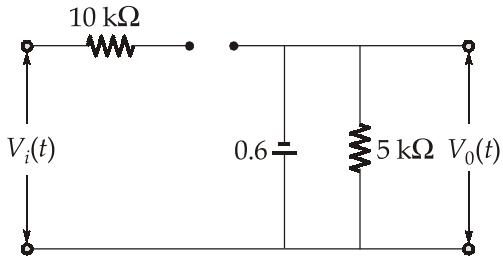
$$V_0(t) = 0\ \text{V}$$



Case-III:

$$V_i(t) < -0.6\ \text{V}$$

Diode D_2 is reversed-biased and diode D_1 is forward biased.



$$V_0(t) = -0.6\ \text{V}$$

For $V_i(t) = 0.6$ V

$$0.6 = 8\sin(150\pi t) = 8\sin\theta_1$$

$$\Rightarrow \quad \theta_1 = \sin^{-1}\left(\frac{0.6}{8}\right) = \sin^{-1}\left(\frac{3}{40}\right) = 4.30°, 175.698°$$

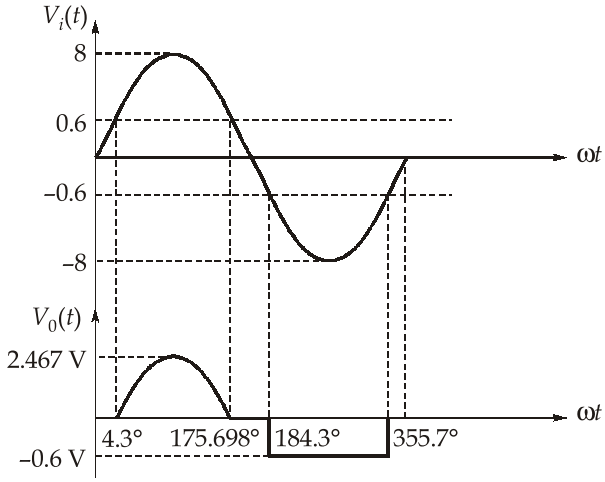
For $V_i(t) = -0.6$ V

$$\theta_2 = 180 + 4.3 = 184.30° \text{ or } 355.7°$$

Hence,

$$V_0(t) = \begin{cases} \frac{1}{3}(V_i(t) - 0.6)\ ; & 4.3° < \theta < 175.698° \\ -0.6V \quad\quad ; & 184.3° < \theta < 355.7° \\ 0 \quad\quad\quad ; & \text{elsewhere} \end{cases}$$

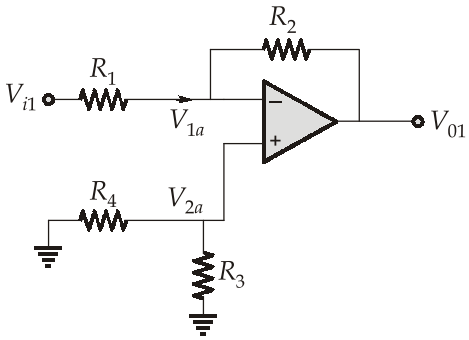
The input and output waveforms can be sketched as below:



Q.1 (d) Solution:

To solve the circuit, we will use superposition theorem and the virtual short concepts.

(i) When V_{i1} is acting alone:

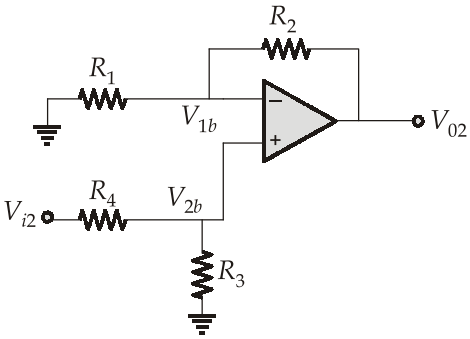


When input $V_{i2} = 0$, no current will flow in R_3 and R_4.

Hence, $V_{2a} = 0$. Using the virtual short concept, $V_{1a} = 0$

We get, $$V_{01} = \frac{-R_2}{R_1} V_{i1} \quad \text{...(i)}$$

When V_{i2} is acting alone:



As current through op-amp input terminals is zero, R_3 and R_4 form a voltage divider.

$$V_{2b} = \frac{R_3}{R_3 + R_4} V_{i2}$$

Also, $V_{2b} = V_{1b}$ (virtual short)

So, $$V_{02} = \left(1 + \frac{R_2}{R_1}\right) V_{1b} = \left(1 + \frac{R_2}{R_1}\right) V_{2b}$$

$$= \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_3}{R_3 + R_4}\right) V_{i2}$$

Which can be arranged as

$$V_{02} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_3 / R_4}{1 + R_3/R_4}\right) V_{i2} \quad \text{...(ii)}$$

Net output, $V_0 = V_{01} + V_{02}$

From equations (i) and (ii)

$$V_0 = \frac{-R_2}{R_1} V_{i1} + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_3/R_4}{1 + R_3/R_4}\right) V_{i2} \quad \text{...(iii)}$$

Given: $$\frac{R_2}{R_1} = \frac{R_3}{R_4}$$

Putting this in equation (iii), we get,

$$V_0 = \frac{R_2}{R_1}(V_{i2} - V_{i1})$$

(ii) The circuit is called difference amplifier. It is used in instrumentation amplifier. Although simple Op-amp is also a difference amplifier, this particular circuit gives us flexibility where output can be scaled by varying ratios of resistors.

(iii) The common mode signal,

$$V_{cm} = \frac{V_{i1} + V_{i2}}{2} \quad \text{...(iv)}$$

$$A_{cm} = \frac{V_0}{V_{cm}}$$

Given, $$\frac{R_3}{R_4} = 13, \frac{R_2}{R_1} = 12$$

From equation (iii),

$$V_0 = (1+12)\left(\frac{13}{1+13}\right)V_{i2} - 12V_{i1}$$

$$V_0 = \frac{13\times 13}{14}V_{i2} - 12V_{i1} \quad ...(v)$$

Also, $V_d = V_{i2} - V_{i1}$ with $A_d = V_0/V_d$ ...(vi)

From equation (iv) and (vi),

$$V_{i1} = V_{cm} - \frac{V_d}{2}$$

$$V_{i2} = V_{cm} + \frac{V_d}{2}$$

Put this in equation (v)

$$V_0 = 12.071\left(V_{cm} + \frac{V_d}{2}\right) - 12\left(V_{cm} - \frac{V_d}{2}\right)$$

$$= 12.0355\ V_d + 0.071\ V_{cm}$$

Comparing from standard equation,

$$V_0 = A_d V_d + A_{cm} V_{cm}$$

We get, $A_d = 12.0355,\ A_{cm} = 0.071$

$$\text{CMRR(dB)} = 20\log\frac{A_d}{A_{cm}} = 20\log\frac{12.0355}{0.071}$$

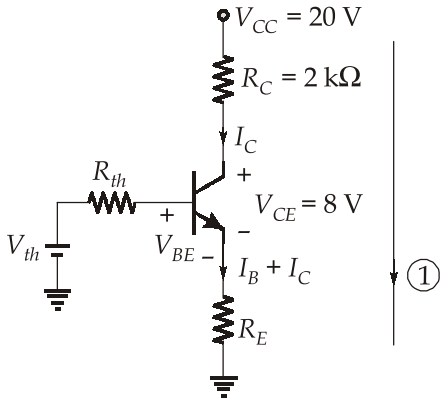
$$\text{CMRR(dB)} = 44.584\ \text{dB}$$

Q.1 (e) Solution:

The thevenin equivalent of the BJT circuit can be drawn as below with

$$V_{th} = \frac{R_2}{R_1+R_2}V_{CC} = \frac{20R_2}{R_1+R_2} \quad ...(i)$$

and $R_{th} = R_1 \parallel R_2$



Given collector current,

$$I_C = 4.2\text{ mA}$$

$$V_{CE} = 8\text{ V}$$

The emitter current,

$$I_E = \frac{(\beta+1)}{\beta} I_C = \frac{51}{50}\times 4.2$$

$$= 4.284\text{ mA}$$

Base current,

$$I_B = \frac{I_C}{\beta} = \frac{4.2}{50} = 0.084\text{ mA}$$

Using KVL,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$20 = 2 \times 4.2 + 8 + 4.284\, R_E$$

$$R_E = \frac{20 - 2\times 4.2 - 8}{4.284} = 0.84\text{ k}\Omega$$

The stability factor,

$$S(I_{CO}) = \frac{\left(1+\frac{R_{th}}{R_E}\right)(1+\beta)}{(1+\beta)+\frac{R_{th}}{R_E}} = 15$$

$$= \frac{\left(1+\frac{R_{th}}{R_E}\right)(1+50)}{(1+50)+\frac{R_{th}}{R_E}} = 15$$

Solving this,

$$\frac{R_{th}}{R_E} = 19.84$$

So,

$$R_{th} = 16.665\text{ k}\Omega$$

From circuit,

$$V_{th} = V_{BE} + R_{th} I_B + R_E(1+\beta) I_B$$

$$= 0.7 + 16.665 \times 0.084 + 51 \times 0.084 \times 0.84$$

$$= 5.698\text{ V}$$

From equation (i), we get

$$5.698 = \frac{20 R_2}{R_1 + R_2}$$

$$\frac{R_2}{R_1 + R_2} = \frac{5.698}{20} = 0.284 \qquad \text{...(ii)}$$

and $$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = 16.665 \quad \text{...(iii)}$$

Dividing equation (iii) by equation (ii) gives

$$R_1 = \frac{16.665}{0.284} = 58.679\ \text{k}\Omega$$

Now, from equation (ii),

$$\frac{R_2}{R_1 + R_2} = 0.284$$

$$R_2 = 0.284R_1 + 0.284R_2$$

$$0.716R_2 = 0.284R_1$$

$$R_2 = \frac{0.284}{0.716} \times 58.679$$

$$= 23.274\ \text{k}\Omega$$

Hence, $R_2 = 23.274\ \text{k}\Omega$

$R_1 = 58.679\ \text{k}\Omega$

$R_E = 0.84\ \text{k}\Omega$

Q.2 (a) Solution:

(i) The sequence of the Modulo 6 gray code counter can be obtained from the corresponding binary values using:

$$G_2 = B_2$$

$$G_1 = B_2 \oplus B_1$$

$$G_0 = B_1 \oplus B_0$$

Binary Code ($B_2B_1B_0$)			Gray Code ($G_2G_1G_0$)		
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1

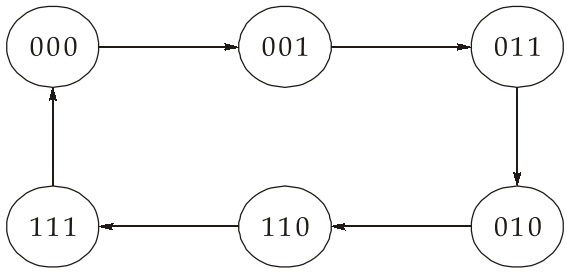
Number of flip-flops required are,

$N \le 2^n$, where N = number of states and n = number of flip-flops

$6 \le 2^n$

$\therefore \quad n = 3$ FFs

The state diagram for the modulo-6 gray code counter is given as below:

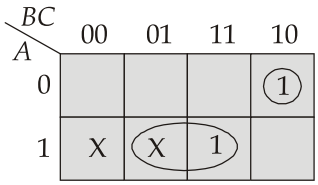


We don't care about the states 100 and 101.

The excitation table:

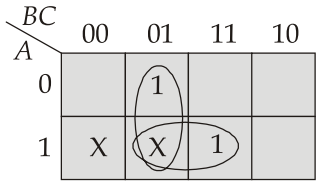
Present state			Next state					
A	B	C	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	0	1
0	1	0	1	1	0	1	0	0
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

For T_A:



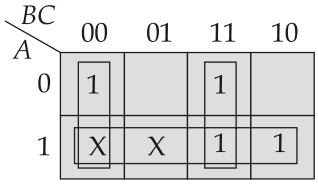
$$T_A = \bar{A}B\bar{C} + AC$$

For T_B:



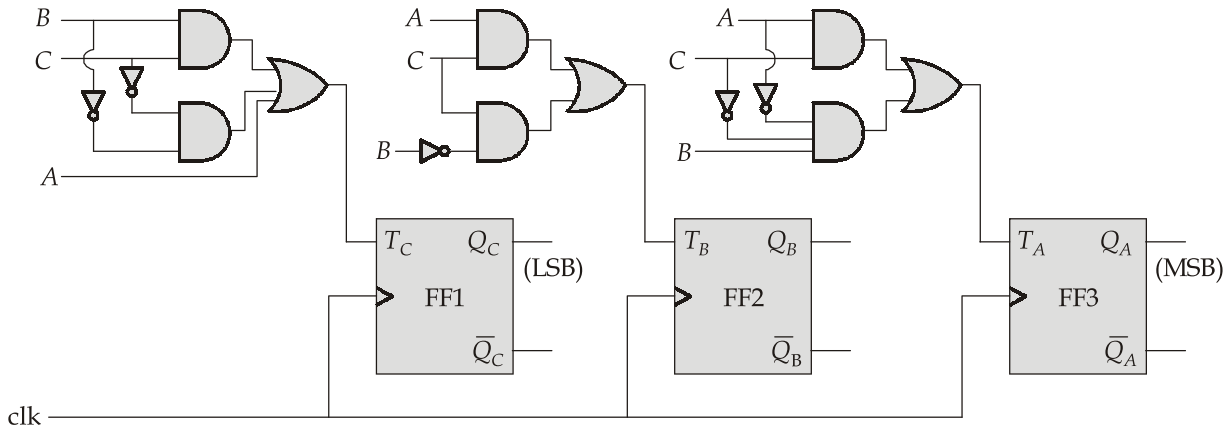
$$T_B = AC + \bar{B}C$$

For T_C:



$$T_C = A + \bar{B}\bar{C} + BC$$

Logic Circuit:



(ii) Given, 10-bit DAC

$$V_{FS} = 10.23 \text{ V}$$

For a 10-bit DAC, number of total possible steps is $2^{10} - 1 = 1023$

$$\therefore \quad \text{step size} = \frac{V_{FS}}{2^n - 1} = \frac{10.23}{1023} = 10 \text{ mV}$$

i.e, V_{AX} increases in steps of 10 mV as the counter counts up from zero.

given, $V_A = 3.728$ V,

$V_T = 0.1$ mV

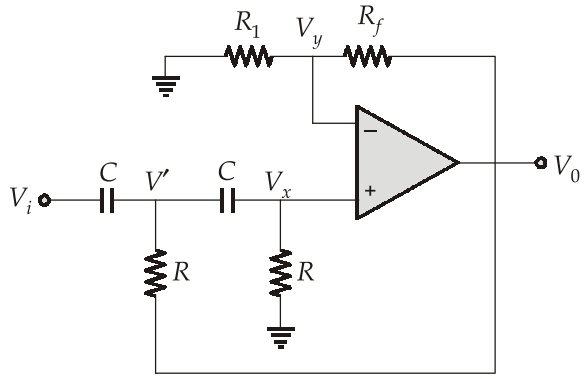
$\therefore$ V_{AX} has to reach 3.728 + 0.1 mV = 3.7281 V or more before the comparator switches low,

this require $\frac{3.7281 \text{ V}}{10 \text{ mV}} = 372.81 \simeq 373 \text{ steps}$

$\therefore$ At the end of the conversion, the counter holds the binary equivalent of 373 i.e, 0101110101_2 which is the desired digital equivalent of analog input $V_A = 3.728$ V produced by the given ADC.

Q.2 (b) Solution:

(i)



Here, $V_y = \frac{V_0}{R_f + R_1} \times R_1$ and $V_x = V_y$ (using virtual short concept)

Applying KCL at node V',

$$\frac{V' - V_i}{1/sC} + \frac{V' - V_x}{1/sC} + \frac{V' - V_0}{R} = 0 \quad ...(1)$$

Applying KCL at node V_x,

$$\frac{V_x - V'}{1/sC} + \frac{V_x}{R} = 0 \quad ...(2)$$

Applying KCL at node V_y,

$$\frac{V_x}{R_1} + \frac{V_x - V_0}{R_f} = 0; \text{ since } V_x = V_y \text{ using virtual short concept} \quad ...(3)$$

On solving equation (1), (2) and (3), we get,

$$\frac{V_0(s)}{V_i(s)} = \frac{Ks^2}{s^2 + s\left(\frac{3-K}{RC}\right) + \left(\frac{1}{RC}\right)^2}$$

where $K = \frac{R_1 + R_f}{R_1}$ = DC gain of amplifier

On substituting, $s = j\omega$, the transfer function is obtained as

$$H(j\omega) = \frac{V_0(j\omega)}{V_i(j\omega)} = \frac{-KR^2C^2\omega^2}{1 + j(3-K)\omega RC - R^2C^2\omega^2}$$

$$|H(j\omega)| = \frac{K\left(\frac{\omega}{\omega_c}\right)^2}{\sqrt{\left[1 - \left(\frac{\omega}{\omega_c}\right)^2\right]^2 + (3-K)^2\left(\frac{\omega}{\omega_c}\right)^2}}; \text{ where } \omega_c = \frac{1}{RC}$$

In above expression, when $\omega \to 0$, $|H(j\omega)| = 0$. Thus low frequency gain of the filter is zero and when $\omega \to \infty$, $|H(j\omega)| = K$, i.e., high frequency gain of K. So, given filter is a high pass filter.

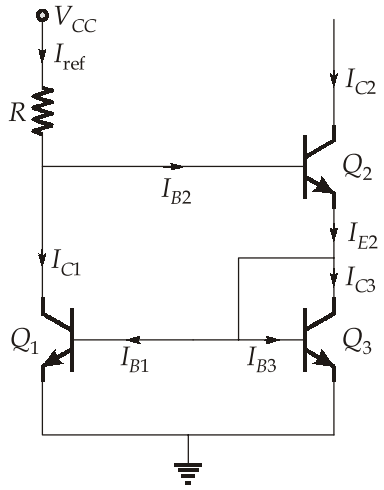
(ii) Advantages of an active filter over a passive filter.

1. **Less Cost:** Active filters are more economical than passive filters due to the variety of cheaper op-amp and the absence of costly inductors.
2. **Gain and frequency adjustment flexibility:** Since the op-amp is capable of providing a gain (which may also be variable), the input signal is not attenuated as it is in a passive filter. In addition, the active filter is easier to tune or adjust.

3. **No loading problem:** Active filters provide an excellent isolation between the individual stages due to the high input impedance (ranging from a few kΩ to a several thousand MΩ) and low output impedance (ranging from less than 1 Ω to a few hundred Ω). So, the active filter does not cause loading of the source or load.
4. **Size and weight:** Active filters are small in size and less bulky (due to the absence of bulky inductors) and are rugged.
5. **Non-floating input and output:** Active filters generally have single-ended inputs and outputs which do not 'float' with respect to the system power supply or common. This property is different from that of the passive filters.
6. **Adjustability:** The characteristics of active filters, such as the cutoff frequency and gain can be easily adjusted by changing resistor and capacitor values or by tuning the active components as compared to passive filters which require physical changes to the components.
7. **Stability and reliability:** Active filters are less sensitive to variations in component values due to temperature changes and aging, providing more stable performance over time compared to passive filters.
8. **Higher order filtering:** Implementing higher-order filters is more straight forward with active filters since they can be cascaded easily without the need for inter-stage buffering, which is often required in passive filters.

Q.2 (c) Solution:

(i)



$$I_{ref} = I_{B2} + I_{C1}$$

$$I_{E2} = I_{C3} + I_{B1} + I_{B3}$$

Since, $V_{BE1} = V_{BE3}$, we have $I_{B1} = I_{B3} = I_B$ (say)

$$\therefore \quad I_{E2} = I_{C3} + 2I_B$$

We have, $$I_B = \frac{I_{C3}}{\beta}$$

$$\therefore \quad I_{E2} = I_{C3} + \frac{2I_{C3}}{\beta}$$

$$I_{E2} = I_{C3}\left(1 + \frac{2}{\beta}\right)$$

Now, $$I_{C2} = I_{E2}\left(\frac{\beta}{1+\beta}\right)$$

$$I_{C2} = I_{C3}\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right) \quad \text{...(i)}$$

$$I_{C3} = I_{C2} \times \frac{1}{\left(\frac{\beta}{1+\beta}\right)\left(1 + \frac{2}{\beta}\right)}$$

$$\therefore \quad I_{ref} = I_{C1} + I_{B2}$$

$$I_{C1} = I_{ref} - I_{B2}$$

$$I_{C1} = I_{ref} - \frac{I_{C2}}{\beta} \quad \text{...(ii)}$$

But $$I_{C3} = I_{C1}$$

From equation (i) and (ii),

$$I_{C2} \times \frac{1}{\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} = I_{ref} - \frac{I_{C2}}{\beta}$$

Thus, $$I_{C2} = I_{ref} \times \left(\frac{\beta(\beta+2)}{\beta^2 + 2\beta + 2}\right)$$

$$I_{C2} = I_{ref}\left[1 - \frac{2}{\beta^2 + 2\beta + 2}\right]$$

(ii) 1. $(447)_8$

Convert into decimal

$$(447)_8 = 4 \times 8^2 + 4 \times 8^1 + 7 \times 8^0$$
$$= 4 \times 64 + 32 + 7$$
$$= 256 + 39 = (295)_{10}$$

12	295	7
12	24	0
	2	

$$(447)_8 \longleftrightarrow (207)_{12}$$

2. $(01101111)_2$

Convert to decimal

$$(01101111)_2 = 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$$
$$= 64 + 32 + 8 + 4 + 2 + 1$$
$$= 71 + 40 = (111)_{10}$$

7	111	6
7	15	1
	2	

$$(01101111)_2 \longleftrightarrow (216)_7$$

3. $(113)_6$

Convert to decimal

$$(113)_6 = 1 \times 6^2 + 1 \times 6^1 + 3 \times 6^0$$
$$= 36 + 6 + 3 = (45)_{10}$$

$$(113)_6 \longleftrightarrow (45)_{10}$$

4. $(76A2)_{16}$

Convert to decimal

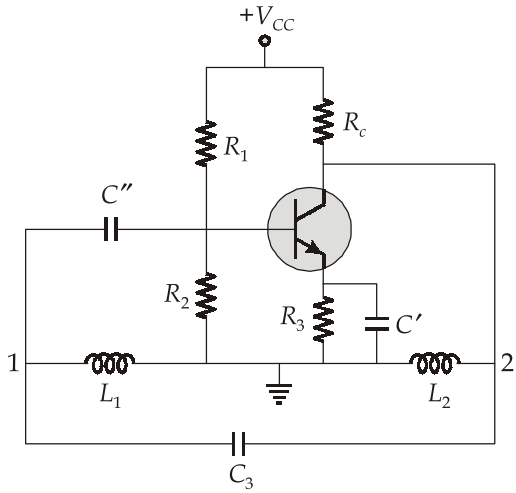
$$(76A2)_{16} = 7 \times 16^3 + 6 \times 16^2 + 10 \times 16 + 2 \times 16^0$$
$$= 28672 + 1536 + 160 + 2 = (30370)_{10}$$

4	30370	2
4	7592	0
4	1898	2
4	474	2
4	118	2
4	29	1
4	7	3
	1	

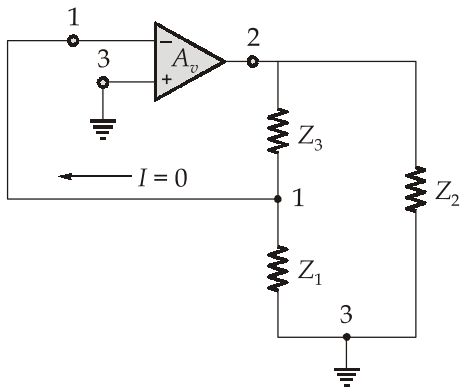
$$(76A2)_{16} \longleftrightarrow (13122202)_4$$

Q.3 (a) Solution:

(i) The Hartely oscillator using transistor is as shown below:



Using Op-amp, Hartley Oscillator is as shown below:



$$Z_1 = jX_1, \qquad Z_2 = jX_2, \qquad Z_3 = jX_3$$

$$X_1 = \omega L_1, \qquad X_2 = \omega L_2, \qquad X_3 = \frac{1}{\omega C_3}$$

Load impedance, $Z_L = Z_2 \| (Z_1 + Z_3)$

The gain without feedback is

$$A = \frac{-A_V Z_L}{Z_L + R_o}$$; (where A_V is internal gain of amplifier and R_0 is the output impedance of amplifier)

Feedback factor, $\beta = \dfrac{-Z_1}{Z_1 + Z_3}$

Loop gain, $-A\beta = \dfrac{-A_V Z_1 Z_L}{(Z_1 + Z_3)(Z_L + R_o)}$

We have, $$Z_L = \frac{Z_2(Z_1+Z_3)}{Z_1+Z_2+Z_3}$$

$$\therefore \quad -A\beta = \frac{-A_V Z_1 \dfrac{Z_2(Z_1+Z_3)}{Z_1+Z_2+Z_3}}{(Z_1+Z_3)\left[\dfrac{Z_2(Z_1+Z_3)}{Z_1+Z_2+Z_3}+R_0\right]}$$

$$-A\beta = \frac{-A_V Z_1 Z_2}{Z_2(Z_1+Z_3)+R_0(Z_1+Z_2+Z_3)}$$

$$A\beta = \frac{(A_V)(jX_1)(jX_2)}{jX_2(jX_1+jX_3)+R_0(jX_1+jX_2+jX_3)}$$

$$A\beta = \frac{-A_V X_1 X_2}{(-X_2X_1-X_2X_3)+jR_0(X_1+X_2+X_3)}$$

$$A\beta = \frac{-A_V X_1 X_2(-X_2X_1-X_2X_3-jR_0(X_1+X_2+X_3))}{(-X_2X_1-X_2X_3)^2+R_0^2(X_1+X_2+X_3)^2}$$

$$A\beta = \frac{(X_2X_1)^2 A_V + A_V X_1 X_2^2 X_3 + jA_V X_1 X_2 R_0(X_1+X_2+X_3)}{(-X_2X_1-X_2X_3)^2+R_0^2(X_1+X_2+X_3)^2(-X_2X_1-X_2X_3)^2+R_0^2(X_1+X_2+X_3)^2} \quad ...(i)$$

As per Barkhausen criteria, at oscillation frequency (ω_0) imaginary part of the loop gain must be zero. Hence,

$$X_1 + X_2 + X_3 = 0$$

Substituting values of X_1, X_2 and X_3, we get $\omega_o L_1 + \omega_o L_2 - \dfrac{1}{\omega_o C_3} = 0$

$$\omega_o(L_1+L_2) = \frac{1}{\omega_o C_3}$$

$$\omega_o^2 = \frac{1}{(L_1+L_2)C_3}$$

$$\omega_o = \frac{1}{\sqrt{(L_1+L_2)C_3}}$$

Frequency of oscillation is,

$$f_o = \frac{1}{2\pi}\frac{1}{\sqrt{(L_1+L_2)C_3}}$$

From equation (i) for $X_1 + X_2 + X_3 = 0$ we get

$$A\beta = \frac{(X_2X_1)^2 A_V + A_V X_1 X_2^2 X_3}{(-X_2X_1-X_2X_3)^2}$$

$$A\beta = \frac{A_V X_1 X_2 [X_1 X_2 + X_2 X_3]}{(X_2 X_1)^2 + (X_2 X_3)^2 + 2X_1 X_2^2 X_3}$$

$$A\beta = \frac{A_V X_1 X_2 [X_1 X_2 + X_2 X_3]}{X_2^2 \left[X_1^2 + X_3^2 + 2X_1 X_3 \right]}$$

$$A\beta = \frac{A_V X_1 [X_1 + X_3]}{(X_1 + X_3)^2}$$

$$A\beta = \frac{A_V X_1}{(X_1 + X_3)}$$

$\therefore \quad X_1 + X_2 + X_3 = X_1 + X_3 = -X_2$

$$A\beta = \frac{-A_V X_1}{X_2}$$

For oscillation to start, $|A\beta| \geq 1$ (Barkhausen criteria)

$$\frac{A_V X_1}{X_2} \geq 1$$

$$\frac{X_2}{X_1} \leq A_V$$

$$\frac{\omega_o L_2}{\omega_o L_1} \leq A_V$$

$$A_V \geq \frac{L_2}{L_1}$$

(ii) For the given comparator circuit,

$$V_o = \begin{cases} +V_{sat} & ; \text{ for } V_i > 2 \text{ V} \\ -V_{sat} & ; \text{ for } V_i < 2 \text{ V} \end{cases}$$

It is given that, $V_{pp} = 10$ V, Hence,

$V_i = 5\sin(\omega t)$ V

At $V_i = 2$ V

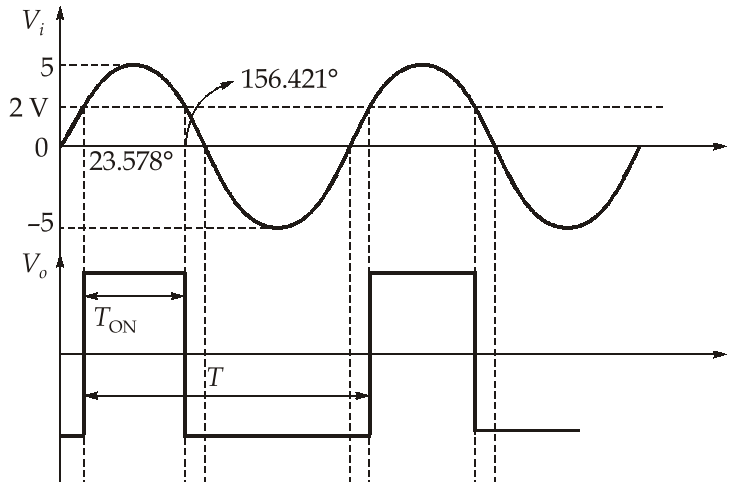
$$2 = 5\sin(\omega t)$$

$$\omega t = \sin^{-1}(0.4)$$

$$\omega t = 23.578°, \quad 156.421°$$

In one input cycle, for $23.578° < \omega t < 156.421°$, $V_i > 2$V. Hence, $V_0 = V_{sat}$

The input and output waveforms can be sketched as below:



$$\text{Duty cycle} = \frac{T_{ON}}{T} = \frac{156.421 - 23.578}{360} = 0.369$$

$$\% \text{ Duty cycle} = 36.9\%$$

Q.3 (b) Solution:

For Full adder

A	*B*	*C*	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum, } F_s(A, B, C) = \Sigma m(1, 2, 4, 7)$$

$$F_s(A, B, C) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

For CMOS logic implementation,

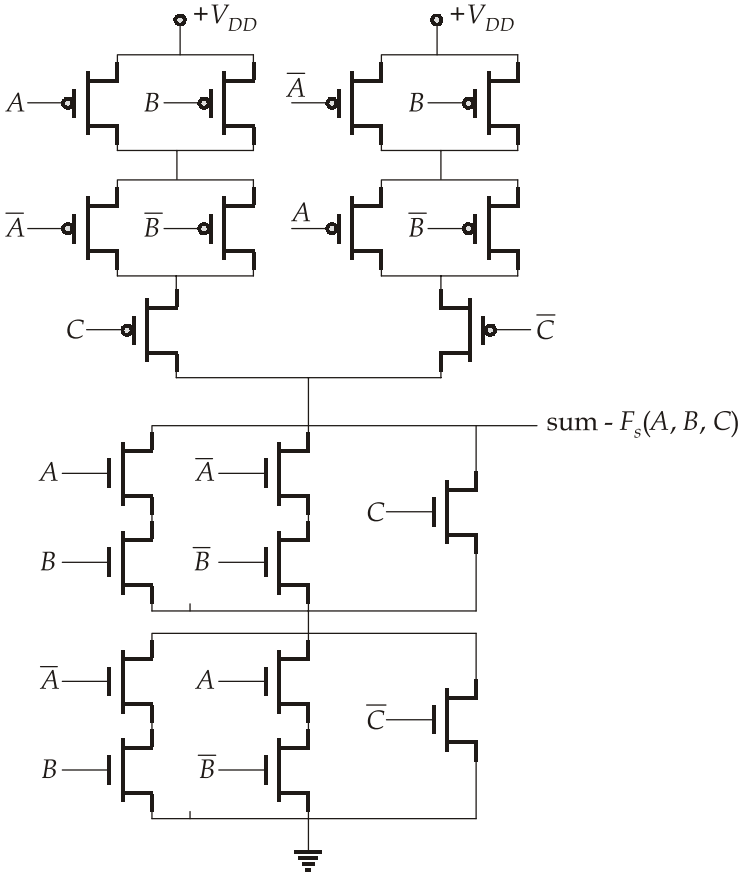
$$F_s(A,B,C) = \overline{\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC}$$

$$= \overline{C(\bar{A}\bar{B} + AB) + \bar{C}(A\bar{B} + \bar{A}B)}$$

Using DeMorgan's Law,

$$= \overline{\left[(A+\bar{B})(\bar{A}+B)+C\right]\left[(\bar{A}+\bar{B})(A+B)+\bar{C}\right]}$$

$$F_s(A,B,C) = \overline{\left[AB+\bar{A}\bar{B}+C\right]\left[\bar{A}B+A\bar{B}+\bar{C}\right]}$$



$$F_C(A,B,C) = \Sigma m(3,5,6,7)$$

$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

For CMOS implementations,

$$\overline{F_C}(A,B,C) = \overline{\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC}$$

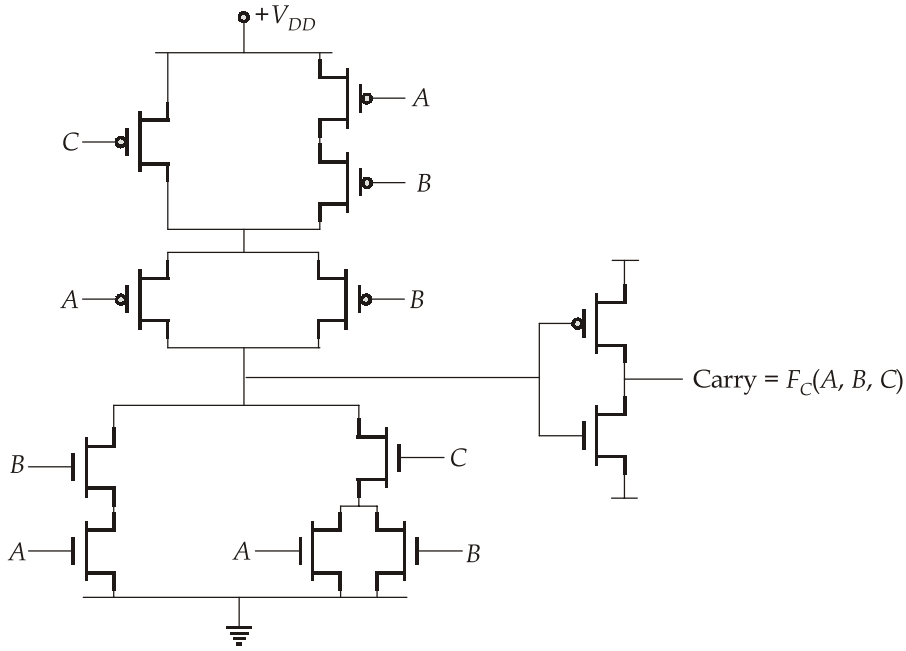
$$= \overline{AB(C+\bar{C}) + \bar{A}BC + A\bar{B}C}$$

$$= \overline{AB + \bar{A}BC + A\bar{B}C}$$

$$= \overline{A(B+\bar{B})(B+C) + \bar{A}BC}$$

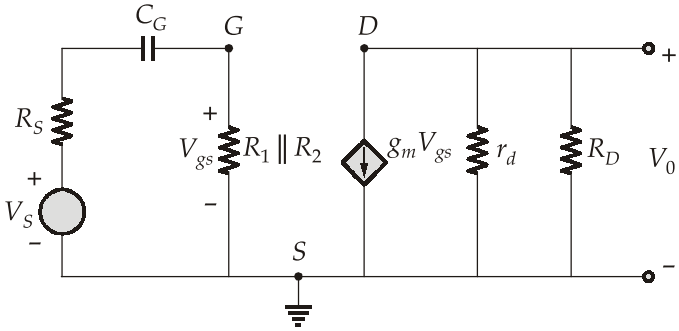
$$= \overline{A(B+C) + \bar{A}BC}$$

$$= \overline{(AB + C(A+B))}$$



Q.3 (c) Solution:

(i) Assuming $R_s'C_s'$ bias as a short, the small signal equivalent of the circuit can be drawn as below:



$$V_0 = -g_m V_{gs}(r_d \parallel R_D) \qquad ...(1)$$

At mid-band, the capacitor C_G acts as short-circuit.

Hence, $$V_{gs} = V_s\left[\frac{R_1 \parallel R_2}{R_s + (R_1 \parallel R_2)}\right]$$

Using equation (i),

$$\frac{V_0}{V_s} = -g_m(r_d \parallel R_D)\left[\frac{R_1 \parallel R_2}{R_s + R_1 \parallel R_2}\right]$$

Substituting the given values,

$$-28 = -5(r_d \parallel R_D)\left[\frac{170 \parallel 45}{0.35 + 170 \parallel 45}\right]$$

$$28 = 5(25 \| R_D)\left[\frac{35.581}{0.35+35.581}\right]$$

$$\frac{28}{5}\times\frac{35.931}{35.581} = \frac{25\times R_D}{25+R_D}$$

$$5.655 = \frac{25R_D}{25+R_D}$$

$$141.377 + 5.655R_D = 25R_D$$

$$19.345R_D = 141.377$$

$$R_D = \frac{141.377}{19.345} = 7.31\ \text{k}\Omega$$

The lower cut-off frequency, f_L due to C_G is

$$f_L = \frac{1}{2\pi C_G[R_s + (R_1 \| R_2)]}$$

$$220 = \frac{1}{2\pi C_G\left[0.35+\frac{170\times 45}{170+45}\right]}$$

$$C_G = \frac{1}{2\pi\times 220\left[0.35+\frac{170\times 45}{170+45}\right]}$$

$$= 2.0133 \times 10^{-5}\ \text{F}$$

$$C_G = 20.13\ \mu\text{F}$$

(ii) Given, $I_{DQ} = 1.25\ \text{mA}$

Since the transistor is in saturation region, thus the transconductance can be calculated as,

$$g_m = \frac{dI_D}{dV_{GS}}$$

We have, $$I_{DQ} = \frac{1}{2}\frac{\mu_n C_{ox} W}{L}(V_{GS}-V_{TN})^2$$

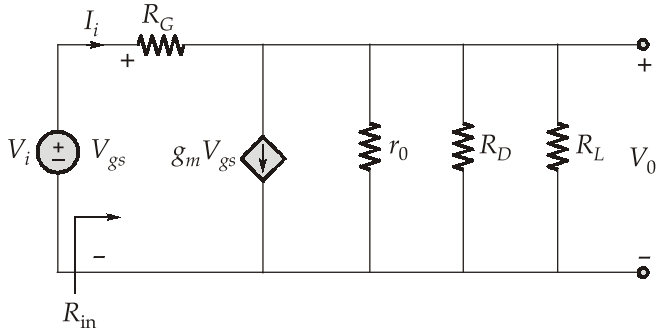
$$g_m = \frac{\mu_n C_{ox} W}{L}(V_{GS}-V_{TN})$$

$$= \sqrt{2\left(\frac{\mu_n C_{ox} W}{L}\right) I_{DQ}} = \sqrt{2\times 0.28\times 1.25\times 10^{-6}}$$

$$g_m = 0.8366\ \text{mA/V}$$

$$r_0 = \frac{V_A}{I} = \frac{60}{1.25} \times 10^3 = 48\text{k}\Omega$$

Now, drawing the small signal model, we get



$$I_i = \frac{V_i - V_0}{R_G} = \frac{V_i}{R_G}\left(1 - \frac{V_0}{V_i}\right) \qquad \text{...(i)}$$

Now, applying KCL, at node V_0, we get

$$V_0\left[\frac{1}{r_0} + \frac{1}{R_D} + \frac{1}{R_L}\right] + g_m V_i + \frac{V_0 - V_i}{R_G} = 0 \qquad [\because V_{gs} = V_i]$$

$$V_0\left[\frac{1}{r_0} + \frac{1}{R_D} + \frac{1}{R_L} + \frac{1}{R_G}\right] = -\left[g_m - \frac{1}{R_G}\right]V_i$$

$$\frac{V_0}{V_i} = \frac{-\left[0.8366\times10^{-3} - \frac{1}{12\times10^6}\right]}{\left(\frac{1}{48K} + \frac{1}{15K} + \frac{1}{10K} + \frac{1}{12\times10^6}\right)} = \frac{-8.365\times10^{-4}}{0.1875\times10^{-3}}$$

$$\therefore \quad \frac{V_0}{V_i} = -4.4613$$

From equation (i),

$$\frac{V_i}{R_G}[1 - (-4.4613)] = I_i$$

$$\frac{I_i}{V_i} = \frac{1 + 4.4613}{12\times10^6}$$

$$R_{in} = \frac{V_i}{I_i} = \frac{12\times10^6}{5.4613} = 2.197\ \text{M}\Omega$$

Q.4 (a) Solution:

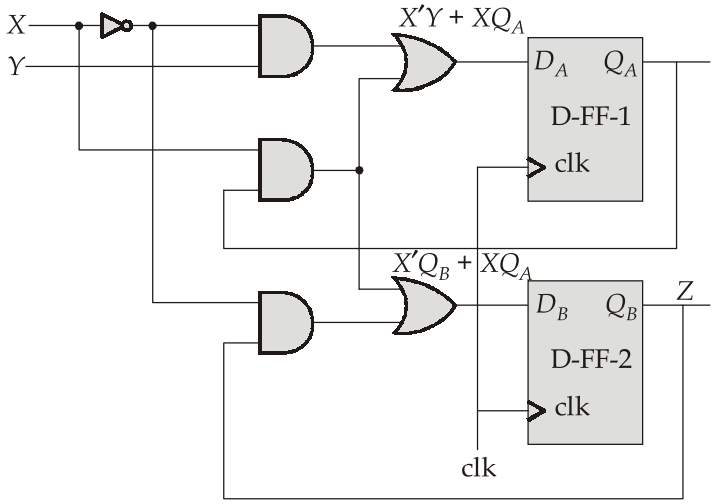
(i) Given,

$$Q_A(t+1) = X'Y + XQ_A$$

$$Q_B(t+1) = X'Q_B + XQ_A$$

$$Z = Q_B$$

Using above state equations, the logic circuit can be drawn as below:



(ii) From the given output equation

$$Q_A(t+1) = X'Y + XQ_A$$

for $X = 0$, $Y = 0$, $Q_A = 0$, $Q_B = 0$

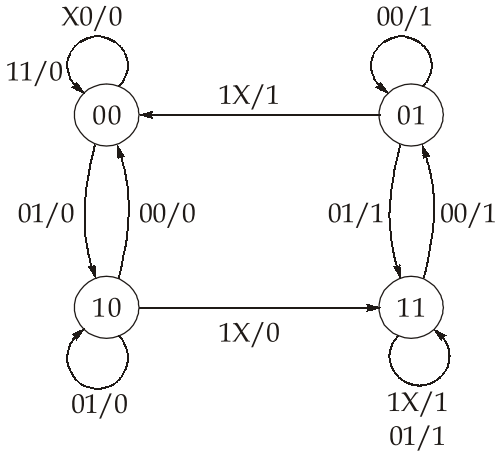
$$Q_A(t+1) = 1.0 + 0.0 = 0$$

$$\text{Output } Z = Q_B = 0$$

In a similar fashion, the state table is obtained as below:

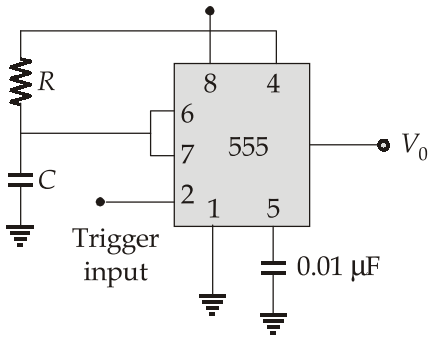
Present state		Inputs		Next state		Output
Q_A	Q_B	X	Y	Q_A^+	Q_B^+	Z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

(iii) State diagram:



Q.4 (b) Solution:

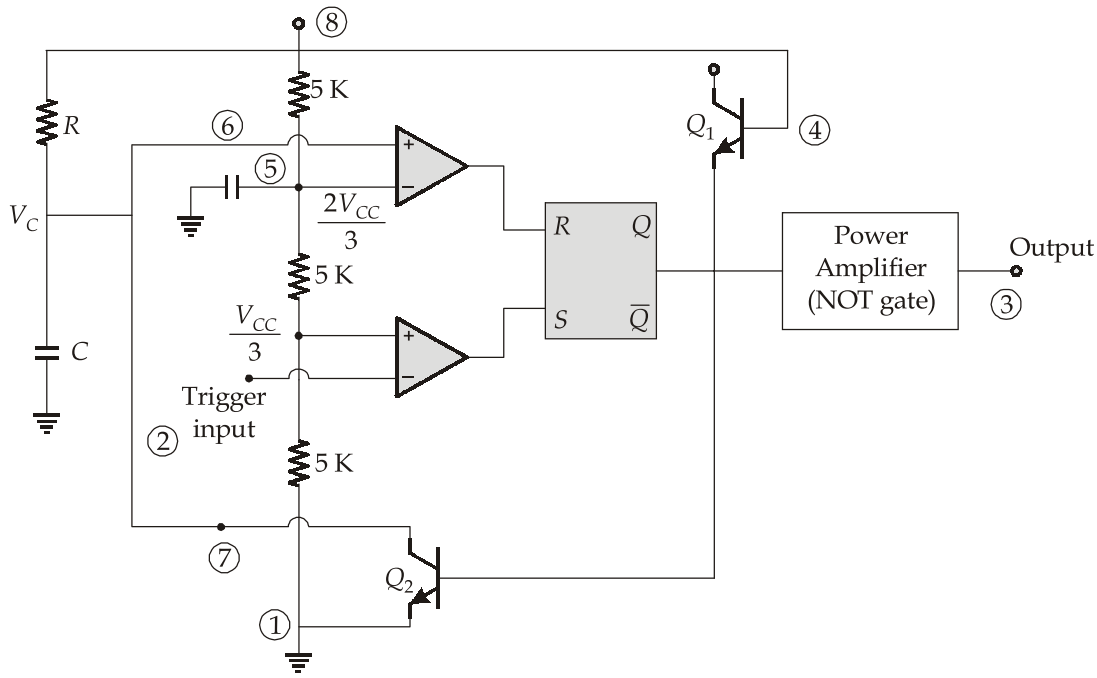
(i) The 555 IC can be configured to work as an monostable multivibrator as shown below:



The output of the monostable multivibrator using 555 timer remains in its stable state until it gets a trigger. We have,

Stable state : $V_o = 0$

Quasi stable state : V_o = "1" or V_{CC}



Case-I (Trigger input is not applied):

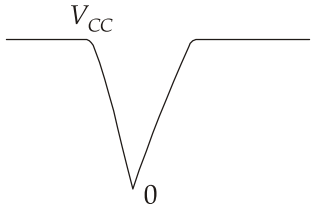
Output remain in stable state, hence

$$V_o = 0$$

As $V_o = 0$; $\overline{Q} = 1 \Rightarrow Q_2 = \text{ON}$

Hence, capacitor discharge fully through Q_2 and voltage across capacitor, $V_C = 0$.

Case-II (Trigger input is applied):



If trigger input is a negative spike, voltage at trigger pin becomes zero when trigger is applied and lower comparator generates logic 1 output causes SET input 'S' to flip flop as logic '1'.

If $S = 1$; $Q = 1$; $\overline{Q} = 0 \Rightarrow V_o = 1$

Hence, output changes to Quasi stable state.

When $V_o = 1 \Rightarrow \overline{Q} = 0 \Rightarrow Q_2 = \text{OFF}$.

Discharge path is disconnected, therefore capacitor can't discharge. Hence, capacitor starts charging through resistor R.

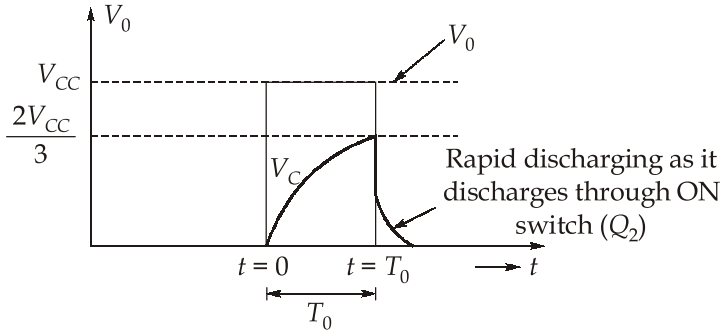
V_C increases exponentially upto $\frac{2V_{CC}}{3}$.

When V_C becomes > $\frac{2V_{CC}}{3}$ then upper comparator generates logic 1 output which acts as RESET input to flip flop.

If $R = 1$; $Q = 0$

$$\bar{Q} = 1 \Rightarrow V_o = 0$$

Hence, output returns back to stable state



When capacitor is charging,

$$V_C = V_{CC}(1 - e^{-t/RC})$$

At $t = T_0$; $V_C = \frac{2V_{CC}}{3}$

$$\frac{2V_{CC}}{3} = V_{CC}(1 - e^{-T_o/RC})$$

$$e^{-T_o/RC} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$T_o = RC \ln(3) = 1.1\, RC$$

It is given that $T_0 = 1$ μs. Hence,

$$1.1\ RC = 1 \times 10^{-6}$$

$$\therefore \quad R = \frac{1\times10^{-6}}{325\times10^{-12}} = 3.076\ \text{k}\Omega$$

(ii) 1. For FWR with inductor filter, ripple factor

$$r = \frac{R_L}{3\sqrt{2}\,\omega_o L} = \frac{650}{3\sqrt{2}\times 2\pi\times 60\times 6} = 0.0677$$

2. DC Output voltage, $V_{DC} = \frac{2V_m}{\pi} - I_{DC}R = \frac{2V_m}{\pi} - \frac{V_{DC}}{R_L}\cdot R$

$$V_{DC}\left(1+\frac{R}{R_L}\right) = \frac{2V_m}{\pi} \quad \text{...(i)}$$

where, $R = \frac{R_{sw}}{2} + R_f + R_{ind} = \frac{45}{2} + 20 + 30 = 72.5\ \Omega$

We have $\frac{V_m}{\sqrt{2}} = 50 \Rightarrow V_m = 50\sqrt{2} = 70.7106$ V

Putting above value is equation (i),

$$V_{DC}\left(1+\frac{72.5}{650}\right) = \frac{2\times 70.71}{\pi}$$

$$V_{DC}(1.115) = 45.015$$

$$V_{DC} = \frac{45.015}{1.115} = 40.372 \text{ V}$$

AC output voltage is V'_{rms} so

$$V'_{rms} = r\, V_{DC} = 0.0677 \times 40.372 = 2.733 \text{ V}$$

3. $$\%\ \text{Regulation} = \frac{R}{R_L}\times 100\% = \frac{72.5}{650}\times 100 = 11.15\%$$

Q.4 (c) Solution:

(i) Given, digital input,

$$00110010_2 = 2^5 \times 1 + 2^4 \times 1 + 2^1 \times 1 = 32 + 16 + 2 = 50_{10}$$

We have, V_0 = (Resolution) × (Decimal equivalent of binary input)

Thus, $1.0 \text{ V} = K \times 50$

$\therefore$ $$K = \frac{1}{50} = 20 \text{ mV}$$

The largest output will occur for an input of 11111111_2 in 8-bit DAC.

i.e., $11111111_2 = 2^7 \times 1 + 2^6 \times 1 + 2^5 \times 1 + 2^4 \times 1 + 2^3 \times 1 + 2^2 \times 1 + 2^1 \times 1 + 2^0 \times 1$

$$= 255_{10}$$

$\therefore$ Largest value of output voltage,

$$V_{out} = K \times 255$$

$$= 20 \times 10^{-3} \times 255$$

$$V_{out} = 5.10 \text{ V}$$

(ii) Given, 8-bit DAC,

$$I_{FS} = 2 \text{ mA}$$

$$\text{Step size} = \frac{I_{FS}}{2^N - 1} = \frac{2\text{ mA}}{2^8 - 1} = \frac{2\text{ mA}}{255} = 7.84\,\mu\text{A}$$

Given, input $10000000_2 = 128_{10}$

$\therefore$ The ideal output should be $128 \times 7.84\,\mu\text{A}$

$= 1003.52\,\mu\text{A}$

The error can be as much as $\pm 0.5\% \times 2$ mA

$= \pm 10\,\mu\text{A}$

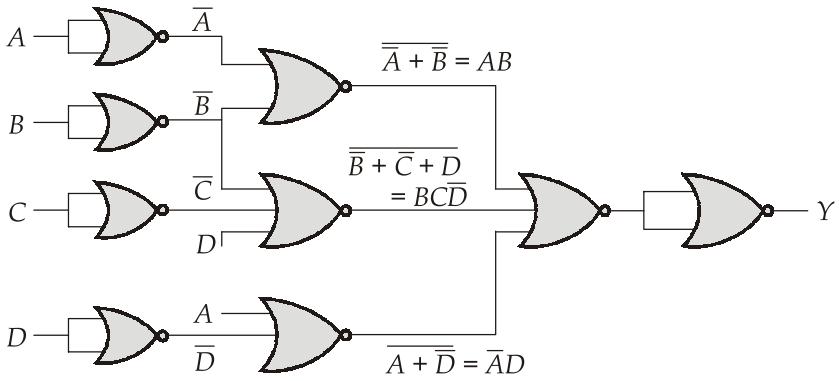
Thus, the actual output can deviate by this amount from the ideal 1003.52 μA.

So, actual output can be anywhere from (1003.52 – 10) μA to (1003.52 + 10) μA i.e., 993.52 μA to 1013.52 μA

(iii) Given $Y = AB + BC\bar{D} + \bar{A}D$

$$\bar{\bar{Y}} = Y = \overline{\overline{AB + BC\bar{D} + \bar{A}D}}$$

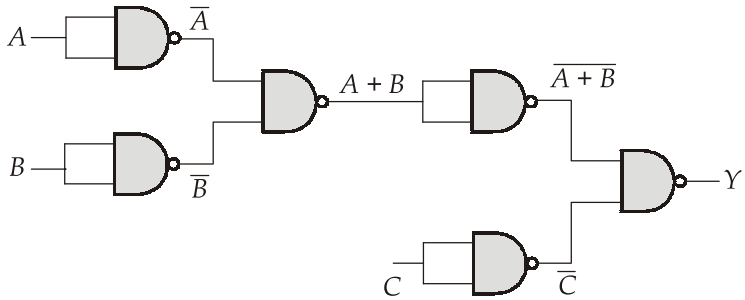
$$Y = \overline{\overline{(\bar{A} + \bar{B}) + (\bar{B} + \bar{C} + D) + (A + \bar{D})}}$$



(iv) Given $Y = A + B + C = (A + B) + C$

$$\bar{\bar{Y}} = Y = \overline{(\overline{A + B}) \cdot \bar{C}}$$

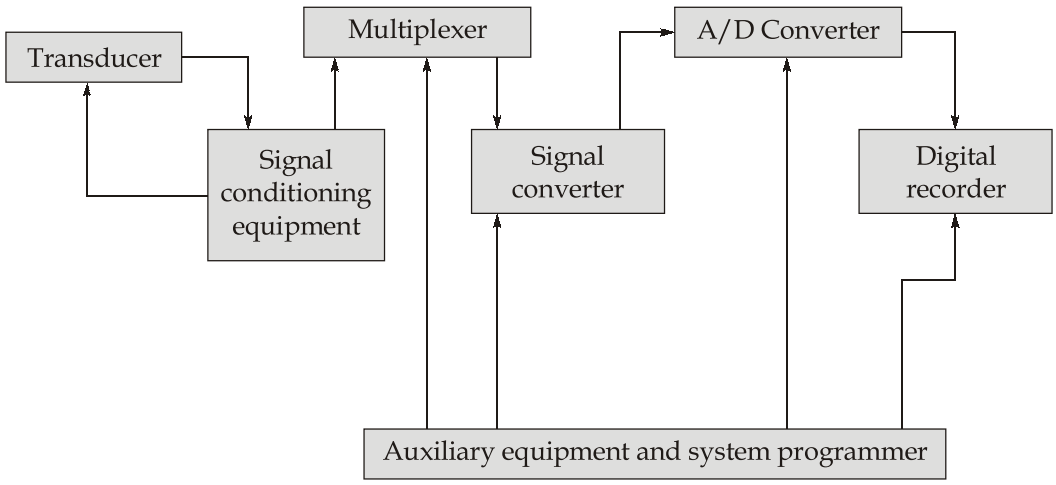
$$Y = \overline{\bar{\bar{A}} \cdot \bar{\bar{B}} \cdot \bar{C}}$$



Section B : Advanced Electronics-2 + Electronic Measurements and Instrumentation-2

Q.5 (a) Solution:

A generalized diagram of a digital data acquisition system is shown below:



Digital data acquisition system

A digital data acquisition system may include some or all of the components shown in figure. The essential functional operations of a digital data acquisition system are:

(a) handling of analog signals,

(b) making the measurement,

(c) converting the data to digital form and handling it, and

(d) internal programming and control.

The various components and their functions are described below:

1. **Transducer:** They convert a physical quantity into an electrical signal which is acceptable by the data acquisition system.
2. **Signal Conditioning Equipment:** Signal conditioning or data acquisition equipment is an excitation and amplification system for passive transducers. It may be an amplification system for active transducers. In both the applications, the transducer output is brought upto adequate level to make it useful for conversion, processing, indicating and recording.
3. **Multiplexer:** Multiplexing is the process of sharing a single channel with more than one input. Thus, a multiplexer accepts multiple analog inputs and connects them sequentially to one measuring instrument.
4. **Signal Converter:** A signal converter translates the analog signal to a form acceptable by the analog to digital (A/D) converter. An example of the signal converter is an amplifier for amplifying the low level signal voltages produced by transducers.

5. **Analog to Digital Converter (A/D converter):** An A/D converter converts the analog voltage to its equivalent digital form. The output of the A/D converter may be fed to digital display or may be fed to digital recorders for recording. It may be fed to a digital computer for data reduction and further processing.
6. **Auxiliary Equipment:** This contains devices for system programming functions and digital data processing. Some of the typical functions done by auxiliary equipment are linearization and limit comparison of signals. These functions may be performed by individual devices or by a digital computer.
7. **Digital Recorders and Digital Printers:** Records of information in digital form may be held on punched cards, perforated paper tapes, type written pages, floppy, discs, magnetic tape, or a combination of these systems. The digital printer provides a high quality hard copy for records, minimizing the operator's work.

Q.5 (b) Solution:

The resultant emfs at the junction temperature of θ_1, and reference junction temperature of $\theta_2 = 20°C$ are

At $\theta_1 = 900°C$, $E_1 = 8.446 - 0.112 = 8.334$ mV and

At $\theta_1 = 1200°C$, $E_2 = 11.946 - 0.112 = 11.834$ mV

With the same standardising current, the emfs are:

$$E_{ac} = \frac{1.08}{R_1 + 2.5 + R_2} \times R_1 = 8.334 \times 10^{-3} \quad ...(i)$$

and

$$E_{ad} = \frac{1.08}{R_1 + 2.5 + R_2} \times (R_1 + 2.5) = 11.834 \times 10^{-3} \quad ...(ii)$$

Dividing (ii) by (i), we have,

$$\frac{R_1 + 2.5}{R_1} = \frac{11.834}{8.334}$$

On solving we get, $R_1 = 5.95\ \Omega$

Substituting value of R_1 in (i), we get,

$$R_2 = 384.279\ \Omega$$

Q.5 (c) Solution:

We know that,

$$\text{Maximum stress, } S_m = \frac{3D^2 P}{16t^2}$$

where, D = Diameter of diaphragm = 10×10^{-3} m

P = Applied pressure = 350 kN/m^2

t = Thickness of the diaphragm

S_m = Maximum stress tolerance limit = 300×10^6 N/m^2

On substituting all the above values, we get

$$300 \times 10^6 = \frac{3 \times (10 \times 10^{-3})^2 \times 350 \times 10^3}{16t^2}$$

$$t = \sqrt{\frac{3 \times (10 \times 10^{-3})^2 \times 350 \times 10^3}{16 \times 300 \times 10^6}}$$

$$= 0.148 \times 10^{-3} \text{ m} = 0.148 \text{ mm}$$

Hence, for the diaphragm of thickness, t = 0.148 mm, maximum stress can't exceed 300 MN/m^2 limit.

Now, the deflection at the centre for a pressure of 175 kN/m^2 is given as

$$d_m = \frac{3PD^4(1-\gamma^2)}{256Et^3} \text{ N/m}^2$$

$$d_m = \frac{3 \times 175 \times 10^3 \times (10 \times 10^{-3})^4 (1 - 0.28^2)}{256 \times 195 \times 10^9 \times (0.148 \times 10^{-3})^3} = 0.03 \text{ mm}$$

The natural frequency is given by

$$\omega_n = \frac{20t}{D^2}\sqrt{\frac{E}{3\rho(1-\gamma^2)}} \text{ rad/sec}$$

$$\omega_n = \frac{20 \times 0.148 \times 10^{-3}}{(10 \times 10^{-3})^2}\sqrt{\frac{195 \times 10^9}{3 \times 7800 \times (1 - 0.28^2)}}$$

$$\omega_n = 89008.17 \text{ rad/sec}$$

$$f_n = 14.166 \text{ kHz}$$

Q.5 (d) Solution:

Maximum operating frequency (f_0) is inversely proportional to the gate delay (T_d).

$$f_0 \propto 1/T_d$$

where $T_d = R_{on}C_g$

Gate capacitance, $C_g = \frac{\varepsilon_{ox}}{t_{ox}}(\text{Gate area}) = C_{ox}(WL)$

Channel resistance, $R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)}$

So, $$T_d = \frac{L^2}{\mu(V_{GS} - V_T)}$$

Given that, μ is constant. When V_{DD} is scaled by $(1/\beta)$, $(V_{GS} - V_T)$ will be also scaled by $(1/\beta)$ and L will be scaled by $(1/\alpha)$.

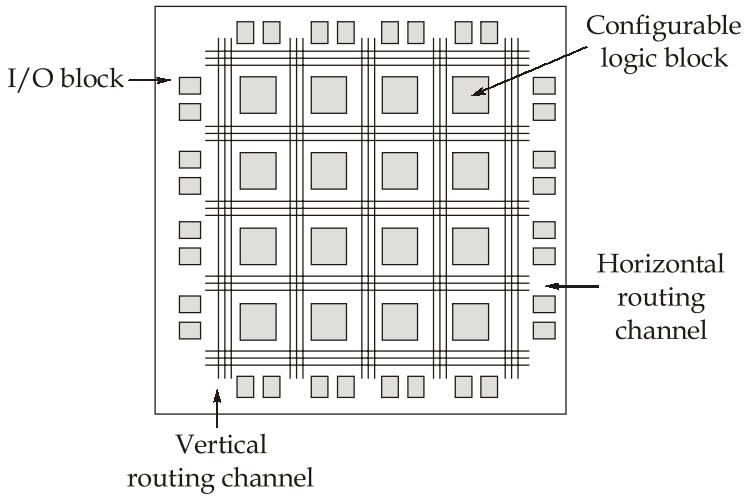
So, T_d will be scaled by $\frac{(1/\alpha)^2}{(1/\beta)} = \frac{\beta}{\alpha^2}$

Since, $f_0 \propto 1/T_d$, f_0 will be scaled by (α^2/β)

i.e., $$f_{0(\text{post-scaling})} = \frac{\alpha^2}{\beta} f_{0(\text{pre-scaling})}$$

Q.5 (e) Solution:

Field programmable gate array (FPGA) is a fully fabricated IC chip in which the interconnections can be programmed to implement different functions. An FPGA chip has thousands of logic gates which can be connected to implement any logic function. A typical FPGA architecture is shown below.



It has the following three main components:

- I/O buffers
- Array of configurable logic blocks (CLBs)
- Programmable interconnects

In the FPGA-based design, first a behavioural netlist is written to describe the functionality of the design. This is done using the hardware description languages such as Verilog or VHDL. Then the netlist is synthesized to come up with the gate level design. The next step is to map the logic blocks into available logic cells. This process is called the technology-mapping. This is followed by placement and routing, which

configures the CLBs and defines interconnections. The next step is to generate the bit-stream and download the bit-stream into an FPGA chip with the help of a software interface. Then the FPGA chip can function as desired as long as the power is ON, or it is reprogrammed.

Q.6 (a) Solution:

(i) Time taken for executing 50 instructions in pipelined manner = $n + k - 1$

$= 50 + 5 - 1 = 54$ clock cycles

Time taken for executing 50 instructions in non-pipelined fashion = $n \times k = 50 \times 5$

$= 250$ clock cycles

$$\text{Speed up} = \frac{T_{\text{Non-pipelined}}}{T_{\text{Pipelined}}} = \frac{(n \times k) \text{ clock cycles}}{(n + k - 1) \text{ clock cycles}}$$

$$= \frac{250}{54} = 4.62 \cong 5$$

$$\text{Throughput} = \frac{\text{Number of instructions executed}}{\text{Number of clock cycles taken}}$$

$$= \frac{50}{54} = 0.9259 \text{ instructions per cycle (IPC)}$$

Throughput is mentioned in terms of IPC (Instructions Per Cycle)

In a pipelined approach, maximum throughput achievable is 1. In real scenario, a throughput of 1 will never be achieved in a pipelined processor because of pipeline hazards.

(ii) Good design practices learnt through experiences are used as guidelines for ad-hoc DFT.

Some important guidelines are given below:

Things to be followed:

1. Large circuits should be partitioned into smaller sub circuits to reduce test costs. One of the most important steps in designing a testable chip is to first partition the chip in an appropriate way such that for each functional module there is an effective (DFT) technique to test it.

Partitioning must be done at every level of the design process, from architecture to circuit, whether testing is considered or not. Partitioning can be functional (according to functional module boundaries) or physical (based on circuit topology). Partitioning can be done by using multiplexers and/or scan chains.

2. Test access points must be inserted to enhance controllability and observability of the circuit. Test points include control points (CPs) and observation points (OPs). The CPs are active test points, while the OPs are passive ones. There are also test points, which are both CPs and OPs. Before exercising test through test points that are not PIs (Primary Inputs) and POs (Primary Outputs), one should investigate into additional requirements on the test points raised by the use of test equipments.
3. Circuits (flip flops) must be easily initializable to enhance predictability. A power on reset mechanism controllable from primary inputs is the most effective and widely used approach.
4. Test control must be provided for difficult-to-control signals.
5. Automatic Test Equipment (ATE) requirements such as pin limitation, tri stating, timing resolution, speed, memory depth, driving capability, analog/mixed signal support, internal/boundary scan support etc. should be considered during the design process to avoid delay of the project and unnecessary investment on the equipments.
6. Internal oscillations, PLLs and clock should be disabled during test. To guarantee tester synchronization, internal oscillators and clock generator circuitry should be isolated during the test of the functional circuitry. The internal oscillators and clocks should also be tested separately.
7. Analog and digital circuits should be kept physically separate. Analog circuit testing is very much different from digital circuit testing. Testing for analog circuits refers to real measurement, since analog signals are continuous (as opposed to discrete or logic signals in digital circuits). They require different test equipments and different test methodologies. Therefore, they should be tested separately.

Things to be avoided:

1. Asynchronous (unclocked) logic feedback in the circuit must be avoided. A feedback in the combinational logic can give rise to oscillation for certain inputs. Since, no clocking is employed, timing is continuous instead of discrete, which makes tester synchronization virtually impossible, and therefore only functional test by application board can be used.
2. Monostables and self resetting logic should be avoided. A monostable (one-shot) multivibrator produces a pulse of constant duration in response to the rising or falling transition of the trigger input. Its pulse duration is usually

controlled externally by a resistor and a capacitor (with current technology, they also can be integrated on chip). One shots are used mainly for

(i) pulse shaping (ii) switch on delays

(iii) switch off delays (iv) signal delays

Since it is not controlled by clocks, synchronization and precise duration control are very difficult, which in turn reduces testability by ATE. Counters and dividers are better candidates for delay control.

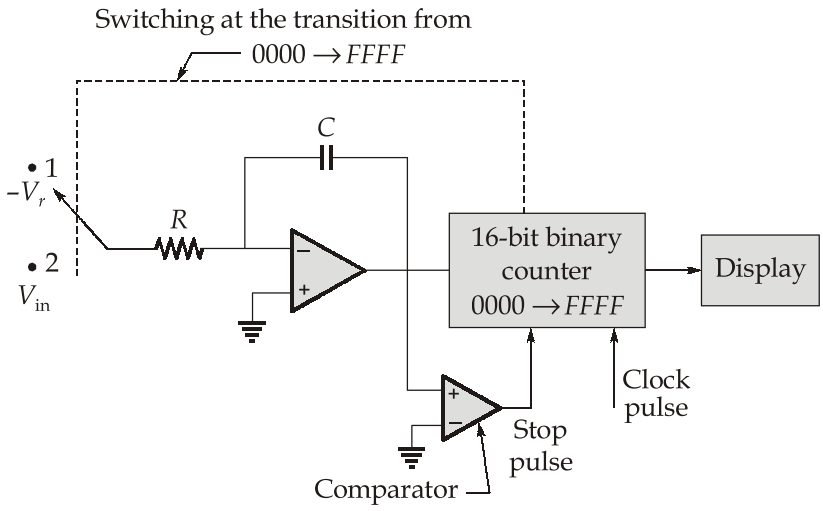
3. Redundant gates must be avoided.
4. High fan-in/fan-out combinations must be avoided as large fan-in makes the inputs of the gate difficult to observe and makes the gate output difficult to control.
5. Gated clocks should be avoided. These degrade the controllability of circuit nodes.

Infact, there are drawbakcs for Ad-hoc DFT methods:

1. There is a lack of experts and tools.
2. Test generation is often manual.
3. This method cannot guarantee for high fault coverage.
4. It may increase design iterations.
5. This is not suitable for large circuits.

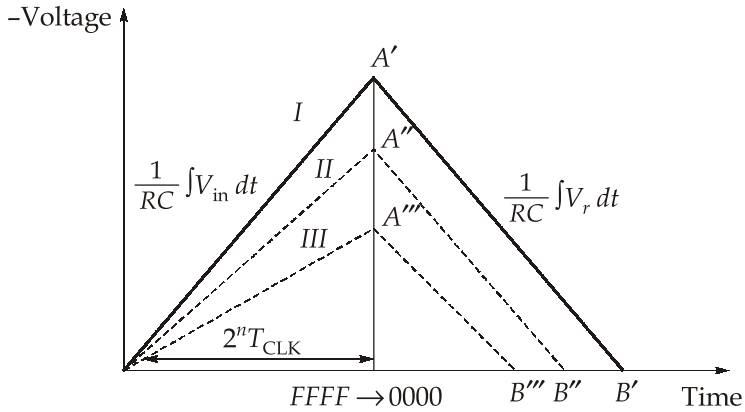
Q.6 (b) Solution:

(i) Dual slope converter: The circuit shown in figure is a dual slope converter.



Circuit diagram or dual slope converter

The binary counter is initially reset. To start conversion, the RC integrator starts integrating the input voltage V_{in}. The output of comparator is zero and the count value of the counter (assume a 16-bit DAC) starts increasing. The input voltage is integrated till the counter reaches FFFF H i.e. for 2^n clock cycles. As the count reaches $FFFF_H$ starting from 0000_H, on the next clock pulse, the counter is reset ($FFFF \rightarrow 0000$). For this particular change of count value from *FFFF* to 0000 , the switch is operated and negative reference voltage V_r is connected at the input of the integrator. As the integrator output reduces from the peak value attained, a stop pulse is generated as the integrator output reaches zero. This stop pulse stops the count of the Hexadecimal counter and triggers the display circuit. The counter count is latched and displayed. The slope of the curve for the first half when the count increases from 0000_H to $FFFF_H$ depends on $\frac{-1}{RC}\int V_{in}\,dt$ whereas the slope for the second half is $\frac{1}{RC}\int V_r\,dt$ i.e., depends on reference voltage. With the increase in input voltage V_{in}, the curve representing the output of integrator reaches at a higher level ($A' > A'' > A'''$) at the fixed time when the count increases from 0000_H – $FFFF_H$ and for the second half, all the negative going curve are of equal slope (As same reference voltage – V_r is connected at the input of the integrator) and thus A' reaches B', $A'' \rightarrow B''$, $A''' \rightarrow B'''$, where $B' > B'' > C'''$. Hence, the counts for higher input voltage is higher and corresponds to the input voltage.

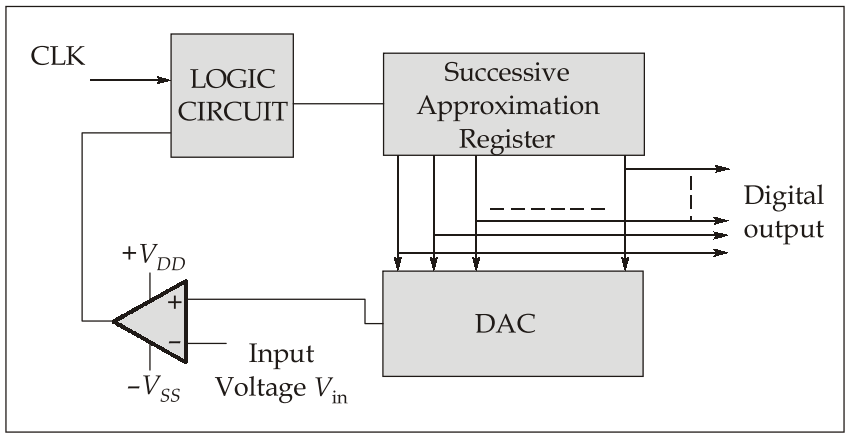


Last but not the least, very less noise corrupted voltage conversion is achieved through this type of converters. This is because the high frequency noise has been averaged out at the integrated output and the system noise has been reduced due to the counting in *two* phases:

1. 0000H — FFFH.
2. 0000H — Hex count value corresponding to V_{in}.

Successive approximation converter: The conversion time for the dual slope converter depends on the input voltage. Whereas, the conversion time of a successive approximation converter is fixed and does not depend on the input voltage.

The basic principle of successive approximation A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The n-bit value is stored in the successive approximation register (SAR) whose flip-flops are set or reset with the help of ring counter starting from MSB. At the start of the conversion, the MSB in the SAR is set and is converted to equivalent analog voltage. If it is less than the analog input voltage, the MSB is retained as 1 and the next bit is set to 1. Otherwise, the MSB is set to 0 and the next bit is set to 1. It is repeated till all the bits in the SAR are tried and the resulting value in the SAR gives the digital value corresponding to the input voltage.



Block Diagram for SAR ADC

For a n-bit SAR ADC, the conversion time will be n clock pulses irrespective of the input voltage. If the digital equivalent obtained in a 4-bit SAR ADC corresponding to the input voltage is 0101, the contents of the SAR changes as follows during the conversion:

$$0000 \rightarrow 1000 \rightarrow 0100 \rightarrow 0110 \rightarrow 0101$$

Q.6 (c) Solution:

(i) Linear approximation: We have,

Initial temperature, $\theta_1 = 110°C$; Final temperature, $\theta_2 = 130°C$

Mean temperature, $\theta_0 = 120°C$; Initial resistance, $R_{\theta_1} = 579.4\ \Omega$

Final resistance, $R_{\theta_2} = 591.7\ \Omega$; Mean resistance, $R_{\theta_0} = 585.7\ \Omega$

The linear approximation of resistance is given by

$$R_\theta = R_{\theta_0}[1 + \alpha_{\theta_0}(\theta - \theta_0)]$$

Given $\theta_0 = 120°C$. Using the values of resistance at 110° C and 130° C, the temperature coefficient can be obtained using above equation as below:

$$\alpha_{\theta_0} = \frac{1}{R_{\theta_0}} \times (\text{Slope at } \theta_0)$$

$$\alpha_{\theta_0} = \frac{1}{585.7} \times \frac{R_{\theta_2} - R_{\theta_1}}{\theta_2 - \theta_1} = \frac{1}{585.7} \times \frac{591.7 - 579.4}{130° - 110°}$$

$$\alpha_{\theta_0} = 1.05 \times 10^{-3}/°C$$

$\therefore$ The linear approximation of resistance is,

$$R_\theta = R_{\theta_0}\left[1 + \alpha_{\theta_0}(\theta - \theta_0)\right]\Omega$$

$$R_\theta = 585.7\left[1 + (1.05 \times 10^{-3})(\theta - 120)\right]\Omega$$

Quadratic approximation:

The resistance R_θ at any temperature θ°C is given by

$$R_\theta = R_{\theta_0}\left[1 + \alpha_1 \Delta\theta + \alpha_2 (\Delta\theta)^2\right]$$

We can find the quadratic terms, by forming two equations using two points about the mean temperature $\theta_0 = 120°C$

We have, $R_{\theta_0} = 585.7\ \Omega$ at $\theta_0 = 120°C$

Now using 110°C and 130°C as two points, we have

$$579.4 = 585.7\left[1 + \alpha_1(110° - 120°) + \alpha_2(110° - 120°)^2\right] \quad ...(i)$$

$$591.7 = 585.7\left[1 + \alpha_1(130° - 120°) + \alpha_2(130° - 120°)^2\right] \quad ...(ii)$$

From equation (i), we get,

$$-10\alpha_1 + 100\alpha_2 = -0.0108 \quad ...(iii)$$

Similarly from equation (ii), we get,

$$10\alpha_1 + 100\alpha_2 = 0.0102 \quad ...(iv)$$

On solving equations (iii) and (iv), we get,

$$\alpha_1 = 1.05 \times 10^{-3}/°C \quad \text{and} \quad \alpha_2 = -3 \times 10^{-6}/(°C)^2$$

Hence, $R_\theta = 585.7\left[1 + (1.05 \times 10^{-3})(\theta - 120°) + (-3 \times 10^{-6})(\theta - 120°)^2\right]$

(ii) The Steinhart and Hart equation provides an empirical expression for resistance temperature relationship of NTC thermistor and NTC probe assemblies.

The most common equation is

$$T = \frac{1}{A + B\ln(R) + C[\ln(R)]^3}$$

where:

'T' is in degrees Kelvin and 'A', 'B' and 'C' are coefficients derived as follows:

First, measure the thermistor resistance at three different temperatures. The temperature should be evenly spaced and at least 10 degree apart. Use the three temperatures to solve three simultaneous equations:

$$\frac{1}{T_1} = A + B\ln(R_1) + C[\ln(R_1)]^3$$

$$\frac{1}{T_2} = A + B\ln(R_2) + C[\ln(R_2)]^3$$

$$\frac{1}{T_3} = A + B\ln(R_3) + C[\ln(R_3)]^3$$

Knowing A, B and C for a thermistor allow to determine the resistance-temperature relationship using Steinhart and Hart equation.

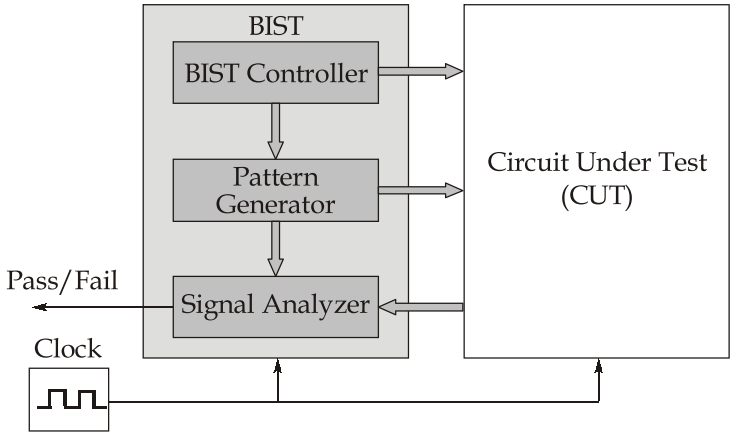
Q.7 (a) Solution:

(i) Traditional techniques that use automatic test pattern generation software to target single faults for digital circuit testing have become quite expensive and no longer provide sufficiently high fault coverage. One approach to be alleviate these testing problems is to incorporate built in self testing features into a digital circuit at the design stage. With logic BiST, circuits that generate test patterns and analyze the output response of the functional circuitry are embedded in the chip or else where in the same board where the chip resides.

There are two general categories of BiST techniques for testing random logic:

1. Online BiST is performed when the functional circuitry is in normal operational mode. It can be done either concurrently or non-concurrently.
2. Offline BiST is performed when the functional circuitry is not in normal mode. This technique does not detect any real time errors but widely used in the industry for testing the functional circuitry to ensure product quality.

The figure below shows BiST architecture. In BiST, a test pattern generator generates test patterns and a signal analyzer (SA) compares test responses. The entire process is controlled by BIST controller.



Advantages:

1. Lower cost of test, since it reduces or eliminates the need for external electrical testing using an automatic test equipment.
2. Better fault coverage.
3. Shorter test time.
4. Support of concurrent testing.

Disadvantages:

1. Additional silicon area requirement.
2. Reduced access time.
3. Additional pin requirement if the BiST can be designed to test more structures in parallel.
4. Possible issues with the correctness of BiST result, since the on-chip testing hardware itself can fail.

(ii) **Controllability:** This is the ability to control the signal value at a node using only the input pins. A node is controllable if we are able to drive a value of 0 and 1 onto that node using primary inputs.

Observability: It is the ability of propagating a signal value at a node to one of output pins of the circuit, so that it can be observed. A node is called observable if the signal value at the node can be propagated to one of the primary outputs.

Fault coverage: It is defined as the number of faults detected divided by the number of potential faults. Typically, for digital circuit, the number refers to stuck at equivalent faults, and for analog, the number refers to shorts and opens.

$$\text{Fault coverage} = \frac{\text{Number of detected faults}}{\text{Total number of faults}} \times 100\%$$

Let us consider the simple circuit shown below consisting of four simple logic gates. To detect any defect on line 8, the primary input A and B must be set to logic 1. However, such a setting forces line 7 to logic 1. Thus, any stuck at (s-a-1) fault on line 7 cannot be tested at the primary output, although in the absence of such a fault, the logic value on line 7 can be fully controllable through primary inputs B, C and D. Hence, the logic value on line 7 is controllable but not observable. Therefore, this circuit is not fully testable. The main cause of this difficulty in this circuit is the fact that input B fans out to lines 5 and 6, and then after the OR gate, both line signals are combined in the AND gate. Such a fanout is called reconvergent fanout.

Reconvergent fanouts make the testing of the circuit much more difficult

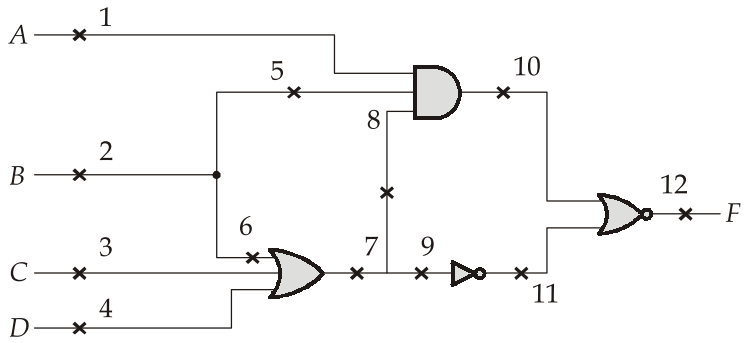


Figure: A simple circuit consisting of four gates with four primary inputs and one primary output.

If a large number of input vectors are required to set a particular node value to 1 or 0 (fault excitation) and to propagate an error at the node to an output (fault effect propagation), then the testability is low. The circuits with poor controllability include those with feedbacks, decoders and clock generators. The circuits with poor observability include sequential circuits with long feedback loops and circuits with reconvergent fanouts, redundant nodes, and embedded memories such as RAM, ROM and PLA.

Q.7 (b) Solution:

(i) We know that, EMF, $E = i[R_m + R_s + R_e]$

where, R_m = Resistance of meter coil = 50 Ω

R_e = Resistance of junction and leads = 12 Ω

R_s = Resistance of series resistor

i = Full scale deflection current = 0.2 mA

At 700°C, EMF = 25 mV. To achieve full scale deflection at 700°C,

$$25 \times 10^{-3} = 0.2 \times 10^{-3} [50 + 12 + R_s]$$

$$R_s = 63\ \Omega$$

(ii) Current in the circuit with increased resistance

$$i = \frac{E}{R_m + R_s + R'_e} = \frac{25 \times 10^{-3}}{50 + 63 + R'_e}$$

where, $R'_e = R_e + 1 = 12 + 1 = 13\ \Omega$

$$i = \frac{25 \times 10^{-3}}{50 + 63 + 13} = 0.198\ \text{mA}$$

$\therefore$ Approximate error in temperature $= \dfrac{(0.198 \times 10^{-3}) - (0.2 \times 10^{-3})}{0.2 \times 10^{-3}} \times 700 = -7°\text{C}$

(iii) Change in resistance of coil with a temperature increase of 10°C = 50 × 0.0043 × 10
= 2.15 Ω

Current in the circuit with increased resistance of coil

$$= \frac{25 \times 10^{-3}}{50 + 2.15 + 63 + 12} = 0.197\ \text{mA}$$

$\therefore$ Approximate error in temperature $= \dfrac{0.197 \times 10^{-3} - 0.2 \times 10^{-3}}{0.2 \times 10^{-3}} \times 700 = -10.5°\text{C}$

Q.7 (c) Solution:

- **Resistance-temperature characteristics of thermistor :**

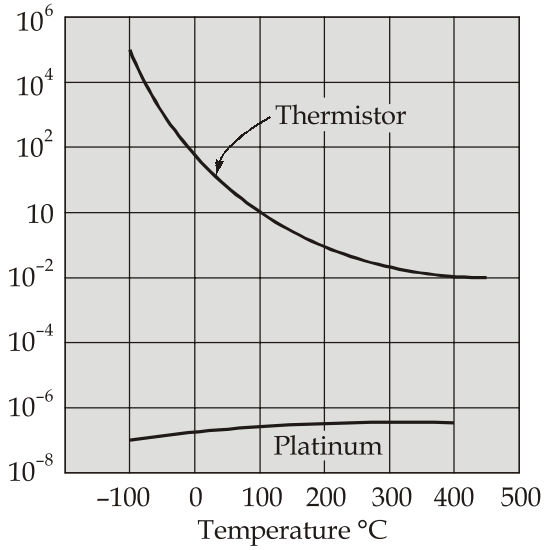
The mathematical expression for the relationship between the resistance of a thermistor and absolute temperature of thermistor is:

$$R_{T1} = R_{T2} \exp\left[\beta\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

where R_{T1} = Resistance of the thermistor at absolute temperature T_1; °K,
R_{T2} = Resistance of the thermistor at absolute temperature T_2; °K,
and β = A constant depending upon the material of thermistor, typically 3500 to 4500 °K

The resistance temperature characteristics of a typical thermistor are given in figure below. It shows that a thermistor has a very high negative temperature coefficient of resistance, making it an ideal **temperature transducer**. Figure also shows the resistance temperature characteristics of platinum which is a commonly used material for resistance thermometers. Let us compare the characteristics of the two materials. Between - 100°C and 400°C, the thermistor changes its resistivity from 10^5 to 10^{-2} a factor of 10^7, while platinum changes its resistivity by a factor of about

10 within the same temperature range. This explains the high sensitivity of thermistors for measurement of temperature.



Resistance-temperature characteristics of a typical thermistor and platiinum

The characteristics of thermistors are no doubt non-linear but a linear approximation of the resistance-temperature curve can be obtained over a small range of temperature. Thus, for a limited range of temperature, the resistance of a thermistor varies as given by equation

$$R_\theta = R_{\theta_0}\left[1 + \alpha_{\theta_0}\Delta\theta\right]$$

A thermistor exhibits a negative resistance temperature coefficient which is typically about 0.05/°C.

An individual thermistor curve can be closely approximated through the **Steinhart-Hart equation**:

$$\frac{1}{T} = A + B\log_e R + C(\log_e R)^3$$

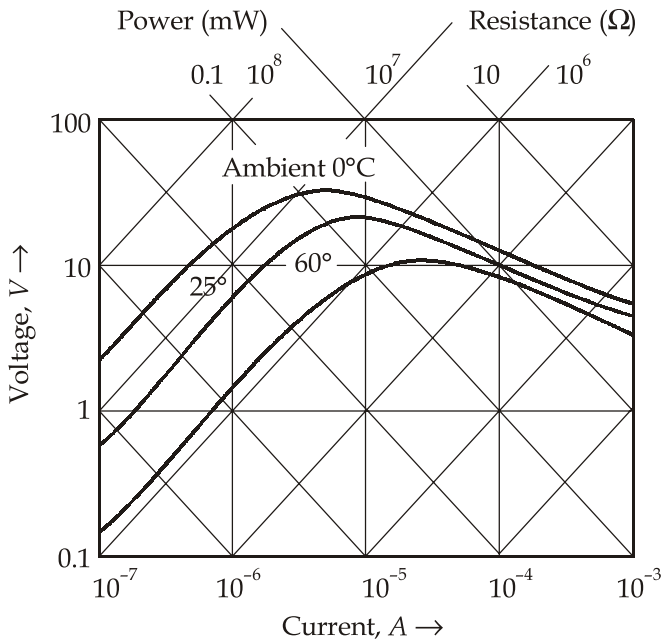
where, T = temperature ; ° K, R = Resistance of thermistor ; Ω

and A, B, C = curve fitting constants

- **Voltage-current characteristics :** These characteristics are shown in figure below. It shows that the voltage drop across a thermistor increases with increasing current until is reaches a peak value beyond which the voltage drop decreases as the current increases. In this portion of the curve, the thermistor exhibits a negative resistance characteristic. If a very small voltage is applied to the thermistor, the resulting

small current does not produce sufficient heat to raise the temperature of the thermistor above ambient. Under this condition, Ohm's law is followed and the current is proportional to the applied voltage. Larger currents, at larger applied voltages, produce enough heat to raise the thermistor temperature above the ambient temperature and its resistance then decreases. As a result, more current is then drawn and the resistance decreases further. The current continues to increase until the heat dissipation of the thermistor equals the power supplied to it. Therefore, under any fixed ambient conditions, the resistance of a thermistor is largely a function of the power being dissipated within itself, provided that there is enough power available to raise its temperature above ambient. Under such operating conditions, the temperature of the thermistor may rise 100°C or 200°C and its resistance may drop to one-thousandth of its value at low current.

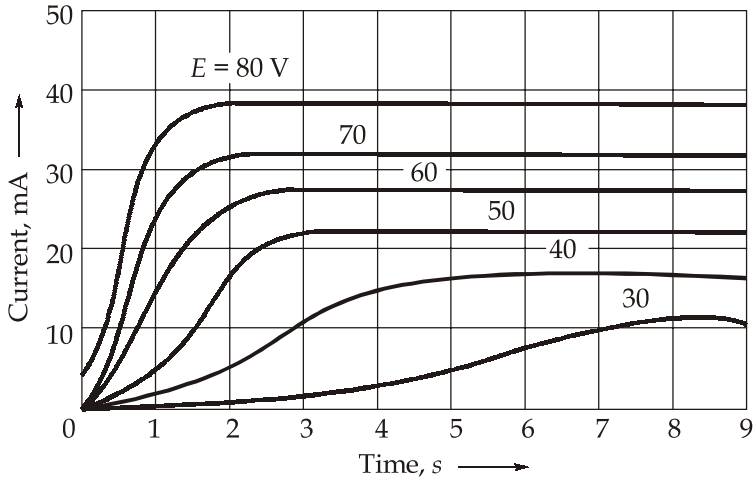
This characteristic of self-heat provides an entirely new field of uses for the thermistor. In the self-heat state, the thermistor is sensitive to anything that changes the rate at which heat is conduced away from it. It can so be used to measure flow, pressure, liquid level, composition of gases, etc. If, on the other hand, the rate of heat removal is fixed, then the thermistor is sensitive to power input and can be used for voltage or power-level control.



Voltage-current characteristics of thermistors

- **Current-time characteristics :** The current-time characteristics shown in figure below indicate the time delay to reach maximum current as a function of the applied

voltage. When the heating effect just described occurs in a thermistor network, a certain finite time is required for the thermistor to heat and the current to build up to a maximum steady-state value. This time, although fixed for a given set of circuit parameters, may easily be varied by changing the applied voltage or the series resistance of the circuit. This time-current effect provides a simple and accurate means of achieving time delays from milliseconds to many minutes.



Current-time characteristics of thermistors

Q.8 (a) Solution:

(i) Advantages of Pipelining:

1. The cycle time of the processor is reduced, increasing the instruction throughput. Pipelining does not reduce the time it takes to complete an instruction, instead it increases the number of instructions that can be processed simultaneously ("at once") and reduces the delay between completed instructions (called throughput).
2. If pipelining is used, the CPU arithmetic logic unit can be designed faster, but will be more complex.
3. Pipelining in theory increases performance over an unpipelined core by a factor of the number of stages and the code is ideal for pipeline execution.
4. Pipelined CPU's generally work at a higher clock frequency than the RAM clock frequency increasing computer's overall performance.

Disadvantages of Pipelining: Pipelining has many disadvantages through there are lot of techniques used by CPU's and compilers designers to overcome most of them; the following is a list of common drawbacks:

1. The design of a non-pipelined processor is simpler and cheaper to manufacture, non-pipelined processor executes only a single instruction at a time. This

prevents branch delays (in pipelining, every branch is delayed) as well as problems when serial instructions being executed concurrently.

2. In pipelined processor, insertion of flip flops between modules increases the instruction latency compared to a non-pipelined processor.
3. A non-pipelined processor will have a defined instruction throughput. The performance of a pipelined processor is much harder to predict and may vary widely for different programs.
4. When a programmer writes assembly code, they generally assume that each instruction is executed before the next instruction is being executed. When this assumption is not validated by pipelining, it causes a program to behave incorrectly, this situation is known as hazard.
5. Self modifying programs may fail to execute properly on a pipelined architecture when the instructions being modified are near the instructions being executed. This can be caused by the instruction may already being in the prefetch Input Queue, so the modification may not take effect for the upcoming execution of instructions. Instruction caches make the problem even worse.

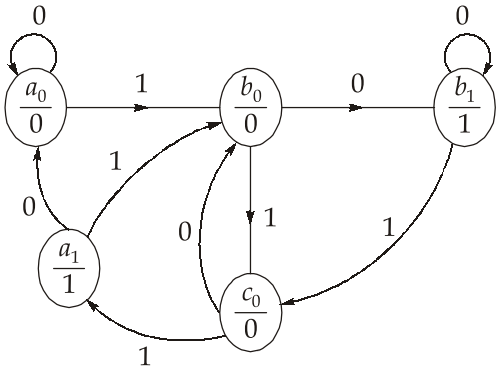
Difference between linear and non-linear pipline:

Sl. No.	Linear Pipeline	Non-linear pipeline
1.	Linear pipeline are static pipeline because they are used to perform fixed functions.	Non-linear pipeline are dynamic pipeline because they can be reconfigured to perform variable functions at different times.
2.	Linear pipeline allows only streamline connections.	Non-linear pipeline allows feed forward and feedback connections in addition to the streamline connection
3.	It is relatively easy to partition a given function into a sequence of linearly ordered sub functions.	Functional partitioning is relatively difficult because the pipeline stages are interconnected with loops in addition to streamline connections.
4.	The output of the pipeline is produced from the last stage.	The output of the pipeline is not necessarily produced from the last stage.
5.	The reservation table is trivial in the sense that data flows in linear streamline.	The reservation table is non-trivial in the sense that there is non linear streamline for data flows.
6.	Static pipelining is specified by single reservation table.	Dynamic pipelining is specified by more than one reservation table.
7.	All initiations to a static pipeline use the same reservation table.	A dynamic pipeline may allow different initiations to follow a mix of reservation tables.

(ii) The state table for the given Mealy circuit is as below:

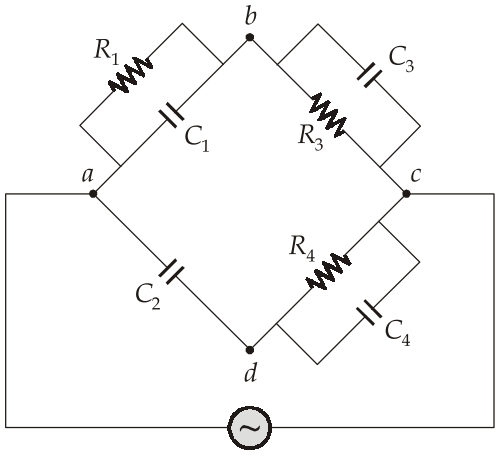
Present State	Input		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	a	b	0	0
b	b	c	1	0
c	b	a	0	1

The output of the Moore machine is solely determined by its current state. Hence, the Moore circuit for above Mealy circuit can be drawn as below,



Q.8 (b) Solution:

From the above given description, we can draw circuit as



For balance, $Y_1\, Y_4 = Y_2\, Y_3$

or $$\left(\frac{1}{R_1} + j\omega C_1\right)\left(\frac{1}{R_4} + j\omega C_4\right) = (j\omega C_2)\left(\frac{1}{R_3} + j\omega C_3\right)$$

$$\frac{1}{R_1 R_4} + \frac{j\omega C_4}{R_1} + \frac{j\omega C_1}{R_4} - \omega^2 C_1 C_4 = \frac{j\omega C_2}{R_3} - \omega^2 C_2 C_3$$

$$\left[\frac{1}{R_1 R_4} - \omega^2 C_1 C_4\right] + j\left[\frac{\omega C_4}{R_1} + \frac{\omega C_1}{R_4}\right] = -\omega^2 C_2 C_3 + \frac{j\omega C_2}{R_3}$$

Equating the real and imaginary parts, we get,

$$\frac{1}{R_1 R_4} - \omega^2 C_1 C_4 = -\omega^2 C_2 C_3 \quad \text{...(ii)}$$

and

$$\frac{\omega C_4}{R_1} + \frac{\omega C_1}{R_4} = \frac{\omega C_2}{R_3}$$

$$\frac{\omega C_4}{R_1} = \frac{\omega C_2}{R_3} - \frac{\omega C_1}{R_4}$$

$$\frac{\omega C_4}{\frac{\omega C_2}{R_3} - \frac{\omega C_1}{R_4}} = R_1$$

$$R_1 = \frac{C_4}{\frac{C_2}{R_3} - \frac{C_1}{R_4}} \quad \text{...(i)}$$

Substitute R_1 in equation (ii), we get,

$$\frac{1}{\left(\frac{C_4 R_4}{\frac{C_2}{R_3} - \frac{C_1}{R_4}}\right)} - \omega^2 C_1 C_4 = -\omega^2 C_2 C_3$$

$$\frac{1}{\frac{C_4 R_4^2 R_3}{C_2 R_4 - C_1 R_3}} - \omega^2 C_1 C_4 = -\omega^2 C_2 C_3$$

$$\frac{C_2 R_4 - C_1 R_3}{C_4 R_4^2 R_3} - \omega^2 C_1 C_4 = -\omega^2 C_2 C_3$$

$$\frac{C_2 R_4}{C_4 R_4^2 R_3} - \frac{C_1 R_3}{C_4 R_4^2 R_3} - \omega^2 C_1 C_4 = -\omega^2 C_2 C_3$$

$$\frac{-C_1 R_3}{C_4 R_4^2 R_3} - \omega^2 C_1 C_4 = -\omega^2 C_2 C_3 - \frac{C_2 R_4}{C_4 R_4^2 R_3}$$

$$C_1\left[\frac{R_3}{C_4 R_4^2 R_3} + \omega^2 C_4\right] = \frac{\omega^2 C_2 C_3 C_4 R_4^2 R_3 + C_2 R_4}{C_4 R_4^2 R_3}$$

$$C_1\left[R_3 + \omega^2 C_4^2 R_4^2 R_3\right] = \omega^2 C_2 C_3 C_4 R_4^2 R_3 + C_2 R_4$$

$$C_1 = \frac{\omega^2 C_2 C_3 C_4 R_4^2 R_3 + C_2 R_4}{R_3 + \omega^2 C_4^2 R_4^2 R_3}$$

$$C_1 = \frac{\omega^2 C_2 C_3 C_4 R_4^2 + \dfrac{C_2 R_4}{R_3}}{1 + \omega^2 C_4^2 R_4^2}$$

Now, $\omega^2 C_2 C_3 C_4 R_4^2 << \dfrac{C_2 R_4}{R_3}$

and $\omega^2 C_4^2 R_4^2 << 1$

Hence, we can write, $C_1 = C_2 \dfrac{R_4}{R_3}$

When the capacitor C_1 is without specimen dielectric, let its capacitance be C_0.

$\therefore$ $C_0 = C_2 \dfrac{R_4}{R_3} = 150 \times 10^{-12} \times \dfrac{8 \times 10^3}{8 \times 10^3}$

$C_0 = 150$ pF

When the specimen is inserted as dielectric, let the capacitance be C_s.

$$C_s = C_2 \frac{R_4}{R_3} = 750 \times \frac{8000}{8000} = 750 \text{ pF}$$

Now, $C_0 = \dfrac{\epsilon_o A}{d}$ and $C_s = \dfrac{\epsilon_r \epsilon_o A}{d}$

Hence, relative permittivity of specimen,

$$\epsilon_r = \frac{C_s}{C_0} = \frac{750}{150} = 5$$

Q.8 (c) Solution:

(i) 1. Pipelining to 5 stages reduces the cycle time to the length of the longest stage. Additionally, the cycle time needs to be slightly longer to accomodate the buffer delay. Hence,

Cycle time = Highest stage latency + Buffer delay
= 550 + 20 = 570 ps

2. The latency for the instruction is 5 * (cycle time), since an instruction needs to go through 5 pipeline stages, spending 1 cycle in each. Hence,

Latency = Cycle time × Number of stages
= 570 × 5 = 2850 ps

(ii) **Branch Fault:** This fault is modeled at the behavioral level where the circuit function is described in a programming language. A branch fault affects a branch statement and causes it to branch to an incorrect destination.

Bus Fault: A bus fault specifies the status for each line in a bus as stuck-at-0, stuck-at-1, or fault free. Thus, for an n-bit bus, there are $3^n - 1$ bus faults. A total bus fault assumes all lines of the bus to be stuck at the same 0 or 1 state.

Defect Oriented Faults: Faults at the physical level that usually occur during manufacture are called defects. The electrical or logic level faults that can be produced by physical defects are classified as defect oriented faults. Examples of physical defects are broken (open) wires, bridges, improper semiconductor doping, and improperly formed devices. Some defect oriented fault models are bridging faults, stuck open faults, and increased I_{DDQ} faults. PLA and some analog fault models are also classified as defect oriented faults.

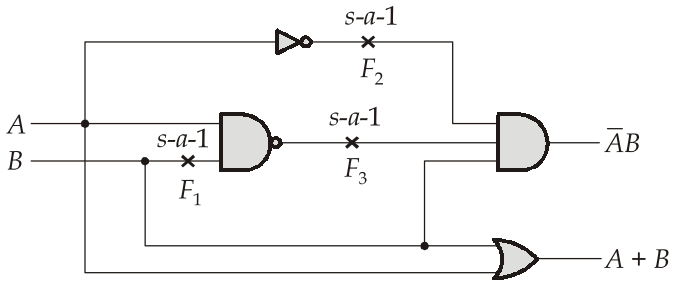
Line Delay Fault: This fault models rising and falling delays of a given signal line. In contrast with the transition fault where the transition can be propagated through any path, a test for a line delay fault must propagate the transmission through the longest sensitizable path. A single fault assumption limits the number of faults to twice the number of lines. Test can detect all spot defects and many (not all) distributed delay defects.

Logical Faults: These faults affect the state of logic signals. Normally, the state may be modeled as {0, 1, X(unknown), z(high impedance)}, and a fault can transform the correct value to any other value. Several types of faults can be modeled at the logic level. However, the term logical faults often implies stuck at faults.

Stuck at Fault: This fault is modeled by assigning a fixed (0 or 1) value to a single line in the circuit. A signal line is an input or an output of a logic gate or a flip-flop. The most popular forms are the single stuck at faults i.e. two faults per line, stuck-at-1 (s-a-1 or $sa1$) and stuck at 0 (s-a-0 or $sa0$).

Multiple Fault: A multiple fault represents a condition caused by the simultaneous presence of a group of single faults. Frequently considered multiple faults consist of same type of single faults. For example, multiple stuck at faults, or multiple testable path delay faults.

Example of multiple stuck at faults:



Multiple stuck at fault	Output at $\bar{A}B$	Test
F_1, F_2	$\bar{A}B$	Redundant
F_1, F_3	$\bar{A}B$	Redundant
F_2, F_3	B	11
F_1, F_2, F_3	B	11

Initialization Fault: Circuits with memory elements (eg. flip-flops) are designed so that they can be initialized by applying suitable input signals. Faults that interfere with such an initialization procedure are called initialization faults. A typical example of such a fault is the clock line of a flip-flop being stuck in the inactive state.

Delay Fault: These faults cause the combinational delay of a circuit to exceed the clock period. Specific delay faults are transition faults, gate-delay-faults, line-delay faults, segment-delay faults and path-delay faults.

Intermittent Fault: A fault that appears and disappears as a function of time is called an intermittent fault. A fracture in an interconnect may produce an intermittent open for some time before it becomes a permanent fault. Intermittent faults can be of any type eg. stuck-at fault or a bridging fault with its presence in time described probabilistically.

Redundant Fault: Any fault that does not modify the input-output function of the circuit is called a redundant fault. A redundnant fault cannot be detected by any test.

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