S.No. : 01 LS1_EC_D_080919

Microprocessor

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CLASS TEST 2019-2020

ELECTRONICS ENGINEERING

Date of Test : 08/09/2019

ANSWER KEY ➤ Microprocessor

1.	(d)	7.	(b)	13.	(c)	19.	(d)	25.	(b)
2.	(d)	8.	(d)	14.	(d)	20.	(d)	26.	(b)
3.	(b)	9.	(a)	15.	(c)	21.	(a)	27.	(d)
4.	(b)	10.	(a)	16.	(d)	22.	(b)	28.	(c)
5.	(d)	11.	(d)	17.	(c)	23.	(c)	29.	(c)
6.	(a)	12.	(b)	18.	(b)	24.	(d)	30.	(b)

Detailed Explanations

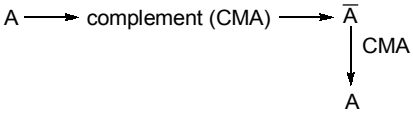
1. (d)

$$\begin{array}{r} 8C\ H \\ +\ 7E\ H \\ \hline 1\ 0A\ H \end{array}$$

$$CY = 1$$
$$(A) = 0A\ H$$

3. (b)

CMA instruction complements the contents of accumulator



$$\overline{A} = 10100101$$
$$A = 01011010 = 5A\ H$$

6. (a)

MVI A, 82 H : (A) ← 82 H

XRA A :

$$\begin{array}{r} 1000\ 0010 \\ 1000\ 0010 \\ \hline 0000\ 0000 \end{array} \quad (A) \leftarrow 00\ H$$

JP DISPLAY : Jump if positive ⇒ as sign flag = 0 after XRA A, condition for Jump is satisfied (Port 1) ← (A) ⇒ (Port 1) = 00 H.

8. (d)

$$\text{Total number of input lines} = 16 = n$$
$$\text{Total number output lines} = 16 = m$$
$$\text{ROM size} = 2^n \times m = 2^{16} \times 16$$
$$= 64\ k \times 16$$

9. (a)

When ALE goes high data bus is used as address bus when it goes low it is used as data bus only.

10. (a)

The above instructions are used to multiply the contents of Register B by '2'.

11. (d)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
(a)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
(b)	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1
(c)	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0
	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1
(d)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1

For the address range to be represented by chip 1 and chip 2, A_9 A_8 should be either 01 or 10, here in option (d) A_9 A_8 is 00. So, this circuit can't address the range F800 H - F9FF H.

12. (b)

[PC]

0700 H LXI SP, 00FF H : contents of 0701 H = FF H, contents of 0702 H = 00 H

0703 H LXI H, 0701 H

0706 H MVI A, 20 H

0708 H SUB M

[PC] → 0709 H

When [PC] → 0709 H; contents of memory location 0701 H subtracted from accumulator.

i.e. 20 H – FF H = 21 H

13. (c)

05 H AND 80 H = 00 H

After ANI instruction, CY = reset, AC is set and S, Z, P are modified.

S = 0, Z = 1, AC = 1, P = 1, CY = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	X	1	X	1	X	0
S	Z	X	AC	X	P	X	CY

14. (d)

(i) DAD R_P doesn't affect any flag except CY

(ii) PCHL copies the content of HL pair to the program counter

(iii) All have fetch of 6 T-states except XTHL which has fetch of 4T states

(iv) In INR R, all flags are affected except CY flag

15. (c)

After the execution of RET instruction the top two bytes of stacks are transferred to program counter.

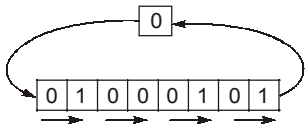
17. (c)

MVI A, 45 H ⇒ A : 45 H

MOV B, A ⇒ B : 45 H

STC ⇒ CY = 1

CMC ⇒ CY = 0

RAR = 

(Rotate Accumulator Right with carry)

A : 0 0 1 0 0 0 1 0

B : 0 1 0 0 0 1 0 1

A XOR B : 0 1 1 0 0 1 1 1

6 7

A : 67 H

18. (b)

The above program is used to multiply the contents of Accumulator by $(10)_{10}$.

$10(A_{initial})$ = 46 H = $(70)_{10}$

(BYTE 1) = $(A_{initial})$ = 07 H

19. (d)

starting address = 1001 H
ending address = 2016 H
size of memory = (2016 – 1001) H + 1 H
= 1016 H = 4118 bytes

20. (d)

LXI H, 3000 H	HL : 3000 H
MOV E, M	E : 02 H
INX H	HL : 3001 H
MOV D, M	D : 30 H
LDAX D	A : 00 H
MOV L, A	L : 00 H
INX D	DE : 3003 H
LDAX D	A : 30 H
MOV H, A	H : 30 H

After execution of the program contents of H = 30 H.

21. (a)

Moving reverse in the program given
Assuming contents at 2000 H as XX H

LDA 2000 H : (A) = XX H
CMA : (A) = FF H – XX H
ADI 01 H : (A) = FF H – XX H + 01 H
STA 2100 H : (A) = FF H – XX H + 01 H → (2100) H
FF H – XX H + 01 H = 89 H
XX H = FF H – 89 H + 01 H
= 77 H

22. (b)

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

8000 H - 87FF H

25. (b)

RAM chip size = 1 k × 8 (1024 words of 8 bits each)
RAM to be constructed = 16 k × 16

$$\text{Number of chips required} = \frac{16\,k \times 16}{1k \times 8} = 16 \times 2$$

16 chips vertically, each having 2 chips horizontally required.
so, to select 16 chips vertically, we need 4 × 16 decoder, but available one is 2 × 4 decoder.
to construct a 4 × 16 decoder using 2 × 4 decoder,

$$\left(\frac{16}{4} = 4\right) + \left(\frac{4}{4} = 1\right) = \text{“5” } 2 \times 4 \text{ decoders are required.}$$

26. (b)

$18\,H = (24)_{10}$

DELAY : MVI D, 18 H ⇒ 1 time ⇒ 7 T

LOOP : DCR D ⇒ 24 times ⇒ 24 (4 T)

JNZ LOOP ⇒ 23 times true + 1 time false ⇒ 23 (10 T) + (7 T)

RET ⇒ 1 time ⇒ 10 T

total delay = (7 + 96 + 237 + 10) T - states

= 350 T - states

$$\text{one T - state} = \frac{1}{f_{clock}} = \frac{1}{5}\mu s$$

$$\text{total delay} = \frac{350}{5}\mu s = 70\,\mu s$$

27. (d)

Initialization :

(3000 H) = 03 H

(B) = 03 H

(C) = 03 H

(A) = 00 H

LOOP :

(A) = (A) + (B) + (B) + (B)

∵ ADD B instruction will be executed for 3 times

(A) = 00 H + 3(03 H) = 09 H

$(09\,H) = (09)_{10}$

28. (c)

LHLD 3000 H : Load HL Pair will
(L) ← (3000 H)
(H) ← (3001 H)

XCHG : Exchange HL with DE pair

LHLD 3002 H : (L) ← (3002 H)
(H) ← (3003 H)

DAD D : Add DE pair with HL pair

SHLD 3004 H : Store result in address location 3004 H
(3004 H) ← (L)
(3005 H) ← (H)

Before Execution
3000 H : 12 H
3001 H : 04 H
3002 H : 04 H
3003 H : 03 H

0412 H + 0304 H = 0716 H

After Execution
3004 H : 16 H
3005 H : 07 H

contents of memory location 3004 H = 16 H.

29. (c)

MVI B, 00 H : (B) ← 00 H
MVI A, 1C H : (A) ← 1C H
DCR B : (B) ← (B) – 1 = FF H
DAA : Adjust the accumulator to BCD values

(A) = 1C H

```
  0 0 0 1   1 1 0 0
+           0 1 1 0
-----------------------
  0 0 1 0   0 0 1 0
-----------------------
```

Hence (A) : 22 H
Contents of 3000 H is 22 H
$22\ H = (16 \times 2 + 2)_{10} = (34)_{10}$.

30. (b)

The above program displays the absolute value of DATA 1. If DATA 1 is negative, it determines it's 2's complement and displays at PORT 1.

(A) = 87 H = $(10000111)_2$

MSB is 1, so sign flag S = 1 after ORA A and condition for JM DSPLY is satisfied.

so, (PORT 1) = 2's complement of $(10000111)_2$
= $(01111000)_2 + (1)_2$
= $(01111001)_2 = (79)_{16}$ or 79H

■■■■