CLASS TEST

Sl.: 01-CS-CO-09082023

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COMPUTER SCIENCE & IT

Computer Organization

Duration : 1:00 hr. **Maximum Marks : 50**

Read the following instructions carefully

1. This question paper contains **30** objective questions. **Q.1-10** carry one mark each and **Q.11-30** carry two marks each.
2. Answer all the questions.
3. Questions must be answered on Objective Response Sheet (**ORS**) by darkening the appropriate bubble (marked **A**, **B**, **C**, **D**) using HB pencil against the question number. Each question has only one correct answer. In case you wish to change an answer, erase the old answer completely using a good soft eraser.
4. There will be **NEGATIVE** marking. For each wrong answer **1/3rd** of the full marks of the question will be deducted. More than one answer marked against a question will be deemed as an incorrect response and will be negatively marked.
5. Write your name & Roll No. at the specified locations on the right half of the **ORS**.
6. No charts or tables will be provided in the examination hall.
7. Choose the **Closest** numerical answer among the choices given.
8. If a candidate gives more than one answer, it will be treated as a **wrong answer** even if one of the given answers happens to be correct and there will be same penalty as above to that questions.
9. If a question is left blank, i.e., no answer is given by the candidate, there will be **no penalty** for that question.

DO NOT OPEN THIS TEST BOOKLET UNTIL YOU ARE ASKED TO DO SO

Q.No. 1 to Q.No. 10 carry 1 mark each

Q.1 Consider a CPU, where all the instructions require 6 clock cycles to complete their execution. Under the instruction set there are 215 instructions and a total of 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programmed control unit, single address field format is used for branch control logic.

What is the minimum size of control word and control address register.

(a) 136, 11 (b) 7, 12
(c) 7, 11 (d) 125, 12

Q.2 Consider the following Booth's multiplication

Multiplicand : 1011 0111 1111

Multiplier : 0110 1001 0110

How many arithmetic operations are required in the multiplication.

(a) 6 (b) 7
(c) 8 (d) 9

Q.3 Consider an instruction of indirect addressing mode. What are the number of memory reference by the processor when instruction is a computation that requires a single operand and when it is a branch instruction respectively?

(a) 3, 3 (b) 2, 3
(c) 3, 2 (d) 2, 2

Q.4 The following assembly code is to be executed in a 3-stage pipelined processor with hazard detection and resolution in each stage. The stage are IF, OF (one or more as required) and execution (including write-back operation). What are the number of possible RAW, WAW and WAR hazards in the execution of the code.

Instruction	Meaning
I_1: Inc R_0	$R_0 \leftarrow (R_0) + 1$
I_2: Mul ACC, R_0	Acc $\leftarrow$ (ACC) $\times$ (R_0)
I_3: Store R_1, ACC	$R_1 \leftarrow$ (ACC)
I_4: Add ACC, R_0	Acc $\leftarrow$ (ACC) + (R_0)
I_5: Store M, ACC	M $\leftarrow$ (ACC)

(a) 6, 1, 2 (b) 5, 3, 3
(c) 5, 3, 2 (d) 3, 1, 2

Q.5 Consider the following statements:

S_1: Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non-pipelined but identical CPU we can say that $T_1 \le T_2$.

S_2: The performance of pipelined processor suffers if the pipeline stages have different delays.

Which of the following option is correct?

(a) Both S_1 and S_2 are correct
(b) only S_1 is correct
(c) Only S_2 is correct
(d) None of S_1 or S_2 is correct

Q.6 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Programmed IO
B. Interrupt driven IO
C. Direct memory access

List-II

1. On I/O command issued by the processor, the process busy-waits for the operation to be completed.
2. After issuing an I/O command, processor continues to execute subsequent instructions, and is intrupted by the concerned module, when latter has completed its work.
3. Processor send a request for the transfer of a block of data to the concerned module and is interupted when the entire block has been transferred.

Which of the following code is correct?

Codes:

	A	B	C
(a)	1	3	2
(b)	1	2	3
(c)	2	1	3
(d)	1	3	2

Q.7 A cache block has 64 kbyte. The main memory has latency 64 μsec and bandwidth 1 GBps. What is the total time required to fetch the entire cache block from the main memory (in μsec, $1G=10^9$)?

(a) 125 (b) 128
(c) 135 (d) None of these

Q.8 A 4-way set associative cache memory consists of 128 blocks. The main memory consist of 32768 memory blocks and each block contain 512 eight bit words. Find how many bits are needed to represent TAG, SET and WORD field respectively?

(a) 5, 9, 10 (b) 10, 6, 8
(c) 10, 9, 5 (d) 10, 5, 9

Q.9 Consider the following statements :

S_1 : Microprogrammed control unit uses fixed logic to interrupt instruction.

S_2 : Horizontal microprogramming control unit requires an additional hardware (like a decoder)

S_3 : The overall performance of a system is directly proportional to the memory accesses which can be satisfied by the cache.

Which of the following option is true ?

(a) Only S_1 and S_2 (b) Only S_1 and S_3
(c) Only S_3 (d) None of the above

Q.10 Consider the following bit pattern represents the floating point number in IEEE 754 single precision format:

1 10000101 11000000000000000000000

Which of the following represents the decimal value of above floating point number?

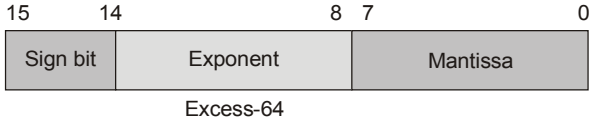
(a) –110 (b) –112
(c) –120 (d) –96

Q.No. 11 to Q.No. 30 carry 2 marks each

Q.11 The average seek time and rotational delay in a disk system are 6 ms and 3 ms, respectively. The rate of data transfer to or from the disk is 30 MBps and all disk accesses are of 8 KB of data. Disk DMA controller, the processor, and the main memory are all attached to a single bus. The data bus width is 32 bits, and a bus transfer to or from the main memory takes 10 nanoseconds. How many disk units are there that can be simultaneously transferring data to or from the main memory?

(a) 11 (b) 12
(c) 13 (d) 14

Q.12 Consider the following floating point format



Mantissa is a pure fraction in sign-magnitude form. What is the representation of decimal number 0.625×2^{18} in hexadecimal without normalization and rounding off ?

(a) 52B0 (b) 52A0
(c) 52A1 (d) None of these

Q.13 Consider the following statement. Out of the statements choose the one which best characterize computers that use memory mapped I/O.

(a) the computer provides special instruction for manipulating I/O port.
(b) I/O ports are placed at address on bus and as accessed just like other memory location.
(c) to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.
(d) ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

Q.14 Consider 4-way set associative cache of a 64 KB organized into a 32 blocks. Main memory size is 4 GB. In the cache controller, each line in the set contain 1 valid, 1 modified and 2 replacement bits along with a tag. How much space is required in the cache controller to store the tag information (Meta data) (in Kb)?

(a) 44 (b) 22
(c) 32 (d) 18

Q.15 Consider the following statements :

S_1: Delayed control transfer involve starting the execution of the instruction after a branch or control instruction regardless of whether the branch is taken.

S_2: A way to implement branch prediction is to store the result of a branch condition in a branch target buffer.

S_3: If, a multi-cycle, pipelined processor has '*N*' pipeline stages, then structural hazards can be avoided completely if at least '*N*' registers are available.

Which of the above statements are true ?

(a) S_1 only (b) S_1 and S_2 only
(c) S_1 and S_3 only (d) All of these

Q.16 Consider the 2 GHz clock frequency processor used execute the following program segment.

Instruction	Meaning	Size (in words)
I_1 : MOV r0, @3000	r0 ← m[[3000]]	4
I_2 : MOV r1, [2000]	r1 ← m[2000]	2
I_3 : ADD r0, [2000]	r0 ← r0 + m[2000]	1
I_4 : Sub r0, r1	rD ← r0 – r1	1
I_5 : Mov @ 3000, r0	m[[3000]] ← r0	4
I_6 : Halt	Machine halts	1

Assume that memory reference consumers 4 cycles and ALU operations consumes 2 cycles. What is the total time required to complete the program execution (in ns)?

(a) 32 (b) 34
(c) 36 (d) 40

Q.17 Assume that a hypothetical system in which program execution gives 200 stall cycles per instruction on an average. There are 260 and 120 misses in L_1 (Level-1) and L_2 (Level-2) cache out of total 1000 CPU references. If L_2 to memory miss penalty is twice the hit time. What are hit time of L_2 and "L_2 to memory miss penalty" values respectively (in cycles)? [Given 2.5 memory reference per instruction]

(a) 300, 600 (b) 400, 800
(c) 160, 320 (d) 160, 340

Q.18 We have two designs D_1 and D_2 for a synchronous pipeline processor. D_1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D_2 has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design D_2 over design D_1 for executing 100 instructions ?

(a) 214 nsec (b) 202 nsec
(c) 86 nsec (d) 200 nsec

Q.19 The designers of a cache system need to reduce the number of cache misses that occur in a certain group of programs. Which of the following statements is/are true?

S_1: If compulsory misses are most common, then the designers should consider increasing the cache line size to take better advantage of locality.

S_2: If capacity misses are most common, then the designers should consider increasing the total cache size so it can contain more lines.

S_3: If conflict misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs.

(a) S_3 only (b) S_1 and S_2 only
(c) S_2 and S_3 only (d) All of these

Q.20 Consider the following statements :

S_1: 3 control signals are needed for memory data register.

S_2: The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto same block.

Which of the following option is correct ?

(a) Only S_1 is true
(b) Only S_2 is true
(c) Both S_1 and S_2 are true
(d) Neither of S_1 or S_2 is true

Q.21 An instruction pipeline consist of 4 stages IF, ID, EX and WB. Four instructions need these stages for different number of cycles as shown by the table below

Instruction	# Cycle needed for			
	IF	ID	EX	WB
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1

Find number of clock cycles needed to execute the above 4 instructions.

(a) 12 (b) 13
(c) 14 (d) 15

Q.22 A Hypothetical control unit supports 5 groups of mutually exclusive signals

Group	G_1	G_2	G_3	G_4	G_5
Control Signal	2	1	4	27	17

Find size of control memory (in bytes) using vertical programming if control unit support 256 control word memory.

(a) 704 bytes (b) 672 bytes
(c) 604 bytes (d) 804 bytes

Q.23 Consider a CPU shared bus system in which each CPU requests the bus 35% of the time. What is the probability that exactly 3 CPU's are requesting the bus, when there are 10 CPU's competing for bus?

(a) 0.40 (b) 0.25
(c) 0.35 (d) 0.15

Q.24 Consider a system in which DMA technique is used to transfer 16 MB of data from an I/O device into memory. The bandwidth of I/O device is 128 KB/s. Once the data is filled into interface buffer, the DMA controller takes over the bus and transfer it to main memory in 28 sec.

What percentage of time is the CPU in busy mode (approximately)?

(a) 17 (b) 82
(c) 35 (d) 41

Q.25 Which of the following best characterize computers that uses memory mapped I/O?

(a) the computer provides special instruction for manipulating I/O port
(b) I/O ports are placed at addresses on bus and are accessed just like other memory location
(c) to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation
(d) ports are referenced only by memory mapped instruction of the computer and are located hard wired memory location

Q.26 Consider the addition of the two numbers 10001110 and 10000000 in an 8-bit ALU. Which of the following best summarizes the result and the status of the Z(zero), S(sign), C(carry) and O(overflow) flags? Assume that the numbers are represented in 2's Complement format and that S=1 if the result is negative.

(a) Sum = 100001110, Z = 0, C = 1, O = 0, S = 1
(b) Sum = 00001110, Z = 0, C = 0, O = 1, S = 0
(c) Sum = 100001110, Z = 0, C = 0, O =1, S = 0
(d) Sum = 100001110, Z = 0, C = 1, O =1, S = 0

Q.27 A CPU, which addresses the data through its 5 registers in one of 14 different modes, is to be designed to support 10 arithmetic instructions, 15 logic instructions, 20 data moving instructions and 10 branch instructions of these instructions 20%, 60%, 60% and 50% are respectively either single-operand or zero operand instructions and rest of them are double operand type. What is the minimum size of CPU instruction word?

(a) 18
(b) 19
(c) 20
(d) 21

Q.28 Consider a system employing an interrupt driven I/O for a particular device that transfers data at an average of 8 KB/s on a continuous basis. Assume that interrupt processing takes about 100 ns (i.e. jump to the interrupt service routine (ISR); execute it and return to the main program). Determine what fraction of processor time is consumed by this I/O device when it is interrupted for every byte.

(a) 0.41
(b) 0.8
(c) 0.36
(d) 0.72

Q.29 In a hypothetical system, the read and write operations occur 40% and 60% of the times respectively. If average cycle time for read and write are 79.1 ns and 84.2 ns respectively, find the data rate of memory approximately (in mega words/sec). Assume only one word is read and written in one cycle.

(a) 160
(b) 150
(c) 140
(d) 170

Q.30 Which of the following is/are true?

S_1: The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto same region.

S_2: For two level memory hierarchy cache and main memory, WRITE THROUGH results in more write cycles to main memory than WRITE BACK.

(a) Only S_1
(b) Both S_1 and S_2
(c) Only S_2
(d) Neither of them

■■■■

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COMPUTER SCIENCE & IT

Date of Test : 09/08/2023

ANSWER KEY ➤

1.	(a)	7.	(b)	13.	(b)	19.	(d)	25.	(b)
2.	(c)	8.	(d)	14.	(a)	20.	(d)	26.	(d)
3.	(c)	9.	(c)	15.	(b)	21.	(b)	27.	(b)
4.	(d)	10.	(b)	16.	(d)	22.	(a)	28.	(b)
5.	(c)	11.	(c)	17.	(c)	23.	(b)	29.	(a)
6.	(b)	12.	(b)	18.	(b)	24.	(b)	30.	(c)

DETAILED EXPLANATIONS

1. (a)

Since, it uses horizontal micro-programmed that requires 1 bit control / signal.
For 125 control signal, we need 125 bits.
Total number of micro-operation instruction = 215 × 6 = 1290
It requires 11 bit.

2. (c)

Multiplier	Pair with ($q-1$)	Recorder
0	0	0
1	0	–1
1	1	0
0	1	+1
1	0	–1
0	1	+1
0	0	0
1	0	–1
0	1	+1
1	0	–1
1	1	0
0	1	+1

3. (c)

When instruction is a computation:

Memory reference : Fetch instruction
Fetch reference of the operand
Fetch operand

Total 3 memory references.

When instruction is a branch:

Memory reference : Fetch instruction
Fetch operand reference and loading program counter

Total 2 memory references.

4. (d)

RAW:

$I_2 - I_1\ (r_0)$
$I_3 - I_2\ (\text{ACC})$
$I_5 - I_4\ (\text{ACC})$

Here, I_4 is non adjacent to I_1 and I_2. So, no need to consider that dependency under in-order dependency.

5. (c)

- In pipelined CPU, there will be buffer delays. So, for single instruction non-pipelined CPU takes less time compared to pipelined CPU.
- Structural dependencies cause hazards during pipelining.

6. (b)

Programmed I/O: Processor issues an I/O command, on behalf of a processor, to an IO module; that process then busy-waits for the operation to be completed before proceeding.

Interrupt driven I/O: The processor isues an IO command on behalf of a process, continues to execute subsequent instruction, and is interrupted by the IO module when the latter has completed its work.

Direct memory access: A DMA module controls the exchange of data between main memory and IO module.

7. (b)

For 1 second it take 10^9 byte

$$\text{So for 64 kbyte it takes} = \frac{64k}{10^9} = 64\ \mu\text{sec}$$

$$\text{Main memory latency} = 64\ \mu\text{sec}$$

$$\text{Total time required to fetch} = 64\ \mu\text{sec} + 64\ \mu\text{sec} = 128\ \mu\text{sec}$$

8. (d)

$$\text{Main memory size} = 32768 \text{ blocks}$$

$$1 \text{ block} = 512 \text{ words}$$

$$= 32768 \times 512 \text{ words} = 2^{15} \times 2^9 = 2^{24} \text{ words}$$

Main memory takes 24 bits.

Block size = 512 words = 2^9 words

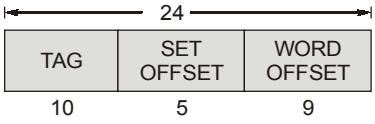
Number of bits for block size = 9 bits.

Number of blocks in set associative = 128

Number of blocks in one set = 4

$$\text{Number of sets in cache} = \frac{128}{4} = 32 = 2^5$$

Number of bits in set offset = 5 bits



Number of TAG bits = 24 – (9 + 5) = 10 bits.

9. (c)

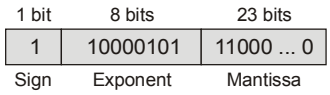
Consider each statement :

S_1 : Microprogrammed control unit uses variable logic to interrupt instruction since its uses encoded scheme for the instruction.

S_2 : Horizontal microprogramming control unit does not requires an additional hardware (like a decoder) because a fixed logic is associated with the instructions.

S_3 : The performance of a system depends on the direct proportion of memory accesses satisfied by cache.

10. (b)



$$\text{Bias exponent value} = 10000101$$

$$\text{Actual exponent} = 10000101 - 127 \qquad [\because 127 \text{ is bias}]$$

$$= 133 - 127 = 6$$

$$\text{Normalized mantissa bits} = 11000000000000000000000$$

$$\text{Actual value} = 1.11000000000000000000000$$

$$\text{Decimal number} = 1.11000 \times 2^6$$

$$= -(1110000)_2$$

$$= -(112)_{10}$$

11. (c)

Rate of transfer to or from any one disk = 30 MBps.

$$\text{Maximum memory transfer rate} = \frac{4\,B}{10\times10^{-9}} = 400\times10^{6}\text{Bps} = 400\text{ MBps}$$

Since rate of data transfer = 30 MBps

$$\text{Here number of disk transfer} = \left\lceil\frac{400}{30}\right\rceil = 13$$

Therefore, 13 disks can simultaneously transfer data to or from the main memory.

12. (b)

$$\text{Biased exponent} = 18 + 64 = 82$$

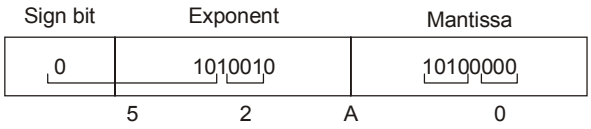
Representing 82 in binary

$$(82)_2 = (1010010)_2$$

Representing mantissa in binary

$$(0.625)_{10} = (0.10100000)$$

Floating point representation is as follows:



13. (b)

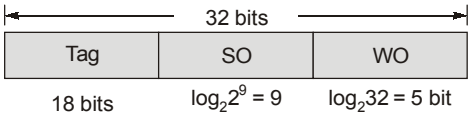
Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.

So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

14. (a)

$$\text{Number of lines} = \frac{64K}{32} = 2^{11}$$

$$\text{Number of sets} = \frac{2^{11}}{4} = \frac{2^{11}}{2^{2}} = 2^{9}$$



$$\text{Tag memory size} = S\times P\times \#\text{ tag bits}$$
$$= 2^{9}\times 4\times(18+1+1+2)$$
$$= 2^{9}\times 2^{2}\times 22\text{ bits} = 2^{10}\times 2\times 22\text{ bits} = 44\text{ K bits}$$

15. (b)

Considering each statement :

S_1 :Delayed control transfer, also known as delayed branching, is an attempt to cope with control hazards.

S_2 :The branch target stores the previous target address for the current branch, other algorithms for branch prediction also exist.

S_3 :For any given instruction set architecture implemented on a *N*-stage pipelined processor, *N* registers probably is not enough registers to completely prevent structural hazards involving a shortage of register hardware.

16. (d)

	IF	ID	OF	PD & WB
I_1:	1 m-ref	3 m-ref	2 m-ref	—
I_2:	1 m-ref	1 m-ref	1 m-ref	—
I_3:	1 m-ref	—	1 m-ref	2 cycles
I_4:	1 m-ref	—	—	2 m-ref
I_5:	1 m-ref	3 m-ref	—	2 m-ref
I_6:	1 m-ref	—	—	—

Total time = 80 cycles × 0.5 ns
= 40 ns

17. (c)

2.5 memory reference per instruction $\Rightarrow \frac{1000}{2.5}$ instruction per 1000 reference.

$\Rightarrow$ 400 instructions.

Now $200 = \left(\frac{260}{400}\right)x + \left(\frac{120}{400}\right)2x$

$$x = \frac{400 \times 200}{500}$$

$$x = \frac{80000}{500}$$

$$x = 160$$

$$2x = 320$$

18. (b)

D_1 : Number of stages, $k = 5$
$\tau_i = 3, 2, 4, 2, 3$ ns
$i = 1$ to 5
$\tau = \max(\tau_i) + d$ here d is negligible
$\tau = 4$ ns

D_2 : Number of stages, $k = 8$
$\tau_i = 2$ ns each
$i = 1$ to 8
$\tau = \max(\tau_0) = 2$ nsec

Number of instructions, $n = 100$

D_1: $T_k = (n + k - 1)\tau$
$= (100 + 5 - 1) \times 4$
$= 104 \times 4 = 416$ ns

D_2: $T_k = (n + k - 1)\tau$
$= (100 + 8 - 1) \times 2$
$= 107 \times 2 = 214$ ns

Total time saved = 416 – 214 = 202 ns

19. (d)

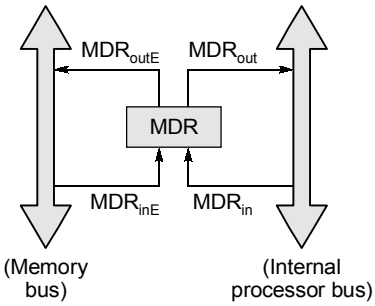
Increasing the cache line size brings in more from memory when a miss occurs. If accessing a certain byte suggests that nearby bytes are likely to be accessed soon (locality), then increasing the cache line essentially prefetches those other bytes. This, in turn, forestalls a later cache miss on those other bytes. If misses occur because the cache is too small, then the designers should increase the size!

Conflict misses occur when multiple memory locations are repeatedly accessed but map to the same cache location. Consequently, when they are accessed, they keep kicking one another out of the cache. Increasing the associativity implies that each chunk of the cache is effectively doubled so that more than one memory item can rest in the same cache chunk.

20. (d)

Considering each statement :

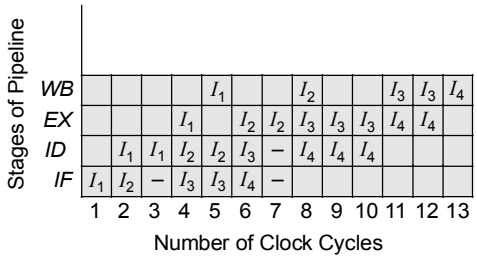
S_1 : 4-control signals are needed for each data register.



MDR is directly connected to data lines of the processor. It has 2 input and 2 output. Data may be loaded into MDR either from memory or from internal bus. Data present in MDR may be placed on either bus are memory. It requires total 4 control signals.

S_2 : The main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on the same region.

21. (b)



22. (a)

Number of bits for control signals in vertical programming:

$$\log_2(2) + \log_2(1) + \log_2(4) + \log_2(27) + \log_2(17)$$
$$= 1 + 1 + 2 + 5 + 5 = 14 \text{ bits}$$

256 CW = 8 bits

VCW:

Branch condition	Flag	Control field	Control memory address
		14	8

VCW size = 14 + 8 = 22 bits

Vertical control memory size = 256 × 22 bits

$$= \frac{256 \times 22}{8} \text{ bytes} = 704 \text{ bytes}$$

23. (b)

The required probability = $^{10}C_3 (0.35)^3 (0.65)^7 = 0.252$

24. (b)

Time taken by I/O device = $\frac{16\,\text{MB}}{128\,\text{kB}} = 128\,\text{sec}$

Percentage time CPU is busy = $\frac{128}{128+28} \times 100 = 82.05$

25. (b)

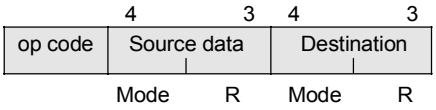
I/O ports are placed at addresses on bus and are accessed just like other memory location in computers that uses memory mapped I/O.

26. (d)

$$\begin{array}{r} 10001110 \\ 10000000 \\ \text{Sum} = \overline{100001110} \end{array}$$

Z = 0, C = 1, O =1, S = 0

27. (b)



Register = 5 = 3 bits

Modes = 14 =4 bits

Type	Single operand or No operand	Double operand
Arithmetic (10)	2	8
Logic (15)	9	6
Data moving (20)	12	8
Branch (10)	5	5

Total 27 double operands = 5 bits

Size of instruction word = 5 + 7 + 7 = 19

28. (b)

8 KB — 1 sec

1 B — ?

$$\Rightarrow \quad \frac{1B}{8\,KB}\text{sec}$$

$$\Rightarrow \quad 125\,\mu\text{sec}$$

Interrupt consumes 100 μsec

$$\therefore \quad \text{Fraction of processor time consumed for INT} = \left(\frac{100}{125}\right) \Rightarrow 0.8$$

29. (a)

Average access time for both read and write operations.

$$= 0.4 \times 79.1\text{ ns} + 0.6 \times 84.2\text{ ns} = 61.952\text{ ns}$$

$$\eta_{memory} = \frac{1}{61.952} = 161.4 \text{ Mega words/sec.}$$

30. (c)

- Main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on to same region.
- Because each and every WRITE operation is done simultaneously on both cache and main memory. WRITE THROUGH results in more cache cycles than WRITE BACK.

■■■■