S.No. : 01 LS1_EC_S+T_100919

Digital Electronics

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CLASS TEST 2019-2020

ELECTRONICS ENGINEERING

Date of Test : 10/09/2019

ANSWER KEY ➤ Digital Electronics

1.	(b)	7.	(b)	13.	(a)	19.	(c)	25.	(b)
2.	(c)	8.	(b)	14.	(b)	20.	(d)	26.	(c)
3.	(b)	9.	(d)	15.	(a)	21.	(b)	27.	(a)
4.	(d)	10.	(b)	16.	(b)	22.	(c)	28.	(c)
5.	(c)	11.	(a)	17.	(c)	23.	(c)	29.	(c)
6.	(c)	12.	(d)	18.	(b)	24.	(c)	30.	(b)

DETAILED EXPLANATIONS

1. (b)

Overall MOD = $3 \times 4 \times 5 = 60$

Lowest frequency is output frequency

$$f_{out} = \frac{24 \times 10^6}{60} = 400 \text{ kHz}$$

2. (c)

Master slave configuration stores 1-bit of data.

3. (b)

It is a toggle flip-flop, the values toggle

Q : 0 → 1 → 0 → 1 → 0 → 1

↑

initial state

4. (d)

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

5. (c)

Using POS form

$$\begin{aligned} Z &= (A+B+\bar{C})(\bar{A}+\bar{B}+\bar{C}) \\ &= (A+B)(\bar{A}+\bar{B})+\bar{C} \\ &= A \oplus B + \bar{C} \\ &= \bar{C} + (A \oplus B) \end{aligned}$$

6. (c)

$$\bar{Y} = A + B + C$$

$$\begin{aligned} Y &= \overline{A+B+C} = \bar{A}\bar{B}\bar{C} \\ &= \Sigma m(0) \\ &= \Pi M\,(1, 2, 3, 4, 5, 6, 7) \end{aligned}$$

7. (b)

$$x \oplus y \oplus xy = (\bar{x}y + x\bar{y}) \oplus xy = (\bar{x}y \oplus xy) + (x\bar{y} \oplus xy) = y(x \oplus \bar{x}) + x(y \oplus \bar{y})$$

$$= y + x$$

8. (b)

$$Y = I_0 \cdot \bar{S}_1\bar{S}_0 + I_1 \cdot \bar{S}_1 S_0 + I_2 \cdot S_1\bar{S}_0 + I_3 S_1 S_0$$

$$Y = A\bar{B} + (1)B = B + A\bar{B} = A + B$$

10. (b)

S_1	S_0	C	Q
$\bar{A}$	$\bar{B}$	C	$\bar{A}\bar{B}C$
$\bar{A}$	B	1	$\bar{A}B$
A	$\bar{B}$	1	$A\bar{B}$
A	B	1	AB

$$Q = \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC + AB\bar{C}$$
$$= \Sigma m(1, 2, 3, 4, 5, 6, 7)$$
$$= \Pi M(0)$$

11. (a)

- 4221 code is a self complementing code.

$\because$ $4 + 2 + 2 + 1 = 9$

- For a self complementing code system, codeword of "5" = 1's complement of codeword of "4"

$\because$ $5 = 9 - 4$ i.e, 9's complement of 4.

so, codeword of 5 = 1's complement of (1000)
= 0111

12. (d)

A ⇓ A_1 A_0 $\quad$ B ⇓ B_1 B_0

$A > B$ is possible when either of the following conditions is satisfied

1. When $A_1 > B_1 \Rightarrow$ i.e., when $G_1 = 1$
2. When $(A_1 = B_1)$ and $(A_0 > B_0) \Rightarrow$ i.e., when $E_1G_0 = 1$

So, the Boolean expression for G is

$$G = E_1G_0 + G_1$$

13. (a)

X	Y	Z	A
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

X \ YZ	I_0 00	I_1 01	I_2 10	I_3 11
0	0	1	0	1
1	0	1	1	0
	0	1	X	$\bar{X}$

Thus solution is option (a).

14. (b)

T_{min} = minimum clock period required

= time delay from the time of active clock edge to the point of time, where the latest change appears at the input of flip-flops before the application of next active clock edge.

Let us assume active clock edge is applied at $t = 0$,

then,

the latest change in Q_0 appears at $\Rightarrow t = 5\ \mu s$

the latest change in Q_1 appears at $\Rightarrow t = 4\ \mu s$

the latest change in Q_2 appears at $\Rightarrow t = 3\ \mu s$

the latest change in D_2 appears at $\Rightarrow t = 4\ \mu s$

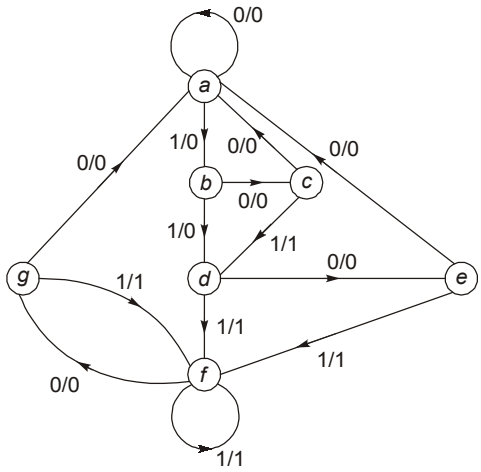
the latest change in D_1 appears at $\Rightarrow t = 8\ \mu s$

the latest change in D_0 appears at $\Rightarrow t = 10\ \mu s$

so $T_{min} = 10\ \mu sec$

$$f_{c\,max} = \frac{1}{T_{min}} = \frac{1}{10\ \mu sec} = 100\ kHz$$

15. (a)



the state table for given state diagram:

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

X = input

state-g and state-e are equal, so we can replace state-g with state-e

so, simplified state table will be,

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

now, state-f and state-d are equal. So, we can replace state-f with state-d
so, simplified state table will be,

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	e	d	0	1
e	a	d	0	1

now, state-e and state-c are equal. So, we can replace state-e with state-c
so, simplified state table will be,

Present state	Next state		Output	
	for $X = 0$	for $X = 1$	for $X = 0$	for $X = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	1
d	c	d	0	1

- it is not possible to reduce the state table further, as there are no more equal states.
- so, minimum number of states required to design the circuit = 4.

and minimum number of flip-flops required = 2.

16. (b)

A	B	f
0	0	P_1
0	1	P_2
1	0	P_3
1	1	P_4

so, the given pass logic network acts as EX-OR gate when $P_1 = P_4 = 0$ and $P_2 = P_3 = 1$.

17. (c)

The output z is connected from inverted outputs of the FFs through AND gate, i.e.

$$z = \bar{Q}_A \bar{Q}_B \bar{Q}_C = \overline{Q_A + Q_B + Q_C}$$

Hence, the output z will be high only when all FF's output are zero, i.e. $Q_A = Q_B = Q_C = 0$
Let initially $z = 1$, then we obtain the truth table for the circuit as

	Present State			Inputs						Next State			
CLK number	Q_A	Q_B	Q_C	J_A	K_A	J_B	K_B	J_C	K_C	Q_A^+	Q_B^+	Q_C^+	z
initial	0	0	0	-	-	-	-	-	-	-	-	-	1
1	0	0	0	1	1	1	1	0	1	1	1	0	0
2	1	1	0	1	1	1	1	1	1	0	0	1	0
3	0	0	1	1	1	0	1	0	1	1	0	0	0
4	1	0	0	1	1	1	1	0	1	0	1	0	0
5	0	1	0	1	1	1	1	1	1	1	0	1	0
6	1	0	1	1	1	0	1	0	1	0	0	0	1

It is MOD-6 counter. So, output z will be 1 after 6 clock pulses.

18. (b)

When Q_4Q_3 is 11, then CLR = 0, hence the count goes back to 00000.

$$Q_4\,Q_3\,Q_2\,Q_1\,Q_0 \qquad\qquad Q_4\,Q_3\,Q_2\,Q_1\,Q_0 \qquad\qquad Q_4\,Q_3\,Q_2\,Q_1\,Q_0$$
$$0\;0\;0\;0\;0 \longrightarrow 1\;0\;1\;1\;1 \longrightarrow 0\;0\;0\;0\;0$$

Thus, counter counts 0 - 23, and clears at 24. It's a MOD-24 counter.

19. (c)

$$f_{max} = \frac{1}{nt_{pd}} \;;$$

t_{pd} = propagation delay of each flip-flop and n = number of flip flops

$$t_{pd} = \frac{1}{n\times 25\times 10^6}\ \text{sec}$$

$$= \frac{1000}{4\times 25}\times 10^{-9}\ \text{sec} = 10\ \text{nsec}$$

20. (d)

Clk No.	Q_1	Q_2	
0	0	0	→initial
1	1	0	
2	1	1	
3	0	1	
4	0	0	

It's a Johnson counter after 4 clock pulses the state (Q_1Q_0) will be (00) again.

21. (b)

$$V_0 = -RV_{ref}\left[\frac{b_3}{2R}+\frac{b_2}{4R}+\frac{b_1}{8R}+\frac{b_0}{16R}\right]$$

$$= -\frac{V_{ref}}{16}\left[8b_3+4b_2+2b_1+b_0\right]$$

$$V_0 = -\frac{V_{ref}}{16}\ [\text{decimal equivalent of input binary code}]$$

given input binary code $= (0110)_2 = (6)_{10}$

so, $$V_0 = \frac{10}{16}(6) = 3.75\ \text{V}$$

22. (c)

A	B	J	K	Q_{n+1}
0	0	1	0	1
0	1	1	1	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0

$$Q_{n+1} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B\bar{Q}_n$$

$$Q_{n+1} = \bar{B} + \bar{A}B\bar{Q}_n = \bar{B} + \bar{A}\bar{Q}_n$$

23. (c)

Output of the 4 : 1 MUX circuit in Figure A is

$$Y = I_0\bar{A}\bar{B} + I_1\bar{A}B + I_2 A\bar{B} + I_3 AB$$

Output of the circuit in Figure B is

$$Y = A \oplus B \oplus C = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

On comparison

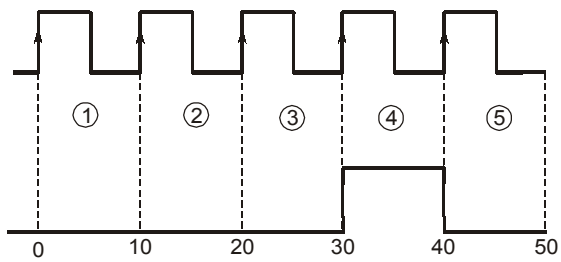
$$I_0 = C$$
$$I_1 = \bar{C}$$
$$I_2 = \bar{C}$$
$$I_3 = C$$

24. (c)

$$Y = (A \oplus B)\cdot A = (\bar{A}B + A\bar{B})\cdot A$$

$$= A\bar{B} = D_2 \cdot \bar{D}_0$$

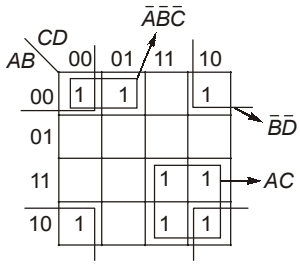
Clock Number	D_4	D_3	D_2	D_1	D_0	Y	
initial	0	1	0	1	0	0	$t \le 0$
1	0	0	1	0	1	0	$0 < t < 10$ ns
2	1	0	0	1	0	0	10 ns $< t <$ 20 ns
3	0	1	0	0	1	0	20 ns $< t <$ 30 ns
4	1	0	1	0	0	1	30 ns $< t <$ 40 ns
5	0	1	0	1	0	0	40 ns $< t <$ 50 ns



The LED will be in ON state for 30 ns $< t <$ 40 ns. So, option (c) is the correct answer.

25. (b)

The *k*-map has to rearranged as



$$F = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{D} + AC$$

26. (c)

$$F = \overline{(A+B)C + D}$$

27. (a)

In the circuit, we have

$$D_0 = \overline{Q_1 Q_2} = \bar{Q}_1 + \bar{Q}_2$$
$$D_1 = Q_0$$
$$D_2 = Q_1$$

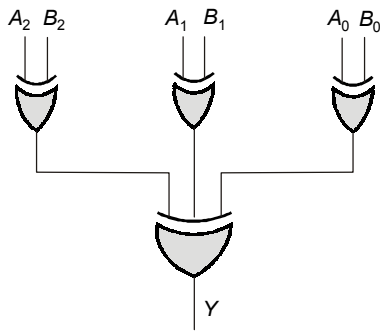
The truth table for the circuit is obtained below.

	Present State			Inputs			Next State		
CLK number	Q_2	Q_1	Q_0	D_2	D_1	D_0	Q_2^+	Q_1^+	Q_0^+
initial	0	0	0	-	-	-	-	-	-
1	0	0	0	0	0	1	0	0	1
2	0	0	1	0	1	1	0	1	1
3	0	1	1	1	1	1	1	1	1
4	1	1	1	1	1	0	1	1	0

After 4 clock pulses, output is $Q_2\ Q_1\ Q_0 = 110$

28. (c)

Redrawing the digital circuit



From the figure we get,

$$Y = A_0 \oplus B_0 \oplus A_1 \oplus B_1 \oplus A_2 \oplus B_2$$

So, Y is XOR of six boolean variables and Y will be 1 when odd number of variable are 1. Thus there will be $\frac{2^6}{2} = 32$ cases for the output to be 1.

29. (c)

Q_0	Q_1	J_0	K_0	J_1	K_1	Q_0^+	Q_1^+	
0	0	1	1	0	1	1	0	} MOD = 3
1	0	1	1	1	0	0	1	
0	1	0	1	0	1	0	0	
0	0	1	1	0	1	1	0	
1	0	1	1	1	0	0	1	
0	1	0	1	0	1	0	0	

30. (b)

Since its an inverting amplifier,

$$V_{out} = -9.375 \text{ V} \quad \text{when } |V_{out}| = 9.375 \text{ V}$$

maximum output means all bits are 1

i.e., $b_0 b_1 b_2 \ldots\ldots b_n = 1111 \ldots\ldots 1$

$$V_{out} = -V\left(\frac{R}{R}b_0 + \frac{R}{2R}b_1 + \frac{R}{4R}b_2 + \frac{R}{8R}b_3 \ldots\ldots + \frac{R}{2^{n-1}R}b^n\right)$$

$$-9.375 = -5\left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \ldots\ldots + \frac{1}{2^{n-1}}\right)$$

$$1.875 = \frac{\left(1-\left(\frac{1}{2}\right)^n\right)}{1-\frac{1}{2}}$$

$$\frac{1}{2}\times 1.875 = 1-\left(\frac{1}{2}\right)^n$$

$$\left(\frac{1}{2}\right)^n = 1-\frac{1}{2}\times 1.875 = 0.0625 = \frac{1}{16}$$

so, $2^n = 16$

$n = 4$

■■■■