CLASS TEST

Sl.: 02SKCS-ABCD-20072023

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DIGITAL LOGIC

COMPUTER SCIENCE & IT

Date of Test : 20/07/2023

ANSWER KEY ➤

1.	(b)	7.	(a)	13.	(d)	19.	(c)	25.	(b)
2.	(c)	8.	(b)	14.	(c)	20.	(b)	26.	(c)
3.	(a)	9.	(c)	15.	(b)	21.	(b)	27.	(d)
4.	(c)	10.	(c)	16.	(a)	22.	(b)	28.	(d)
5.	(b)	11.	(b)	17.	(a)	23.	(b)	29.	(a)
6.	(d)	12.	(c)	18.	(c)	24.	(b)	30.	(a)

DETAILED EXPLANATIONS

1. (b)

Converting into decimal,

$$(2)_3 = 2 \times 3^\circ = 2$$
$$(3)_4 = 3 \times 4^\circ = 3$$
$$(14)_5 = 1 \times 5^1 + 4 \times 5^\circ = 9$$
$$(15)_6 = 1 \times 6^1 + 5 \times 6^\circ = 11$$

2. (c)

The characteristics tabel with J, K, Q_n, Q_{n+1} and the excitation table for S and R is shown below –

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

The K-map for S and R is shown as –

For S,

$$S(J, K, Q_n) = \Sigma m(4, 6) + d(1, 5) = J\bar{Q}_n$$

J \ KQ_n	00	01	11	10
0		×		
1	1	×		1

$$S = J\bar{Q}_n$$

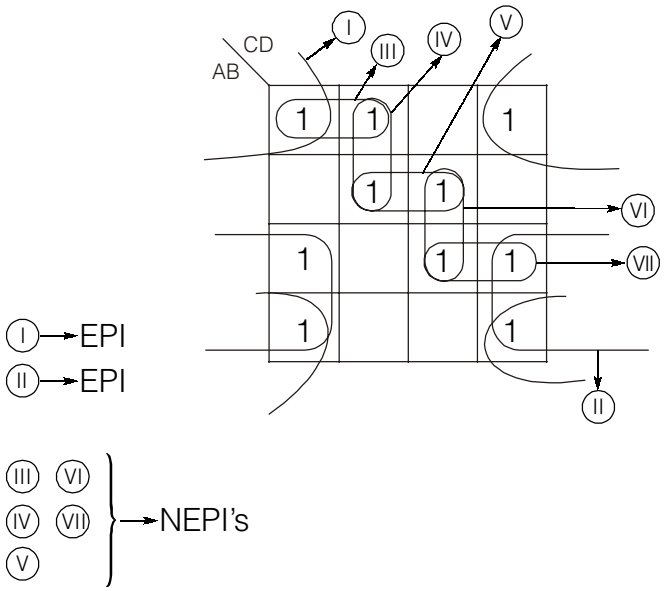
For R,

$$R(J, K, Q_n) = \Sigma m(3, 7) + d(0, 2) = KQ_n$$

J \ KQ_n	00	01	11	10
0	×		1	×
1			1	

$$R = KQ_n$$

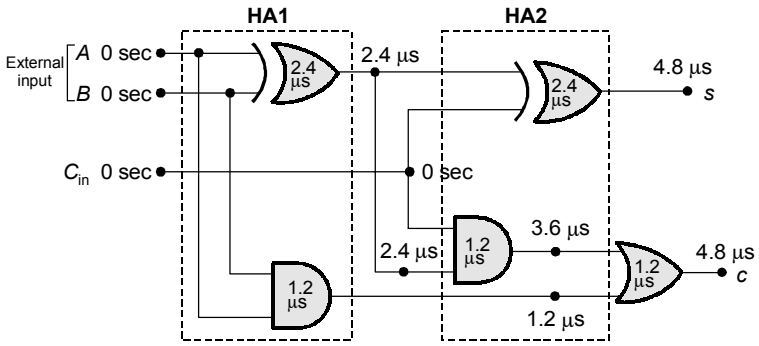
3. (a)



EPI = Essential Prime Implicant [which cover a minterm not covered by any other prime implicants]
NEPI = Non Essential Prime Implicant. Number of EPI's = 2, number of NEPI's = 5.

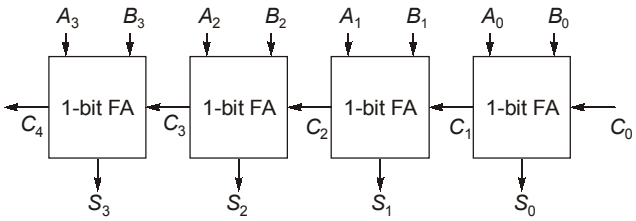
4. (c)

For one full Adder :



The propagation delay of AND / OR gate t_{pd} = 1.2 µ sec.
The propagation delay of EX-OR gate $2t_{pd}$ = 2.4 µ sec.

- Binary Adder external inputs are available to all HA1's simultaneously.
- First HA1 output of all full adders are available simultaneously with delay of 2.4 µsec (i.e., $2t_{pd}$).
- Carry generate from previous Full adder is passing only through HA2 of next full adder.
- The delay of LSB full adder = $4t_{pd}$.
- The 4 bit ripple carry binary delay:



$= 4t_{pd} + 2t_{pd} + 2t_{pd} + 2t_{pd} = 10t_{pd}$
$= 10 \times 1.2$ µsec $= 12$ µsec

5. (b)

For MOD - 10 counter –

X = Jhonson counter required = 5 FF's

Y = ring counter required = 10 FF's

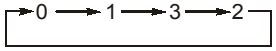
Z = ripple counter required = 4 FF's

$X + Y + Z = 5 + 10 + 4$

$= 19$ FF' s.

6. (d)

Clk	Q_1	Q_0	*FF*1		*FF*0	
			$J_1 = Q_0$	$K_1 = \overline{Q}_0$	$J_0 = \overline{Q}_1$	$K_0 = Q_1$
	0	0	0	1	1	0
1	0	1	1	0	1	0
2	1	1	1	0	0	1
3	1	0	0	1	0	1
4	0	0				



$N = 4$

$K = 334$

$K \% N = 2 = (11)_2$

7. (a)

Prime implicants are:

Cells(0, 2, 8, 10) : This is an EPI because it covers minterm 2 uniquely.

Cells(0, 1, 8, 9) : This is an EPI because it covers minterm 1 uniquely.

Cells (10, 14) : This is an EPI because it covers minterm 14 uniquely.

So, 3 PI, 3 EPI.

So, PI + EPI = 3 + 3 = 6

8. (b)

M = 1000 1111; N = 0110 0010; O = 0100 1001; P = 0111 0010

Now, program execution begins:

1. M ← M ⊕ N :: //M = 1110 1101
2. M ← CSL M :: //M = 1101 1011
3. N ← M + N :: //N = 0011 1101
4. O ← O ∧ N :: //O = 0000 1001
5. O ← CSR O :: //O = 1000 0100
6. P ← P + 1 :: //P = 0111 0011
7. P ← P + O :: //P = 1111 0111

Hence, answer is option (b).

9. (c)

$$Y = \overline{ABC + \bar{A}\bar{B}} + BC$$

Dual of Y

$$Y_d = \overline{(A+B+C)\cdot(\bar{A}+\bar{B})}\cdot(B+C) = \left[\overline{(A+B+C)} + \overline{(\bar{A}+\bar{B})}\right]\cdot(B+C)$$

Compliment of Y

$$Y_c = \overline{\overline{(ABC + \bar{A}\bar{B})} + BC} = \overline{\overline{ABC + \bar{A}\bar{B}}}\cdot\overline{BC}$$

$$= (ABC + \bar{A}\bar{B})\cdot\overline{BC}$$

10. (c)

Output of the 4 : 1 MUX circuit in Figure **A** is

$$Y = I_0\bar{A}\bar{B} + I_1\bar{A}B + I_2A\bar{B} + I_3AB$$

Output of the circuit in Figure **B** is

$$Y = A \oplus B \oplus C = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

On comparison

$$I_0 = C$$
$$I_1 = \bar{C}$$
$$I_2 = \bar{C}$$
$$I_3 = C$$

11. (b)

$$Y_1 = \bar{c}$$
$$F = Y_2 = \bar{d}Y_1 + dc$$
$$= \bar{d}\bar{c} + dc$$
$$= c \odot d$$

12. (c)

A	B	J	K	Q_{n+1}
0	0	1	0	1
0	1	1	1	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0

$$Q_{n+1} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B\bar{Q}_n$$
$$Q_{n+1} = \bar{B} + \bar{A}B\bar{Q}_n$$
$$= \bar{B} + \bar{A}\bar{Q}_n$$

13. (d)

14. (c)

Number of flip-flops for mod-16 ripple counter = 4

$$\text{Maximum clock frequency} = \frac{10^9}{4p}\text{Hz} = 5\text{ MHz}$$

$$p = \frac{10^9}{4\times5\times10^6} = \frac{1000}{20}$$
$$p = 50$$

15. (b)

Let the base be x, then

$$292_{10} = 1204\,x$$
$$= 1 \times x^3 + 2 \times x^2 + 0 \times x^1 + 4 \times x^0$$
$$= 292_{10}$$
$$= x^3 + 2x^2 + 4$$
$$= 6 \text{ (By substitution)}$$

16. (a)

For the given 4 × 1 MUX, 'A' and 'B' are select lines and 'C' be the input

	I_0	I_1	I_2	I_3
$\bar{C}$	⓪	2	④	6
C	①	3	⑤	7
	1	0	1	0

So, $I_0 = 1 = a$

$I_1 = 0 = b$

$I_2 = 1 = c$

$I_3 = 0 = d$

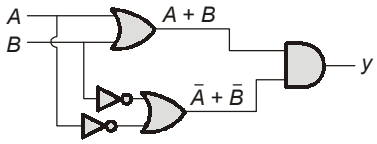
So, $a \oplus d = b \oplus c = 1$

So, output of NAND gate is 0 i.e. MUX 'E' connected to '0'.

The MUX is in disable state. MUX is having active high enable, but $E = 0$, so that MUX is in disable state.

Hence MUX output Z is equal to '0'.

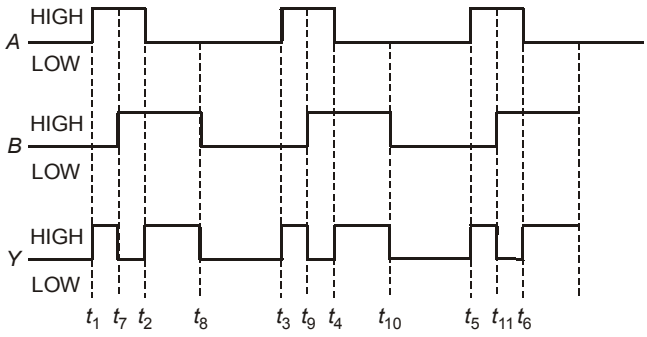
17. (a)



$= (A+B)(\bar{A}+\bar{B})$

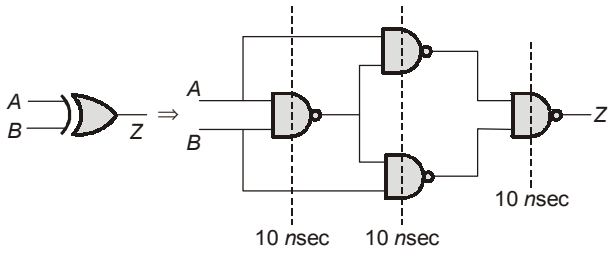
$= A\bar{B} + \bar{A}B$

$= A \oplus B$

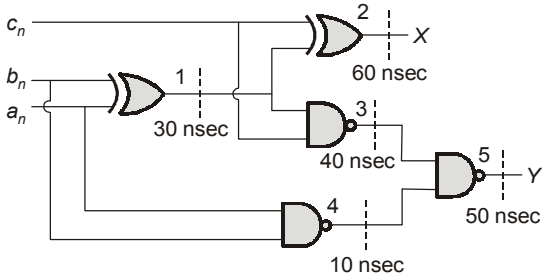


18. (c)

An Ex-OR gate can be represented as

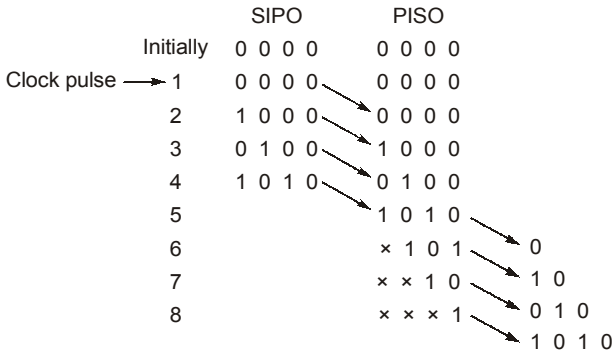


So, for EX-OR gate, it will take 30 nsec to get the output.



So, to get the output *Y*, it will take 50 nsec.

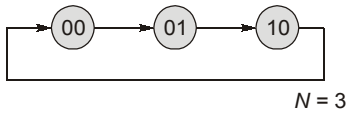
19. (c)



So, after 8 pulses, the output from PISO will be same as input in SIPO.

20. (b)

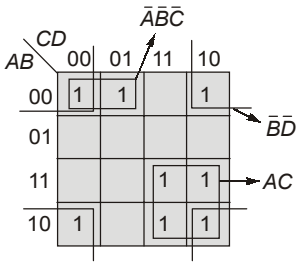
			FFO		FFI	
CLK	Q_1	Q_0	$J_0 = \overline{Q}_1$	$K_0 = 1$	$J_1 = Q_0$	$K_1 = \overline{Q}_0$
	0	0	1	1	0	1
1	0	1	1	1	1	0
2	1	0	0	1	0	1
3	0	0				



$N = 3$

21. (b)

The *k*-map has to rearranged as



$$F = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{D} + AC$$

22. (b)

Simplifying boolean expression:

$$\begin{aligned} F &= C(B + C)(A + B + C) \\ &= (CB + CC)(A + B + C) \\ &= (CB + C)(A + B + C) \\ &= C(1 + B)(A + B + C) \\ &= C(A + B + C) \\ &= AC + BC + C \\ &= C(1 + A + B) \\ &= C \end{aligned}$$

23. (b)

Let the base be x, then

$$\begin{aligned} 292_{10} &= 1204\,x \\ &= 1 \times x^3 + 2 \times x^2 + 0 \times x^1 + 4 \times x^0 \\ &= 292_{10} \\ &= x^3 + 2x^2 + 4 \\ &= 6 \text{ (By substitution)} \end{aligned}$$

24. (b)

Gray codes are less error-prone for mechanical devices that involve making and breaking electrical circuits because they only change in one bit position at a time.

So, they are considered as the minimum error code.

25. (b)

$$Y = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3$$

$$I_0 = I_3 = S_1 \text{ and } I_1 = I_2 = S_0$$

So,
$$\begin{aligned} Y &= \bar{S}_1\bar{S}_0S_1 + \bar{S}_1S_0S_0 + S_1\bar{S}_0S_0 + S_1S_0S_1 \\ &= \bar{S}_1S_0 + S_1S_0 = S_0 \end{aligned}$$

So, whenever $S_0 = B$, output $(Y) = B$

So, option (b) is correct.

26. (c)

All the statements are correct.

27. (d)

- S_1 is incorrect, as mentioned in question would required five 4X1 MUX instead of three.
- S_2 is incorrect, as it is not always the case. For example, the function $f(x, y, z) = \Sigma_m(2, 4, 5, 6)$ can have different PI when group differently in K-map.

28. (d)

Let $x = y \odot z$

So, $x \odot y \odot z$

$$\frac{y \odot z}{P} \odot \frac{y \odot z}{P}$$

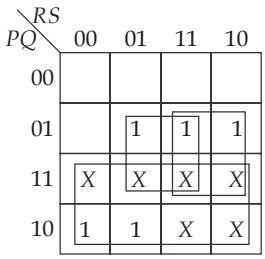
and $P \odot P = 1$. So option (d) is correct.

29. (a)

Truth table for BCD to excess-3 code output:

Decimal Value	Input				Output				Decimal Value
	P	Q	R	S	P	Q	R	S	
0	0	0	0	0	0	0	1	1	3
1	0	0	0	1	0	1	0	0	4
2	0	0	1	0	0	1	0	1	5
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	1	1	7
5	0	1	0	1	1	0	0	0	8
6	0	1	1	0	1	0	0	1	9
7	0	1	1	1	1	0	1	0	10
8	1	0	0	0	1	0	1	1	11
9	1	0	0	1	1	1	0	0	12

K-map for P: $f(P, Q, R, S) = \Sigma m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$



$= P + QS + QR$

$= P + Q(S + R)$

30. (a)

In the given digital circuit each multiplexer is working as a NOT gate thus it is a ring oscillator with five NOT gates.

The frequency of oscillation will be $f = \dfrac{1}{2Nt_{pd}}$.

N = number of NOT gates in cascade

t_{pd} = propagation delay of each NOT gate.

$\therefore \quad f = \dfrac{1}{2 \times 5 \times 25ns} = 4 \times 10^6$ Hz = 4 MHz.

■■■■