S.No. : 04 BS1_CS_A_230819

Computer Organization

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CLASS TEST 2019-2020

COMPUTER SCIENCE & IT

Computer Organization

Date of Test : 23/08/2019

Answer Key

1.	(d)	7.	(b)	13.	(d)	19.	(a)	25.	(b)
2.	(b)	8.	(c)	14.	(d)	20.	(c)	26.	(d)
3.	(c)	9.	(c)	15.	(a)	21.	(a)	27.	(b)
4.	(b)	10.	(b)	16.	(a)	22.	(a)	28.	(a)
5.	(b)	11.	(d)	17.	(b)	23.	(c)	29.	(c)
6.	(c)	12.	(a)	18.	(c)	24.	(c)	30.	(b)

DETAILED EXPLANATIONS

1. (d)

Computer uses addressing mode technique for giving program versatility to user by providing facilities as a pointer to memory counters for loop control and to reduce number of bits in the field of instruction.
Addressing modes are used in specifying rules for modifying or interpreting address field of the instruction.
So all options are correct.

2. (b)

Dirty bit is used to represent the status of cache whether it has been defined after copying from main memory to cache. Dirty bit = 0 shows no modification and dirty bit = 1 shows modification.

3. (c)

For making use of pointer in programs, indirect addressing mode is used.
Pointer stores the address of an variable and indirect addressing mode stores address of effective address in instruction.
Position independent code makes use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.
Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (b)

$$1 \text{ sec} \rightarrow 50 \text{ kbyte}$$

$$1 \text{ byte} \rightarrow \frac{1}{50k} = 20 \times 10^{-6} \text{ sec} = 20 \ \mu\text{sec}$$

For interrupt driven mode it takes 50 μsec
So performance achieved when interrupt driven used over programmed I/O

$$S = \frac{ET_{prog-IO}}{ET_{INT-IO}}$$

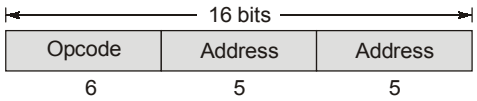
$$S = \frac{20}{50} = 0.4$$

5. (b)

In horizontal: 1 + 5 + 7 + 15 + 8 = 36
In vertical: log 1 + log 5 + log 7 + log 15 + log 8 = 1 + 3 + 3 + 4 + 3 = 14
Total saved bits = 36 – 14 = 22

6. (c)

Address format



Number of operations = $2^6 = 64$
Number of free opcodes after 2-address = 64 – 2 = 62
Number of 1 add instruction = 62 × 32 = 1984
Free opcodes = 1984 – 1024 = 960
Number of 0 add instruction = 960 × 32 = 30720

7. (b)

- More than one word are put in one cache block to explicit in the spatial locality of reference.

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- By the help of virtual memory, programs can exceed from the size of primary memory, hence increases the degree of multi programming.
- Increasing RAM will result in fewer page faults.

Hence only S_2 is the correct statement.

8. (c)

Multiplier	Pair with ($q-1$)	Recorder
0	0	0
1	0	–1
1	1	0
0	1	+1
1	0	–1
0	1	+1
0	0	0
1	0	–1
0	1	+1
1	0	–1
1	1	0
0	1	+1

9. (c)

251 opcodes $\Rightarrow$ 8 bits for each register

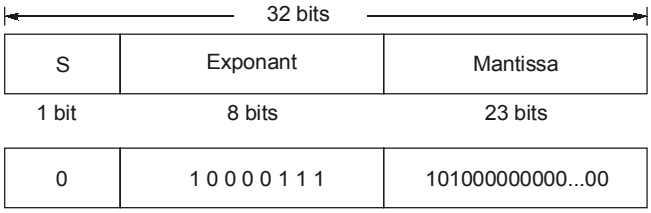
$\therefore$ | Opcode | R_1, R_2, R_3, R_4 |

8 bits + 5 × 4 bits = 8 + 20 = 28 bits

[$\because$ 4 for 4 registers i.e., R_1, R_2, R_3, R_4].

10. (b)

Format of single precision floating point is



$$\text{Value} = 1.M \times 2^{E-127} = 1.1010 \times 2^{135-127} = (1.1010)_2 \times 2^8 = 1.625 \times 2^8$$
$$= (416)_{10}$$

Octal representation

8	416	
8	52	0
	6	4

Octal representation is (640).

11. (d)

S1: Compulsory miss can be reduced by increasing the line size i.e., reduce number of lines.

S2: Conflict miss are occur when too many blocks are mapped into same line or set. So by increasing the associativity i.e. increases the size of set and increases the number of sets.

S3: Capacity miss can be reduced by increasing the cache memory size.

All of the three statements are true.

12. (a)

512 kW = 2^{19} words = 19 bit address

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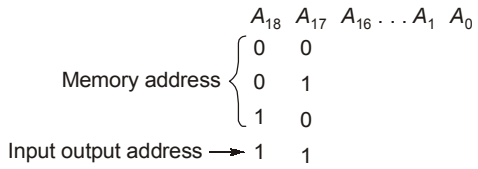


So number of input output addresses = 1×2^{17}
Number of memory addresses = 3×2^{17}

13. (d)

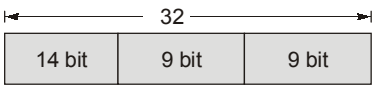
All the above statements are correct.

S1: Reference bit some times called access bit used in page table entry to show if page is replaced or not.

S2: In hierarchial memory access, CPU perform read and write operation only on level 1 memory. If miss occur then data is first transferred to level 1 then CPU access data.

S3: In simultaneous memory access, CPU perform read and write operation on any level of memory i.e. not necessary to take data first into level 1 memory than access it.

14. (d)



2^{14} two address instructions are possible.
Here 400 two addresses are needed so $(2^{14} - 400)$ op-codes are free.
We can store $(2^{14} - 400) \times 2^9$ one address instructions.

15. (a)

Write through protocol update cache and main memory simultaneously where write back first cache is updated and marked by dirty bit then main memory is updated.
Dirty bits are used by only write back protocol to know which cache block is updated.

16. (a)

For non-pipelined processor:

For p-instruction execution time = $\frac{(p \times 5)}{5} = p$ ns

Pipelined processor:

For p-instruction execution time = $\frac{p}{3} = 0.33p$ ns

Speed-up = $\frac{p}{0.33p} = 3.03$

17. (b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.
So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

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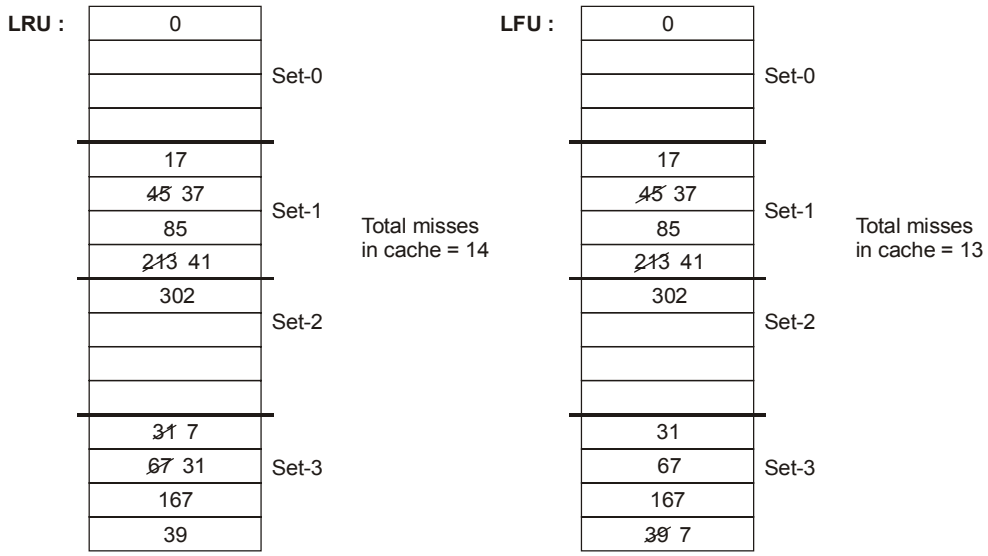
18. (c)



19. (a)

Number of interupts generated = 5000 interrupt / sec

Time by 1 interrupt = 200 μsec

Time consumed by every interrupt = 250 μs

Fraction of processor time consumed = 200/250 = 0.8

In % = 0.8 × 100 = 80

20. (c)

$$\text{Speedup (S)} = \frac{1}{(1-\text{Cache \% used}) + \left[\frac{\text{Cache \% used}}{\text{Speedup using cache}}\right]}$$

$$= \frac{1}{(1-F)+\left(\frac{F}{S}\right)} = \frac{1}{(1-0.9)+\left(\frac{0.9}{30}\right)} = \frac{1}{(0.1)+\left(\frac{0.9}{30}\right)} = \frac{30}{3.9} = 7.69$$

21. (a)

$$\text{CPI} = \text{CPI}_{\text{execution}} + \text{Memory stall per instruction} \quad ...(1)$$

$$\text{Memory stall per instruction} = \text{Memory access / Instruction} * \text{Miss rate} * \text{Miss penalty} \quad ...(2)$$

$$\text{Memory access / Instruction} = \text{Instruction fetch + Load / store} = 1 + 0.3 = 1.3 \quad ...(3)$$

from (2) and (3)

$$\text{Memory stall / Instruction} = 1.3 \times 0.15 \times 5 = 0.975 \quad ...(4)$$

from (1) and (4)

$$\text{CPI} = 1.1 + 0.975 = 2.075$$

The ideal memory CPU with no misses = $\frac{2.075}{1.1}$ = 1.88 time faster

22. (a)

DMA transfer character at rate of 19200 bpsec

8 bit = 1 character

So, 192000 b = 2400 character

So, 1 sec = 2400 character

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$$1 \text{ character} = \frac{1}{2400} = 416.7 \times 10^{-6} \text{ sec}$$

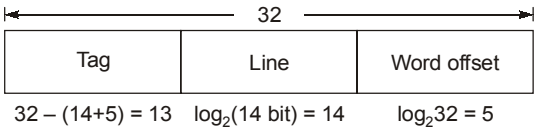
Processor fetch rate is 2 MIPS

$$1 \text{ MIPS} = 1 \text{ sec}$$

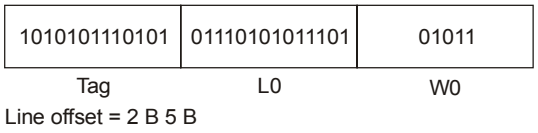
$$1 \text{ Instruction} = \frac{1}{2 \times 10^6} = 0.5 \text{ micro-sec}$$

$$\% \text{ slow down using DMA} = \frac{0.5 \times 10^{-6}}{416.7 \times 10^{-6}} \times 100 = \frac{0.5}{416.7} = 0.11\%$$

23. (c)



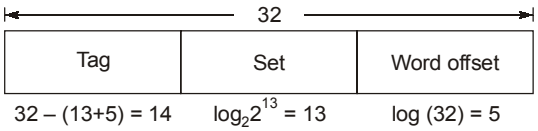
Main memory address:

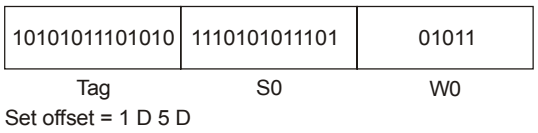


Line offset = 2 B 5 B

2-way set associative cache:

$$\text{Number of set} = \frac{N}{P\text{-way}} = \frac{2^{14}}{2^1} = 2^{13}$$





Set offset = 1 D 5 D

24. (c)

Total number of opcode possible with 5 bit = 32

16 opcode for double operand remaining = 32 – 26 = 6

Remaining = $2^6 \times 6 = 384$

Out of 384, 184 single operand instruction, so remaining are 384 – 184 = 200

Total number of free instruction (zero operand) = $200 \times 2^6 = 2^6 \times 200 = 12800$

25. (b)

	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
I_1	IF	ID	EX	MM	WB					
I_2		IF	ID	EX	MM	WB				
I_3			IF	ID	ID	EX	MM	WB		
I_4				IF	–	ID	EX	MM	WB	
I_5						IF	ID	EX	MM	WB

10 clock cycles used.

To achieve the CPI = 1 number of instructions must be inserted = 10.

Number of instructions present using operand forwaring with 10 cycles = 10 – 5 = 5

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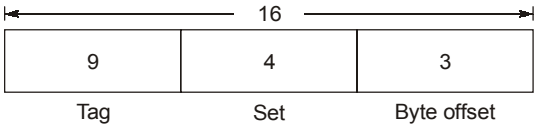
26. (d)

Given memory is byte addressable:



$$\text{Number of set} = 16 - (9 + 3) = 4 \text{ bits} = 2^4 = 16 \text{ sets}$$

$$\text{Number of blocks} = \frac{1024}{16} = \frac{2^{10}}{2^4} = 64 \text{ blocks}$$

$$\text{Associativity} = \frac{\text{Number of blocks}}{\text{Number of sets}} = \frac{64}{16} = 4$$

27. (b)

16 bytes per block, so there are $\log_2 16 = 4$ bits.

Cache size = 17408 bytes

$$\therefore \quad \frac{17408}{16} = 1088 \text{ blocks}$$

The cache is 17 way associative, so, there are $\frac{1088}{17} = 64$ sets

$$\therefore \quad \log_2 64 = 6 \text{ bits (set number)}$$

Number of tag bits is $32 - 6 - 4 = 22$ tag bits.

$$22 + 4 = 26$$

28. (a)

$$S_x = \frac{\text{Pipeline depth}}{(1 + \text{Frequency} \times \#\text{stalls per instruction})} = \frac{5}{1 + (0.3 \times 4)} = 2.27$$

$$S_y = \frac{9}{1 + (0.3 \times 8)} = 2.64$$

$$\frac{S_x}{S_y} = 0.859$$

29. (c)

$$\text{Speed up} = \frac{\text{Pipeline depth}}{(1 + \text{Branch frequency} \times \text{Branch penalty})} \geq 4$$

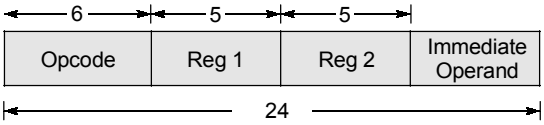
$$\frac{5}{1 + P \times 3} \geq 4$$

$$4 + 12P \leq 5$$

$$12P \leq 1$$

$$P \leq \frac{1}{12} = 0.0833$$

30. (b)



49 instructions $\Rightarrow$ 6 bits needed for Op-code

32 registers $\Rightarrow$ 5 bits needed for register operands

Immediate operand bits = 8

Minimum value = $-2^7 = -128$

Since 1 bit is gone for sign representation.

■■■■

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