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DIGITAL ELECTRONICS

ELECTRONICS ENGINEERING

Date of Test : 24/06/2023

ANSWER KEY ➤

1.	(b)	7.	(b)	13.	(c)	19.	(b)	25.	(b)
2.	(c)	8.	(a)	14.	(d)	20.	(d)	26.	(d)
3.	(b)	9.	(d)	15.	(c)	21.	(b)	27.	(c)
4.	(a)	10.	(c)	16.	(b)	22.	(a)	28.	(b)
5.	(c)	11.	(b)	17.	(a)	23.	(b)	29.	(b)
6.	(b)	12.	(c)	18.	(d)	24.	(b)	30.	(d)

DETAILED EXPLANATIONS

1. (b)

In J-K flip-flop

J	K	Output
1	0	Set
0	1	Reset
0	0	Hold
1	1	Racearound

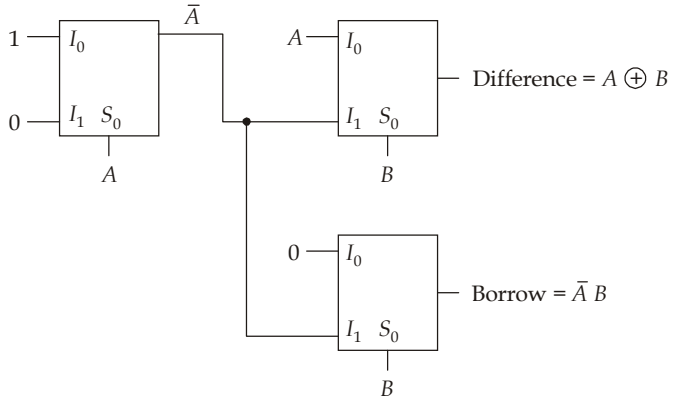
2. (c)

A look ahead carry generator is created using combinational circuit.

3. (b)

$$\begin{aligned} X \oplus Y &= \overline{X \odot Y} = \overline{\bar{X}\bar{Y} + XY} \\ &= \overline{(\bar{X}\bar{Y})}\,\overline{(XY)} \\ &= (X+Y)(\bar{X}+\bar{Y}) \\ &= \bar{X}+\bar{Y} \qquad (\because\ X + Y = 1 \text{ which is given}) \end{aligned}$$

4. (a)



5. (c)

The expression of Y can be written as

$$Y = (A)\bar{A}\bar{B} + (B)\bar{A}B + (B)A\bar{B} + (A)AB = \bar{A}B + AB = B$$

6. (b)

Given Count : 1 0 1 1 0 0 1 1 1 1

+ 1

Next Count : 1 0 1 1 0 1 0 0 0 0

complemented output

$\therefore$ No. of flip flop : 5

7. (b)

$$\begin{aligned} Y &= AB + AC(\overline{AB + AC}) \\ &= AB + AC(\overline{AB} \cdot \overline{AC}) \\ &= AB + AC(\bar{A} + \bar{B})(\bar{A} + \bar{C}) \\ &= AB + AC\bar{B}(\bar{A} + \bar{C}) = AB \end{aligned}$$

8. (a)

Input of D flip flop, $D_n = Q_n \oplus X$

For D flip flop output,

$$Q_{n+1} = D_n = Q_n \oplus X$$

Drawing truth table

X	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

So, $Q_{n+1} = Q_n$ for $X = 0$

and $Q_{n+1} = \bar{Q}_n$ for $X = 1$

$\therefore$ It imitates T flip flop

9. (d)

Given number in decimal form = 64

In binary form 0 1 0 0 | 0 0 0 0

In hexadecimal $(4\ 0)_{16}$

For BCD,

$(4)_{10} - (0100)_2$

$(6)_{10} - (0110)_2$

$(64)_{10} - (01100100)_{BCD}$

10. (c)

At pulse 1	Input :	0	1	1	0
	Output :	1	0	1	1
At pulse 2	Input :	1	0	1	1
	Output :	0	1	0	1
At pulse 3	Input :	0	1	0	1
	Output :	1	0	1	0
At pulse 4	Input :	1	0	1	0
	Output :	1	1	0	1

11. (b)

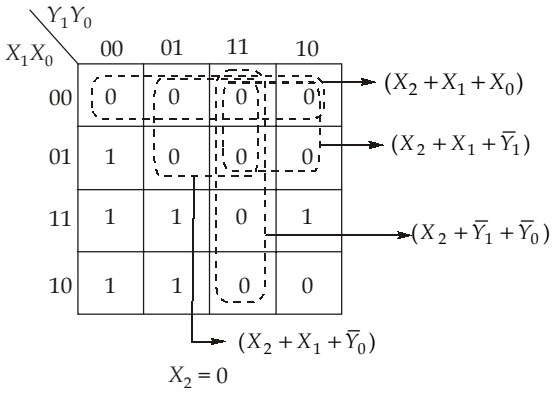
Dual slope A/D convertor has the highest accuracy among the given converters.

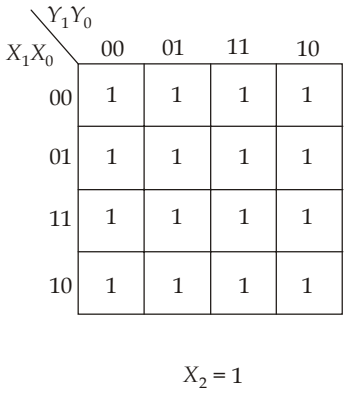
12. (c)

Now, $X > Y$ if

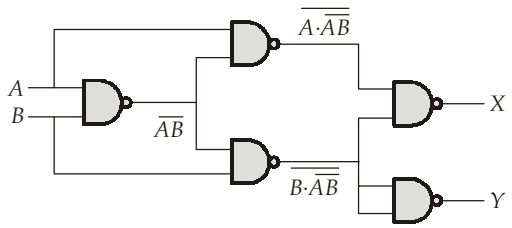
(a) $X_2 = 1$

(b) $X_2 = 0$ and $X_1X_0 > Y_1Y_0$





13. (c)



$$X = \overline{B}(A+B) + \overline{A}(A+B)$$
$$= A\overline{B} + \overline{A}B = A \oplus B$$
$$Y = B(\overline{AB})$$
$$= B(\overline{A} + \overline{B}) = \overline{A}B$$

The above circuit represents a half subtracter constructed using only NAND gates. Thus the truth table can be written as

A	B	Difference (X)	Borrow (Y)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

14. (d)

From figure, $Z = \overline{A}\overline{B}C + \overline{A}B + A\overline{B} + AB$

$$= \overline{A}(\overline{B}C + B) + A(\overline{B} + B)$$
$$= \overline{A}(\overline{B}C + B) + A$$
$$= (\overline{A} + A)(A + B + \overline{B}C)$$
$$= (A + [(B + \overline{B})(B + C)]$$
$$= A + (B + C)$$

Hence option (d) is correct

15. (c)

$$S = \left[\overline{(P+Q)}+\overline{(P+\overline{(P+Q)})}\right]\overline{(P+\overline{(P+Q)})}$$

Considering, $\overline{P+Q} = X$ and $\overline{P+\overline{(P+Q)}} = Y$

Then, $S = (X+Y)Y = XY + Y = Y$

$$S = \overline{P+\overline{(P+Q)}} = \overline{P}.(P+Q) = \overline{P}Q$$

So for, $S = 1,\ P = 0,\ Q = 1$

16. (b)

From the combinational logic.

Assuming D is input, Q_n is present state.

Q_{n+1} is the next state, then

$$R = \overline{D \oplus Q}\ , \qquad S = D \oplus Q$$

Characteristic equation of R – S flip flop

$$Q_{n+1} = S + \overline{R}Q_{in}$$

So,
$$\begin{aligned} Q_{n+1} &= (D \oplus Q_n) + \overline{(D \oplus Q_n)}Q_n \\ &= (D \oplus Q_n) + (D \oplus Q_n)Q_n \\ &= (D \oplus Q_n)[1 + Q_n] \\ &= D \oplus Q_n \\ &= D\overline{Q}_n + \overline{D}Q_n \end{aligned}$$

For, $D = 0\ ;\ Q_{n+1} = Q_n$

$D = 1\ ;\ Q_{n+1} = \overline{Q}_n$

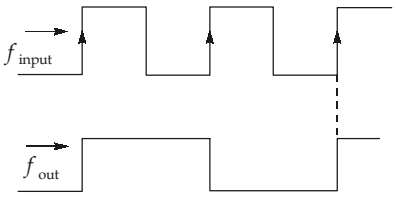
So the circuit functions as a T-flip flop.

17. (a)

From given sequential circuit

$$T = Q + \overline{Q}\ ,\ \text{So, } T = 1$$

So output toggles at every clock pulse



$\therefore$ Output frequency will be half of input frequency

$\therefore$ $a = 0.5 \qquad f_o = 0.5\, f_i$

18. (d)

In the given circuit

$D_0 = \overline{A}_1.\overline{A}_0,\ D_1 = \overline{A}_1.A_0,\ D_2 = A_1\overline{A}_0,\ D_3 = A_1A_0$

For first decoder,

$A_0 = a;\ A_1 = b$

$D_2 = b.\overline{a}$ and $D_3 = ab$

For second decoder,

$$A_1 = D_2.D_3 = b.\bar{a}.a.b = 0$$
$$A_0 = c$$

and $$D_0 = \bar{A}_1\bar{A}_0 + \bar{A}_1A_0 = \bar{A}_1 = 1$$

The value of $f(a, b, c) = D_0 + D_1 = 1 + 0 = 1$

19. (b)

Let initially output is 1

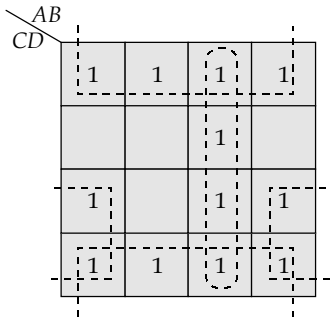
$\left(J_0 = 1,\ K_0 = 1,\ J_1 = \bar{Q}_2,\ K_1 = 1,\ J_2 = Q_1,\ K_2 = 1\right)$

then

CLK	Q_0	Q_1	Q_2	Q_0^+	Q_1^+	Q_2^+	J_0	K_0	J_1	K_1	J_2	K_2	Z
Initially	0	0	0										1
1	1	1	0	1	1	0	1	1	1	1	0	1	0
2	0	0	1	0	0	1	1	1	1	1	1	1	0
3	1	0	0	1	0	0	1	1	0	1	0	1	0
4	0	1	0	0	1	0	1	1	1	1	0	1	0
5	1	0	1	1	0	1	1	1	1	1	1	1	0
6	0	0	0	0	0	0	1	1	0	1	0	1	1

It is mod – 6 counter, so output Z will be 1 after every 6^{th} clock pulse.

20. (d)

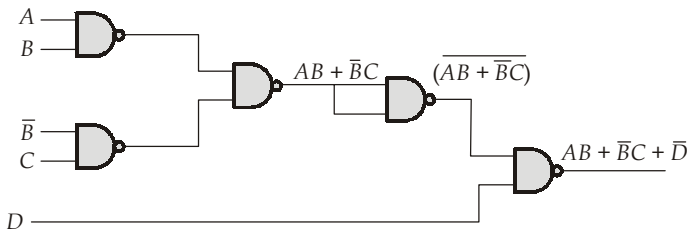


$$F = \bar{D} + \bar{B}C + AB$$

Alternatively

$$F = B\bar{D} + \bar{B}CD + ABC + AB\bar{C}D + \bar{B}\bar{D}$$
$$= \bar{D}(B + \bar{B}) + \bar{B}CD + ABC + AB\bar{C}D$$
$$= \bar{D} + \bar{B}CD + ABC + AB\bar{C}D$$
$$= \bar{D} + \bar{B}CD + AB(C + \bar{C}D)$$
$$= \bar{D} + \bar{B}CD + AB[(C + \bar{C})(C + D)]$$
$$= \bar{D} + (\bar{B}C + AB)D + ABC$$
$$= (\bar{D} + D)(\bar{D} + \bar{B}C + AB) + ABC$$
$$F = \bar{D} + \bar{B}C + AB$$

Now realization



Hence required number of NAND gates : 5

21. (b)

We have the logic function,

$$Z = AB + BC + CA$$

For the function, we form the K-map as shown below:

A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$\therefore$ $Z(A, B, C) = \Sigma m(3, 5, 6, 7)$

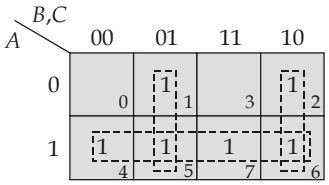
Therefore, during implementation of the function Z-using 8 to 1 MUX, inputs I_3, I_5, I_6 and I_7 will be at high logic (1) and rest inputs remain at logic (0).

Hence option (b) is correct.

22. (a)

	A	B	C	X
0	0	0	0	0
1	0	0	1	1
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

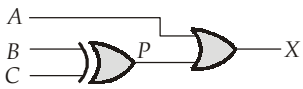
$X(A, B, C) = \Sigma m(1, 2, 4, 5, 6, 7)$



$$X = A + \overline{B}C + B\overline{C}$$
$$= A + B \oplus C$$

Alternate Solution:

Consider the circuit of option a



1. For $B = C$

$$P = B \oplus C = 0$$

and $$X = A + 0 = A$$

i.e. output X will equal to A when control input B and C are same:

2. For $B \neq C$

$$P = B \oplus C = 1$$

and $$X = A + 1 = 1$$

i.e. X will remain high when B and C are different. Hence the circuit meets both requirements.

23. (b)

In ripple counter, total delay time is

$$T_c = nt_d$$

Where, n = number of bits

Here, $n = 4$

and t_d = 10 ns (delay of each FF)

So, we get the worst case delay in ripple counter as

$$T_c = 4 \times 10 \text{ ns} = 40 \text{ ns}$$

(or) $$R = 40 \text{ ns}$$

In synchronous counter, all FF's are clocked simultaneously. So its worst delay will be equal to delay of one FF, i.e.

$$T_c = 10 \text{ ns}$$

(or) $$S = 10 \text{ ns}$$

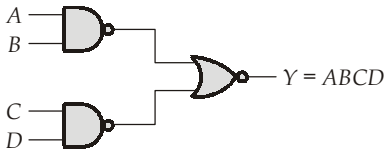
24. (b)

To implement the given function using NAND and NOR gates, we rewrite the given function as

$$Y = ABCD = \overline{\overline{ABCD}}$$

$$= \overline{\overline{AB} + \overline{CD}}$$

So the equivalent circuit for the Boolean function is



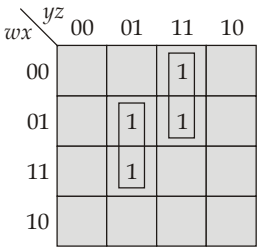
Therefore, two NAND gates and one NOR gate is required to implement $Y = ABCD$.

25. (b)

From the given circuit we obtain the expression for the output X as:

$$X = x\bar{y}z + \bar{w}xz + \bar{w}yz$$

Drawing the K-map for above expression:



By grouping the 1's in K-map, we get the minimized expression as,

$$X = x\bar{y}z + \bar{w}yz$$

$\therefore$ $\bar{w}xz$ i.e. gate-2 is redundant.

26. (d)

From the circuit diagram, we deduce that LED will glow when Z = low (0) and Z will be low only when X or Y or both will be high. Now, we consider the different input conditions as

1. For $A = B = 1$;

$X = 1$ and $Y = 0$

$\Rightarrow$ $Z = 0$; LED glows

2. For $A = B = 0$;

$X = 0$ and $Y = 1$

$\Rightarrow$ $Z = 0$; LED glows

3. For $A = 0$. $B = 1$;

$X = 0$ and $Y = 0$

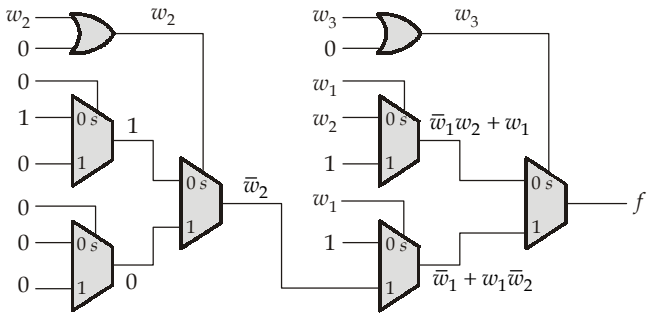
$\Rightarrow$ $Z = 1$; LED does not glows

4. For $A = 1$, $B = 0$;

$X = 0$ and $Y = 0$

$\Rightarrow$ $Z = 1$; LED does not glows

27. (c)



From the circuit, we obtain the output function as

$$\begin{aligned} f &= \bar{w}_3(w_1 + \bar{w}_1 w_2) + w_3(\bar{w}_1 + w_1\bar{w}_2) \\ &= \bar{w}_3(w_1 + w_2) + w_3(\bar{w}_1 + \bar{w}_2) \\ &= \bar{w}_3 w_1 + \bar{w}_3 w_2 + w_3\bar{w}_1 + w_3\bar{w}_2 \\ &= (w_2 \oplus w_3) + (w_1 \oplus w_3) \end{aligned}$$

28. (b)

In the given circuit, the output Z is

$$Z = \overline{(\bar{A} + \bar{B})} = AB$$

Truth table is as given below:

X	$B \oplus X$ J_A	$B\bar{X}$ K_A	AX J_B	AX K_B	A	B	Z	
–	–	–	–	–	0	0	0	
0	0	0	0	0	0	0	0	
1	1	0	0	0	1	0	0	
1	1	0	1	1	1	1	1	Initial
0	1	1	0	0	0	1	0	
0	1	1	0	0	1	1	1	

Hence the sequence of output Z is 00101.

29. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

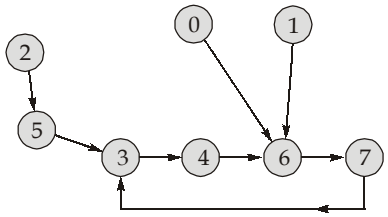
$\therefore$ $Y = Q_2 \oplus Q_1 \oplus Q_0$

$= 1 \oplus 0 \oplus 1 = 0$

30. (d)

Test for Lockout

Present State			Present Input						Nest State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1	1	0	1	1	1	0
0	0	1	1	1	1	1	0	1	1	1	0
0	1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	1	1	0	0	0	0	1	1



Hence, the counter does not enter into lockout state.

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