

CLASS TEST

S.No. : 03 LS1_EE_S_240819

Digital Electronics



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CLASS TEST 2019-2020

ELECTRICAL ENGINEERING

Digital Electronics

Date of Test : 24/08/2019

Answer Key

- | | | | | |
|--------|---------|-----------|---------|---------|
| 1. (b) | 7. (a) | 13. (b) | 19. (d) | 25. (a) |
| 2. (a) | 8. (b) | 14. (a) | 20. (a) | 26. (c) |
| 3. (a) | 9. (b) | 15. (b,d) | 21. (a) | 27. (b) |
| 4. (a) | 10. (a) | 16. (a) | 22. (a) | 28. (a) |
| 5. (c) | 11. (b) | 17. (c) | 23. (a) | 29. (a) |
| 6. (d) | 12. (a) | 18. (a) | 24. (b) | 30. (*) |

DETAILED EXPLANATIONS

1. (b)

$$\begin{aligned}
 0.514 \times 8 &= 4.112 \\
 0.112 \times 8 &= 0.896 \\
 0.896 \times 8 &= 7.168 \\
 0.168 \times 8 &= 1.344 \\
 0.344 \times 8 &= 2.752 \\
 \therefore (0.514)_{10} &= (0.40712)_8
 \end{aligned}$$

2. (a)

Since both PRESET & CLEAR are active low inputs, it will not affect to output status for a given condition. For J = 0, K = 0 input condition output of a JK FF holds. The previous value $Q^+ = Q$

3. (a)

For successive approximation type ADC, conversion time remains the same for any analogue input.

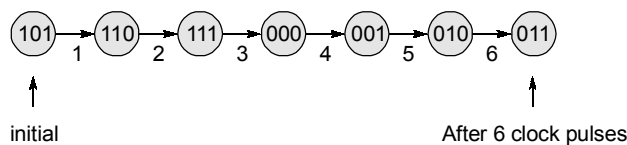
$$\begin{aligned}
 \therefore t_{conv} &= nT \\
 T &= \text{Clock period} \\
 n &= \text{Number of bit} \\
 T &= \frac{1}{1 \times 10^6} = 1 \mu s \\
 \therefore t_{con} &= 12 \times 1 = 12 \mu s
 \end{aligned}$$

5. (c)

$$\begin{aligned}
 \frac{64}{2} = 32, \quad \frac{32}{2} = 16, \quad \frac{16}{2} = 8 \\
 \frac{8}{2} = 4, \quad \frac{4}{2} = 2, \quad \frac{2}{2} = 1 \\
 \therefore \text{Total} = 32 + 16 + 8 + 4 + 2 + 1 = 63
 \end{aligned}$$

6. (d)

MOD-8 ripple up counter counts from 000 to 111

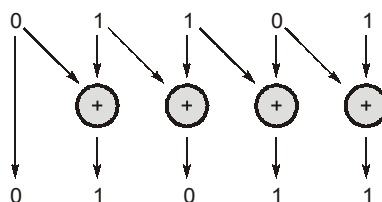


7. (a)

$$\text{Number of chips required} = \frac{\text{Required size of RAM}}{\text{Available size of RAM}} = \frac{64K \times 16}{16K \times 8} = 4 \times 2 = 8$$

9. (b)

Binary to gray code conversion



10. (a)
k-map simplification

A \ BC	00	01	11	10
0	1	1	1	0
1	0	0	1	1

POS expression is

$$F = (\bar{A} + B) \cdot (A + \bar{B} + C)$$

11. (b)
Octal number is obtained by 7's complement of 5264

$$7777 - 5264 = (2513)_8$$

$$\text{Binary equivalent of } (2513)_8 = (010\ 101001\ 011)_2$$

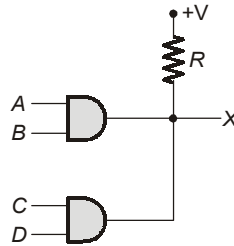
$$\text{Hexadecimal equivalent of } (010\ 101001\ 011)_2 = (54B)_{16}$$

12. (a)
Paralleling of two NAND gate at the input leads to a wire AND
∴ The logic expression at point x.

$$x = \overline{AB} \cdot \overline{CD}$$

Hence,

$$y = \bar{x} = \overline{\overline{AB} \cdot \overline{CD}} = AB + CD$$



13. (b)
Let n number of flip flop cascaded each having propagation delay of t_{pd} .
Frequency of operation

$$\frac{1}{nt_{pd}} \geq 10 \text{ MHz}$$

$$\therefore n \leq \frac{1}{t_{pd} \times 10 \text{ MHz}} \leq \frac{1}{12 \times 10^{-9} \times 10^7} \leq \frac{100}{12}$$

$$n = 8$$

For $n = 8$ MOD number of counter $2^8 = 256$

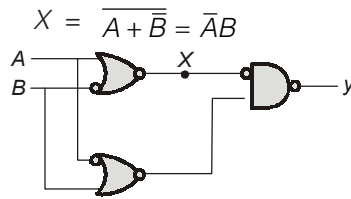
14. (a)
Drawing k-map

AB \ CD	00	01	11	10
00		1	1	
01	1			
11	1	1	1	1
10			1	1

From above k-map it is clear the minterms 4, 10 are grouped only once. Hence the essential prime implicants are $B\bar{C}, AC$.

16. (a)

From figure,



Similarly,

$$y = \overline{\bar{X} \cdot \bar{A} + B} = X + \overline{(\bar{A} + B)} = \bar{A}B + A \cdot \bar{B}$$

$$= A \oplus B$$

∴ X represent BORROW & y represents DIFFERENCE output.

17. (c)

$$\text{Step size} = \frac{\text{Full scale output}}{\text{Number of steps}} = \frac{5V}{2^8 - 1} = 19.607 \text{ mV}$$

For a digital input (10000010) = (130)₁₀ analogue output 130 × 19.607 = 2.549 V

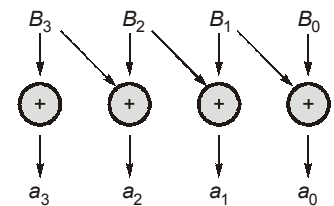
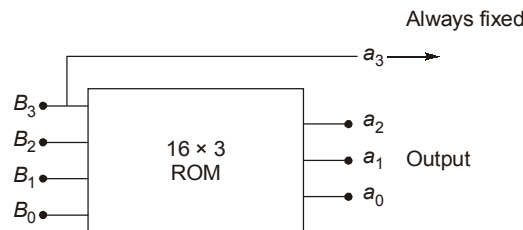
$$\text{Error} = \pm \frac{0.5 \times 5}{100} = 0.025$$

Expected range of output 2.524 – 2.574 V

18. (a)

Number of input = 4

∴ $a_3 = B_3$
 ∴ $a_2 = B_2 \oplus B_3$
 $a_1 = B_2 \oplus B_1$
 $a_2 = B_1 \oplus B_0$



Size of ROM requires $2^4 \times 3 = 16 \times 3$

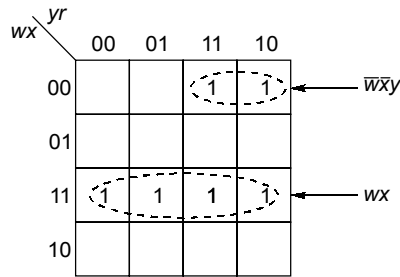
19. (d)

Initial state to be 1000.

CLK	A	B	C	D	X
X	1	0	0	0	0
1	0	1	0	0	1
2	1	0	1	0	1
3	1	1	0	1	0
4	0	1	1	0	0
5	0	0	1	1	0
6	0	0	0	1	1
7	1	0	0	0	0

Hence after 7 clock pulses SIPO shift register comes back to initial state.

20. (a)
k-map simplification



21. (a)
 MOD number of BCD counter = 10
 MOD number of n bit Johnson counter = $2n$
 MOD number of n bit ring counter = n
 \therefore Hence MOD number of given counter arrangement = $10 \times 6 \times 2 = 120$

$$f_0 = \frac{f_{clk}}{120}$$

$$f_{ck} = f_0 \times 120 = 24 \text{ kHz}$$

22. (a)
Output y will be high only if

$$J_2 = X = 1 \text{ and C has a low-to-HIGH transition}$$

X will be high only if

$A = 1$ and B has a LOW-to-HIGH transition.

From above two conditions, it is clear that output y will go high for the following sequence

A - B - C

Analysis:

$A = 1$ and B goes high, A rising edge of B will trigger flip-flop

$$\therefore X = 1 [J_1 = 1; K_1 = 0]$$

Now, C goes high. A rising edge of C will trigger flip-flop 2

$$\therefore Y = 1 [J_2 = X = 1; K_2 = 0]$$

23. (a)
 $X - Y = X + 2s$ complement of Y .

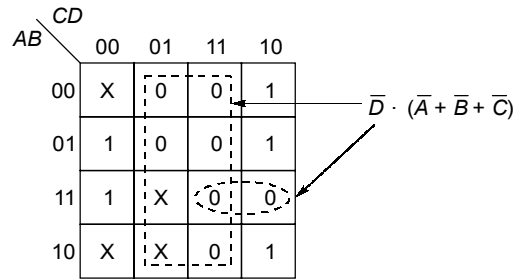
$$\begin{aligned} 2\text{'s complement of } Y &= 1\text{'s complement} + 1 \\ &= 0111100 + 1 = 0111101 \end{aligned}$$

$$\begin{aligned} X - Y &= \begin{array}{r} 1010100 \\ 0111101 \\ \hline 1001001 \end{array} \end{aligned}$$

Discard carry, $X - Y = 0010001$

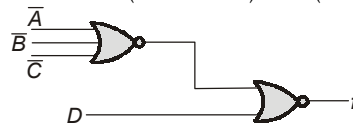
24. (b)

Drawing k-map



POS form is suitable for NOR gate implementation

$$f = \overline{D}(\overline{A+B+C}) = \overline{D(\overline{A+B+C})} = \overline{D + \overline{A+B+C}}$$



NOT required 1 NOR gate.

∴ Total 5 NOR gates required.

25. (a)

From figure

$$y = \overline{Q}A + Q\overline{B}$$

Q - Present state

∴

$$Q^+ = D = y = \overline{Q}A + Q\overline{B}$$

Q⁺ = Next state

For A = 1, B = 1

$$Q^+ = \overline{Q}, 1 + Q, 0 = \overline{Q}$$

For A = 1, B = 0

$$Q^+ = \overline{Q}, 1 + Q, 1 = 1$$

26. (c)

Select line ABC	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇
\overline{D}	0	(2)	4	6	(8)	10	12	(14)
D	(1)	3	5	(7)	(9)	(11)	13	(15)
	D	\overline{D}	0	D	1	D	0	1

27. (b)

Analysis of the circuit,

$$J = \overline{Q} \oplus x, \quad k = \overline{J}$$

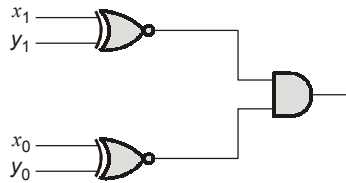
x	Q	J	K	Q ⁺
0	0	1	0	1
0	1	0	1	0
1	0	0	1	0
1	1	1	0	1

∴

$$Q(t+1) = x \odot Q(t)$$

28. (a)

Two numbers will be equal if $y_1 = x_1$ and $y_0 = x_0$
 Ex-NOR logic gate outputs 1(HIGH) for the same input.
 \therefore Above condition will be implement as



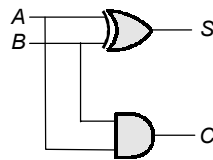
29. (a)

8 bit binary parallel adder can be implemented by 7FA + 1HA

FA = Full adder

HA = Half adder

Half adder



HA requires 1 Ex-OR & 1 AND gate.

1 HA costs $2 + 1 = 3$ units

Full adder requires 2HA & 1 OR gate

\therefore We total require, 15HA & 7OR gate

$$\begin{aligned} \therefore \text{Total cost} &= 15 \times \text{cost of HA} + 7 \times \text{cost of OR gate} \\ &= 15 \times 3 + 7 \times 1 \\ &= 52 \text{ units} \end{aligned}$$

30. (*)

Question data insufficient.

