

CLASS TEST

S.No. : 04 BS_CS_S_190719

Digital Logic



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CLASS TEST 2019-2020

COMPUTER SCIENCE & IT

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ANSWER KEY > Digital Logic

1. (b)	7. (c)	13. (a)	19. (b)	25. (c)
2. (d)	8. (b)	14. (c)	20. (c)	26. (b)
3. (a)	9. (b)	15. (a)	21. (d)	27. (b)
4. (a)	10. (d)	16. (d)	22. (a)	28. (a)
5. (c)	11. (d)	17. (d)	23. (a)	29. (c)
6. (b)	12. (c)	18. (b)	24. (c)	30. (b)

DETAILED EXPLANATIONS

1. (b)

Converting into decimal,

$$(2)_3 = 2 \times 3^0 = 2$$

$$(3)_4 = 3 \times 4^0 = 3$$

$$(14)_5 = 1 \times 5^1 + 4 \times 5^0 = 9$$

$$(15)_6 = 1 \times 6^1 + 5 \times 6^0 = 11$$

2. (d)

$$N = 5,$$

$$t_{pd} = 2 \text{ nsec}$$

$$T = 2 N t_{pd}$$

⇒

$$T = 2 \times 5 \times 2 \times 10^{-9} \\ = 20 \text{ nsec}$$

3. (a)

$$Y = \bar{S}_0 \bar{S}_1 I_0 + S_0 \bar{S}_1 I_1 + \bar{S}_0 S_1 I_2 + S_0 S_1 I_3$$

$$= \bar{A} \bar{B} C + \bar{A} B \cdot 1 + A \bar{B} \cdot 0 + A B \cdot \bar{C}$$

$$= \bar{A} \bar{B} C + \bar{A} B \cdot (C + \bar{C}) + A B \bar{C}$$

$$= \bar{A} \bar{B} C + \bar{A} B C + \bar{A} B \bar{C} + A B \bar{C}$$

$$\approx 001, 011, 010, 110$$

$$f(A, B, C) = \Sigma m(1, 2, 3, 6)$$

4. (a)

 M = total number of states n = total number of FF's $M = 2^n$; Binary counter $M \leq 2^n$; Non-Binary counter

5. (c)

Range of signed 1's complement number is $-2^{n-1} + 1$ to $2^{n-1} - 1$.

6. (b)

$$Y_1 = \bar{c}$$

$$F = Y_2 = \bar{d} Y_1 + dc$$

$$= \bar{d} \bar{c} + dc$$

$$= c \odot d$$

7. (c)

Output of the 4 : 1 MUX circuit in Figure A is

$$Y = I_0 \bar{A} \bar{B} + I_1 \bar{A} B + I_2 A \bar{B} + I_3 A B$$

Output of the circuit in Figure B is

$$Y = A \oplus B \oplus C = \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} \bar{C} + A B C$$

On comparison

$$\begin{aligned} I_0 &= C \\ I_1 &= \bar{C} \\ I_2 &= \bar{C} \\ I_3 &= C \end{aligned}$$

8. (b)

Simplifying boolean expression:

$$\begin{aligned} F &= C(B + C)(A + B + C) \\ &= (CB + CC)(A + B + C) \\ &= (CB + C)(A + B + C) \\ &= C(1 + B)(A + B + C) \\ &= C(A + B + C) \\ &= AC + BC + C \\ &= C(1 + A + B) \\ &= C \end{aligned}$$

9. (b)

$$\begin{aligned} Y &= I_0 \cdot \bar{S}_1 \bar{S}_0 + I_1 \cdot \bar{S}_1 S_0 + I_2 \cdot S_1 \bar{S}_0 + I_3 S_1 S_0 \\ Y &= A\bar{B} + (1)B = B + A\bar{B} = A + B \end{aligned}$$

10. (d)

11. (d)

Counter output =

	S ₂ A ₃	S ₁ A ₂	E A ₁	S ₀ A ₀		
1 st clock	1	1	1	1	-15	I ₇
2 nd	1	1	1	0	-14	I ₆
3 rd	1	1	0	1	-13	0
4 th	1	1	0	0	-12	0
5 th	1	0	1	1	-11	I ₅
6 th	1	0	1	0	-10	I ₄

For 1st and 2nd clock pulses, enable is 1

$$\begin{aligned} & \quad S_2 \quad S_1 \quad S_0 \\ \text{1st clock pulse} & - \quad 1 \quad 1 \quad 1 \rightarrow 1_7 \\ \text{2nd clock pulse} & - \quad 1 \quad 1 \quad 0 \rightarrow 1_6 \end{aligned}$$

For 3rd and 4th clock pulse, enable is 0,

So, Y is 0

12. (c)

The characteristics table with J, K, Q_n, Q_{n+1} and the excitation table for S and R is shown below –

J	K	Q _n	Q _{n+1}	S	R
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

The K-map for S and R is shown as –
For S ,

$$S(J, K, Q_n) = \Sigma m(4, 6) + d(1, 5) = J\bar{Q}_n$$

	KQ_n			
J	00	01	11	10
0		×		
1	1	×		1

$$S = J\bar{Q}_n$$

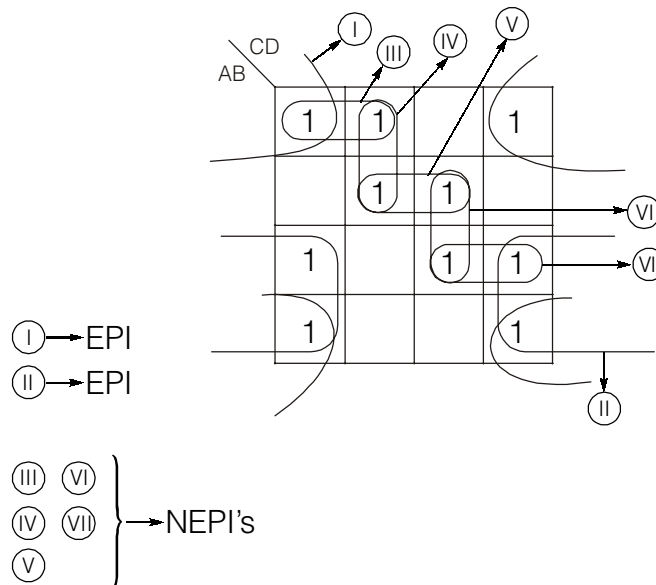
For R ,

$$R(J, K, Q_n) = \Sigma m(3, 7) + d(0, 2) = KQ_n$$

	KQ_n			
J	00	01	11	10
0	×		1	×
1			1	

$$R = KQ_n$$

13. (a)



EPI = Essential Prime Implicant [which cover a minterm not covered by any other prime implicants]
NEPI = Non Essential Prime Implicant. Number of EPI's = 2, number of NEPI's = 5.

14. (c)

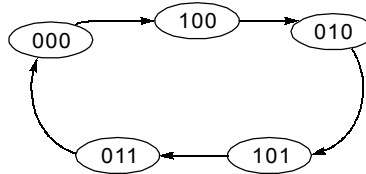
Plotting the K-map for $Y = A\bar{B} + B\bar{C}$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	0	1	3	1 ₂
A	1 ₄	1 ₅	7	1 ₆

So, $\Sigma m(2, 4, 5, 6) = \text{SOP}$
 $\Sigma \pi(0, 1, 3, 7) = \text{POS}$

15. (a)

Clock	Present state			FF2		FF1	FF0
	Q ₂	Q ₁	Q ₀	J ₂ = $\overline{Q_0}$, K ₂ = 1		D ₁ = Q ₂	T ₀ = Q ₁
	0	0	0	1	1	0	0
1	1	0	0	1	1	1	0
2	0	1	0	1	1	0	1
3	1	0	1	0	1	1	0
4	0	1	1	0	1	0	1
5	0	0	0				



The number of used states = 5
∴ modulus value = 5

16. (d)

$$\overline{Z} = (P + A)(Q + \overline{A})$$

$$\overline{Z} = PQ + AQ + \overline{A}P$$

If

$$Z = \overline{A} + B$$

$$\overline{Z} = \overline{\overline{A} + B} = A\overline{B}$$

$$Q = \overline{B}, P = O$$

17. (d)

Q ₂	Q ₁	Q ₀	Cr
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1

So the output Q₂ can be directly connected to clear.
∴ Best architecture is a wire connection.

18. (b)

Clock	S ₁ S ₀ ← MUX inputs	Q ₃ Q ₂ Q ₁ Q ₀				
		Q ₃	Q ₂	Q ₁	Q ₀	
		0	0	1	1	← Initial state
1	0	0	0	0	1	
2	0	0	0	0	0	
3	1	1	0	0	0	
4	1	1	1	0	0	
5	1	1	1	1	0	
6	1	1	1	1	1	
7	0	0	1	1	1	
8	0	0	0	1	1	

After 8 clock pulse.

19. (b)

Let the base be x , then

$$\begin{aligned} 292_{10} &= 1204_x \\ &= 1 \times x^3 + 2 \times x^2 + 0 \times x^1 + 4 \times x^0 \\ &= 292_{10} \\ &= x^3 + 2x^2 + 4 \\ &= 6 \text{ (By substitution)} \end{aligned}$$

20. (c)

A	B	J	K	Q_{n+1}
0	0	1	0	1
0	1	1	1	\bar{Q}_n
1	0	1	0	1
1	1	0	1	0

$$Q_{n+1} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B\bar{Q}_n$$

$$\begin{aligned} Q_{n+1} &= \bar{B} + \bar{A}B\bar{Q}_n \\ &= \bar{B} + \bar{A}\bar{Q}_n \end{aligned}$$

21. (d)

	FFD		FFT	
	Q_D	Q_T	$D = \bar{Q}_T$	$T = \bar{Q}_T \oplus Q_D$
Clock pulse	0	0	1	1
1	1	1	0	1
2	0	0	1	1
3	1	1	0	1
4	0	0		

So, output will either be 00 or 11 and never 10.

22. (a)

State table can be drawn from state diagram

Present state	Input	Next state
Q_n	X	Q_{n+1}
0	1	0
0	0	1
1	1	0
1	0	0

$$Q_{n+1} = \overline{Q_n + X} \quad (Q_{n+1} \text{ represent output of NOR gate})$$

23. (a)

In the circuit, we have

$$D_0 = \overline{Q_1 Q_2} = \overline{Q_1} + \overline{Q_2}$$

$$D_1 = Q_0$$

$$D_2 = Q_1$$

The truth table for the circuit is obtained below:

CLK number	Present State			Inputs			Next State		
	Q ₂	Q ₁	Q ₀	D ₂	D ₁	D ₀	Q ₂ ⁺	Q ₁ ⁺	Q ₀ ⁺
initial	0	0	0	-	-	-	-	-	-
1	0	0	0	0	0	1	0	0	1
2	0	0	1	0	1	1	0	1	1
3	0	1	1	1	1	1	1	1	1
4	1	1	1	1	1	0	1	1	0

After 4 clock pulses, output is Q₂ Q₁ Q₀ = 110

24. (c)

For 1st 4 × 1 MUX,

$$I_0 = C$$

$$I_1 = \overline{C}$$

$$I_2 = \overline{C}$$

$$I_3 = C$$

$$\begin{aligned} \text{So, } f_1(A, B, C) &= \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC \\ &= \Sigma_m(1, 2, 4, 7) \end{aligned}$$

For 2nd 4 × 1 MUX,

$$I_0 = C$$

$$I_1 = 1$$

$$I_2 = 0$$

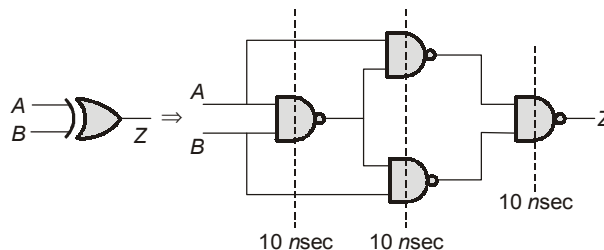
$$I_3 = C$$

$$\begin{aligned} \text{So, } f_2(A, B, C) &= \overline{A}\overline{B}C + \overline{A}B \cdot 1 + A\overline{B} \cdot 0 + AB \cdot C \\ &= \Sigma_m(1, 2, 3, 7) \end{aligned}$$

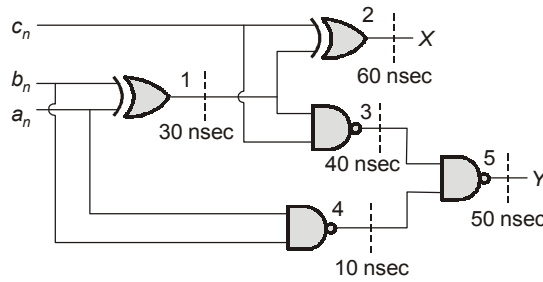
So, $f_1(A, B, C)$ represents the difference of full subtractor while $f_2(A, B, C)$ represents the borrow of full subtractor.

25. (c)

An Ex-OR gate can be represented as



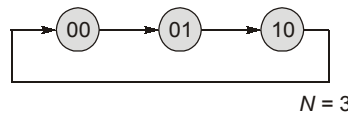
So, for EX-OR gate, it will take 30 nsec to get the output.



So, to get the output Y, it will take 50 nsec.

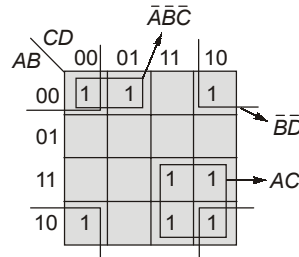
26. (b)

CLK	FFO				FFI	
	Q_1	Q_0	$J_0 = \bar{Q}_1$	$K_0 = 1$	$J_1 = Q_0$	$K_1 = \bar{Q}_0$
	0	0	1	1	0	1
1	0	1	1	1	1	0
2	1	0	0	1	0	1
3	0	0				



27. (b)

The k-map has to be rearranged as



$$F = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{D} + AC$$

28. (a)

For the given 4×1 MUX, 'A' and 'B' are select lines and 'C' be the input

	I_0	I_1	I_2	I_3
\bar{C}	0	2	4	6
C	1	3	5	7
	1	0	1	0

So,

$$I_0 = 1 = a$$

$$I_1 = 0 = b$$

$$I_2 = 1 = c$$

$$I_3 = 0 = d$$

So,

$$a \oplus d = b \oplus c = 1$$

So, output of NAND gate is 0 i.e. MUX 'E' connected to '0'.

The MUX is in disable state. MUX is having active high enable, but $E = 0$, so that MUX is in disable state. Hence MUX output Z is equal to '0'.

29. (c)

Number of flip-flops for mod-16 ripple counter = 4

$$\text{Maximum clock frequency} = \frac{10^9}{4\rho} \text{ Hz} = 5 \text{ MHz}$$

$$\rho = \frac{10^9}{4 \times 5 \times 10^6} = \frac{1000}{20}$$

$$\rho = 50$$

30. (b)

$$X = (A \oplus B)(B \odot C)C$$

to get $X = 1$,

$$A \oplus B = 1$$

$$B \odot C = 1$$

$$C = 1$$

for $(ABC) = (101) \Rightarrow A \oplus B = 1, B \odot C = 0, C = 1 \Rightarrow X = 0$

for $(ABC) = (011) \Rightarrow A \oplus B = 1, B \odot C = 1, C = 1 \Rightarrow X = 1$

for $(ABC) = (111) \Rightarrow A \oplus B = 0, B \odot C = 1, C = 1 \Rightarrow X = 0$

for $(ABC) = (110) \Rightarrow A \oplus B = 0, B \odot C = 0, C = 0 \Rightarrow X = 0$

