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DIGITAL ELECTRONICS

ELECTRONICS ENGINEERING

Date of Test : 23/09/2022

ANSWER KEY ➤

1.	(d)	7.	(c)	13.	(a)	19.	(d)	25.	(b)
2.	(d)	8.	(b)	14.	(a)	20.	(a)	26.	(d)
3.	(c)	9.	(c)	15.	(b)	21.	(d)	27.	(a)
4.	(b)	10.	(b)	16.	(c)	22.	(a)	28.	(b)
5.	(d)	11.	(a)	17.	(b)	23.	(a)	29.	(a)
6.	(b)	12.	(d)	18.	(a)	24.	(d)	30.	(a)

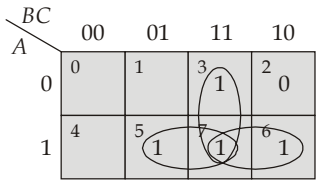
DETAILED EXPLANATIONS

1. (d)

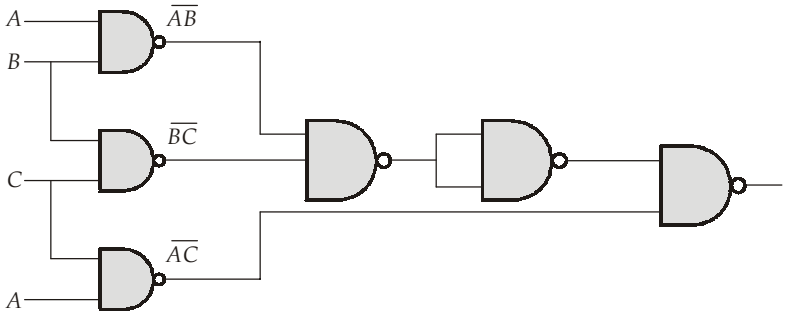
Let F be the majority function,

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$F(A, B, C) = \Sigma m\{3, 5, 6, 7\}$



$F = AC + AB + BC$



$\overline{\overline{AB} \cdot \overline{BC} \cdot \overline{AC}} = AB + BC + AC$

Hence, 6 NAND gates are required to realize the function.

2. (d)

$$F(A, B, C, D) = A\overline{B} + BD + \overline{B}C\overline{D}$$
$$= \Sigma m(2, 5, 7, 8, 9, 10, 11, 13, 15)$$

To implement the four variable function F, we need '$2^4 - 1$' number of 2×1 multiplexer.

$\therefore$ $2^4 - 1 = 15$ 2×1 multiplexer are required to implement F.

3. (c)

For half subtractor, Difference, $D = A \oplus B$

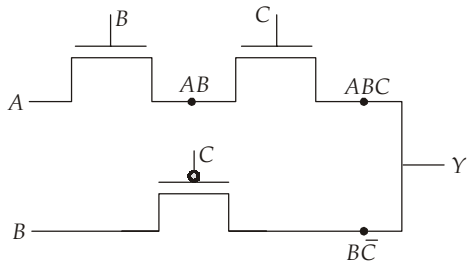
$$\text{Borrow} = \overline{A}B$$

$\therefore$ output of 4×1 multiplexer,

$$Y = \overline{S}_1\overline{S}_0(0) + \overline{S}_1S_0(1) + S_1\overline{S}_0(1) + S_1S_0(D)$$

$$Y = (\overline{A \oplus B})(\overline{\bar{A}B})(0) + (\overline{A \oplus B})(\bar{A}B)(1) + (A \oplus B)(\overline{\bar{A}B})(1) +$$
$$(A \oplus B)(\bar{A}B)(A \oplus B)$$
$$= (\overline{A \oplus B})(\bar{A}B) + (A \oplus B)(A + \bar{B}) + (A \oplus B)(\bar{A}B)$$
$$= \bar{A}B + (A \oplus B)(A + \bar{B})$$
$$= \bar{A}B + (\bar{A}B + A\bar{B})(A + \bar{B})$$
$$Y = \bar{A}B + A\bar{B}$$

4. (b)



$$Y = ABC + B\bar{C}$$
$$= B(AC + \bar{C})$$
$$= B(A + \bar{C})$$

5. (d)

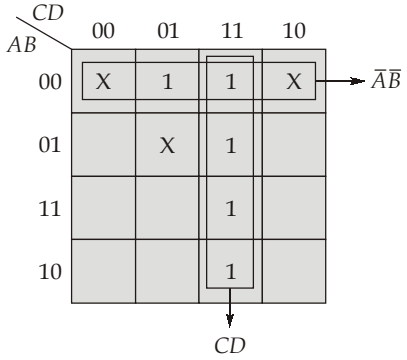
$$F = \overline{(X \odot Y)Z} = \overline{(XY + \bar{X}\bar{Y})Z}$$
$$F = (\overline{XY + \bar{X}\bar{Y}}) + \bar{Z} = (\overline{XY})\,(\overline{\bar{X}\bar{Y}}) + \bar{Z}$$
$$F = (\bar{X} + \bar{Y})\,(X + Y) + \bar{Z} = \bar{X}Y + X\bar{Y} + \bar{Z}$$

6. (b)

15's complement is equivalent to $(r - 1)$'s complement , thus

$$\begin{array}{r} F\ F\ F \\ -\,B\ B\ C \\ \hline (4\ 4\ 3)_{16} \end{array}$$

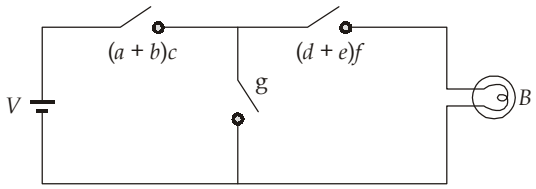
7. (c)



$$Y = CD + \bar{A}\bar{B}$$

8. (b)

The given figure can be reduced as



g	B
0	$(a+b)c\,(d+e)f$
1	0

$$\therefore \quad B = \bar{g}(a+b)(d+e)fc$$

9. (c)

Figure of merit of an IC is = Average power dissipation × Average propagation delay
$= 5 \times 10^{-3} \times 10 \times 10^{-9} = 50$ pico Joules

10. (b)

From 0 to $(511)_{10}$ total number of decimal numbers are 512, so for this count we require ($2^9 = 512$) 9 flip-flops.

Hence, 9 + 1 = 10 flip-flops are required to count from 0 to 512.

11. (a)

B_4	B_3	B_2	B_1	X_4	X_3	X_2	X_1
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

$$X_4 = \Sigma m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$$
$$X_3 = \Sigma m(1, 2, 3, 4, 9) + d(10, 11, 12, 13, 14, 15)$$
$$X_2 = \Sigma m(0, 3, 4, 7, 8) + d(10, 11, 12, 13, 14, 15)$$
$$X_1 = \Sigma m(0, 2, 4, 6, 8) + d(10, 11, 12, 13, 14, 15)$$

$\therefore$ The minimal expressions are:

$$X_4 = B_4 + B_3B_2 + B_3B_1$$
$$X_3 = B_3\overline{B_2}\,\overline{B_1} + \overline{B_3}B_1 + \overline{B_3}B_2$$
$$X_2 = \overline{B_2}\,\overline{B_1} + B_2B_1$$
$$X_1 = \overline{B_1}$$

12. (d)

From the given CMOS logic,

$$\overline{F} = ab + bd + bc$$

$$\overline{F} = b(a + d + c)$$

$$F = \overline{b} + \overline{a}\,\overline{d}\,\overline{c}$$

ab \ cd	00	01	11	10
00	1	1	1	1
01	1	0	0	0
11	0	0	0	0
10	1	1	1	1

$\therefore$ Pull-up network has maxterms as $\pi M(5, 6, 7, 12, 13, 14, 15)$

13. (a)

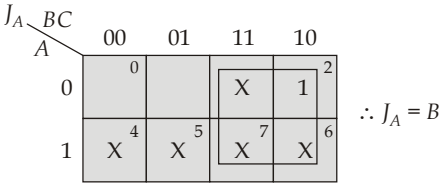
Excitation table for *JK* flip flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

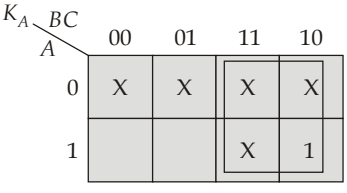
Excitation table for given counter

Present state			Next state			Flip-flop Outputs					
A	B	C	A^+	B^+	C^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

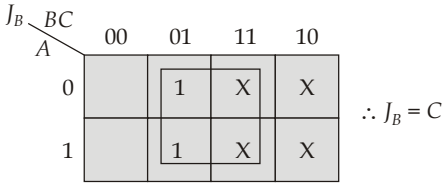
($\because$ given 3 and 7 are unused states so consider them as don't cares).



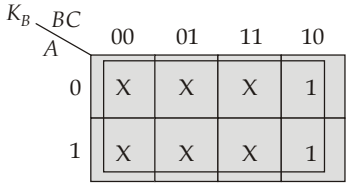
$\therefore J_A = B$



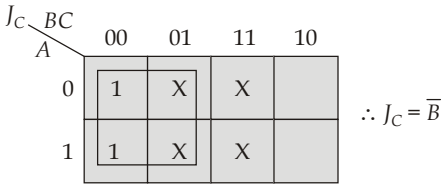
$\therefore K_A = B$



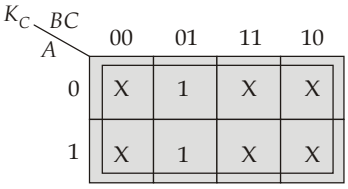
$\therefore J_B = C$



$\therefore K_B = 1$

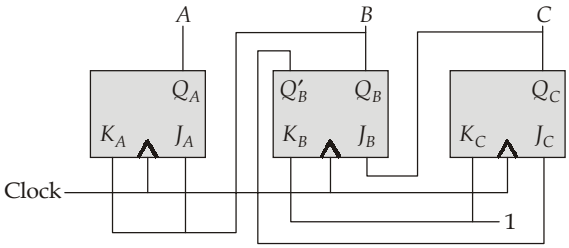


$\therefore J_C = \overline{B}$



$\therefore K_C = 1$

$\therefore$ The logic diagram of counter.



14. (a)

Quantization error in a DAC is given by $V_{LSB}/2$.

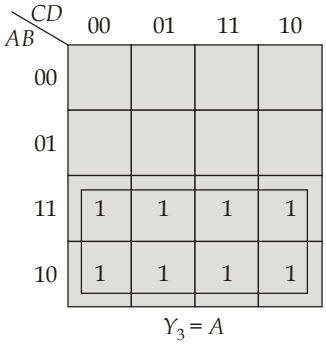
$$\frac{V_{FS}}{2(2^n - 1)} \times 100 < (0.4)\ V_{FS}$$

$$\frac{1}{2^n - 1} < 0.008$$

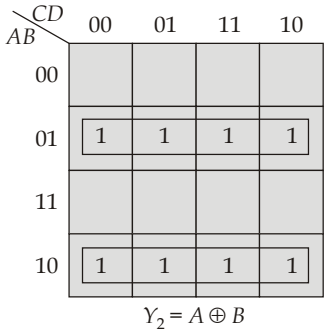
$$2^n - 1 > 125$$

$\therefore$ $n_{min.} = 7$

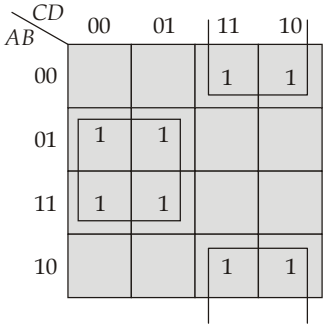
15. (b)



$Y_3 = A$

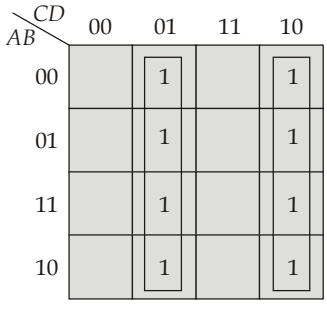


$Y_2 = A \oplus B$



$Y_1 = C\overline{B} + \overline{C}B$

$= C \oplus B$



$Y_0 = \overline{C}D + C\overline{D}$

$= C \oplus D$

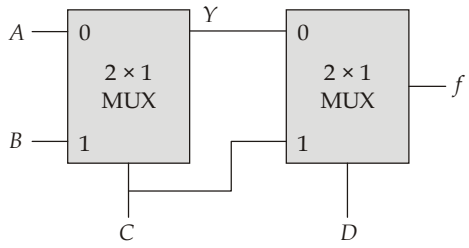
$Y_3 = A$

$Y_2 = A \oplus B$

$Y_1 = B \oplus C$

$Y_0 = C \oplus D$

16. (c)



$$Y = A\bar{C} + BC$$

$$f = Y\bar{D} + CD$$

$$f = (A\bar{C} + BC)\bar{D} + CD = A\bar{C}\bar{D} + BC\bar{D} + CD$$

CD / AB	00	01	11	10
00			1	
01			1	1
11	1		1	1
10	1		1	

$\therefore$ $f(A, B, C, D) = \Sigma m(3, 6, 7, 8, 11, 12, 14, 15)$

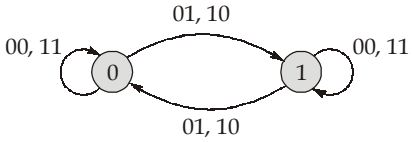
17. (b)

Register-*A* and Register-*B* together form a cyclic register, and so, contents in Register-*A* and *B* appears after 7-clock pulses

Clock pulse	Register-*A*	Register-*B*
7	1 1 0 1	0 1 0
8	0 1 1 0	1 0 1
9	1 0 1 1	0 1 0
10	0 1 0 1	1 0 1

18. (a)

Present State	Inputs		Next State
A	x	y	A^+
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



19. (d)

PS		NS		FF inputs	
Q_A	Q_B	Q_A	Q_B	J_B	k_B
0	0	1	1	1	x
1	1	1	0	x	1
1	0	0	1	1	x
0	1	0	0	x	1

On solving for J_B and k_B

Q_A \ Q_B	0	1
0	1	x
1	1	x

$J_B = 1$

Q_A \ Q_B	0	1
0	x	1
1	x	1

$k_B = 1$

20. (a)

$$P = \bar{B}\bar{C}A + \bar{B}C\bar{A} + B\bar{C}\bar{A} + BCA$$

$$= \bar{A}[B\bar{C} + \bar{B}C] + A[BC + \bar{B}\bar{C}]$$

$$= \bar{A}[B \oplus C] + A[\overline{B \oplus C}]$$

$$P = A \oplus B \oplus C$$

$$P(A, B, C) = \Sigma m(1, 2, 4, 7)$$

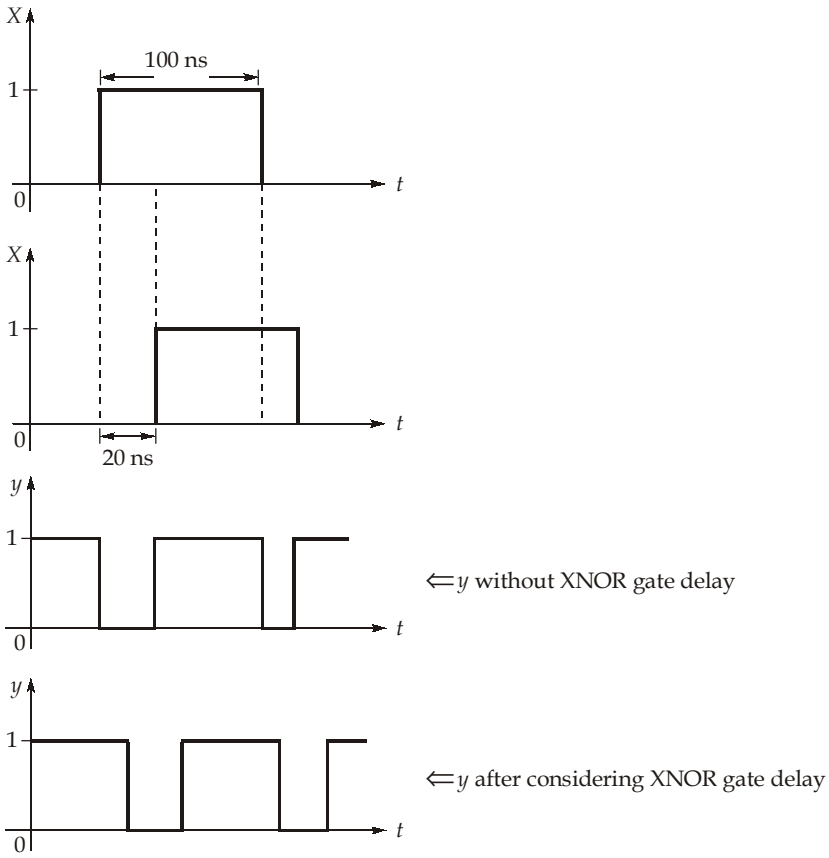
$$Q = \bar{B}\bar{C} \cdot 0 + \bar{B}C\bar{A} + B\bar{C}\bar{A} + BC$$

$$= \bar{B}C\bar{A} + B\bar{C}\bar{A} + BC(A + \bar{A})$$

$$= \bar{B}C\bar{A} + B\bar{C}\bar{A} + ABC + \bar{A}BC$$

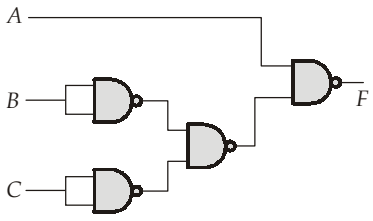
$$Q(A, B, C) = \Sigma m(1, 2, 3, 7)$$

21. (d)



22. (a)

$$F = \overline{A(B+C)}$$



23. (a)

$V_{out} = -9.375$ V when $|V_{out}| = 9.375$ V

maximum output means all bits are 1

i.e., $b_0 b_1 b_2 \ldots\ldots b_{n-1} = 1111 \ldots\ldots 1$

Since its an inverting amplifier,

$$V_{out} = -V\left(\frac{R}{R}b_0 + \frac{R}{2R}b_1 + \frac{R}{4R}b_2 + \frac{R}{8R}b_3 \ldots\ldots + \frac{R}{2^{n-1}R}b_{n-1}\right)$$

$$-9.375 = -5\left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \ldots\ldots + \frac{1}{2^{n-1}}\right)$$

$$1.875 = \frac{\left(1-\left(\frac{1}{2}\right)^n\right)}{1-\frac{1}{2}}$$

$$\frac{1}{2}\times 1.875 = 1-\left(\frac{1}{2}\right)^n$$

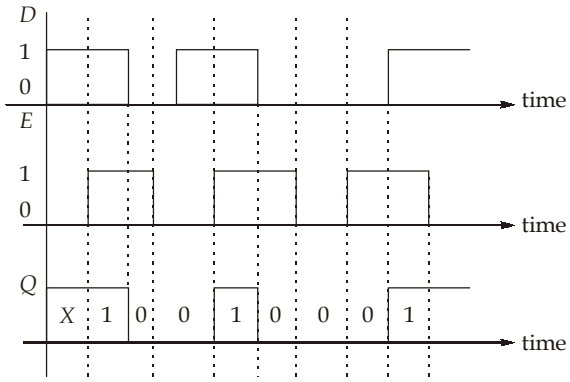
$$\left(\frac{1}{2}\right)^n = 1-\frac{1}{2}\times 1.875 = 0.0625 = \frac{1}{16}$$

so, $2^n = 16$

$n = 4$

24. (d)

D	E	Q	$\overline{Q}$
X	0	Q	$\overline{Q}$
0	1	0	1
1	1	1	0



25. (b)

For decoding any binary data, output must be high for that data (code) and this is possible in one 4-input AND gate, one inverter option only.

A decoder is a combinational circuit that converts n-bit binary coded data upto 2^n outputs.

26. (d)

From the given circuit, $F = ABC\overline{D} + ABEF$

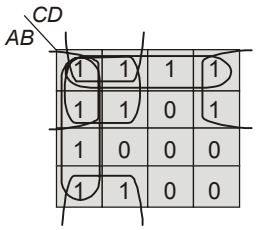
Sum-of-products form represents the sum (OR) of product (AND) terms having variables in complemented as well as in uncomplemented form. Here the diagram 'Z' contains the OR gate followed by the AND gates, which gives the output function F same as in the given figure M.

27. (a)

Using Truth table:

A	B	C	D	$S_1 \times S_2$	F
0	0	0	0	$0 \times 0 = 0 \le 2$	1
0	0	0	1	$0 \times 1 = 0 \le 2$	1
0	0	1	0	$0 \times 2 = 0 \le 2$	1
0	0	1	1	$0 \times 3 = 0 \le 2$	1
0	1	0	0	$1 \times 0 = 0 \le 2$	1
0	1	0	1	$1 \times 1 = 1 \le 2$	1
0	1	1	0	$1 \times 2 = 2 \le 2$	1
0	1	1	1	$1 \times 3 = 3 > 2$	0
1	0	0	0	$2 \times 0 = 0 \le 2$	1
1	0	0	1	$2 \times 1 = 2 \le 2$	1
1	0	1	0	$2 \times 2 = 4 > 2$	0
1	0	1	1	$2 \times 3 = 6 > 2$	0
1	1	0	0	$3 \times 0 = 0 \le 2$	1
1	1	0	1	$3 \times 1 = 3 > 2$	0
1	1	1	0	$3 \times 2 = 6 > 2$	0
1	1	1	1	$3 \times 3 = 9 > 2$	0

$\therefore$ $F =$



$$F = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{C}\bar{D} + \bar{A}\bar{D} + \bar{B}\bar{C}$$

28. (b)

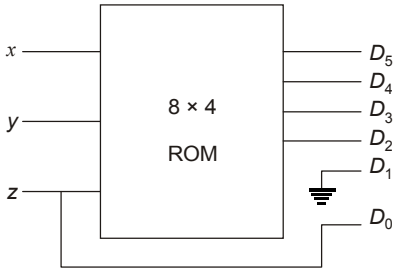
The ROM should have three inputs to accept a 3-bit number. The number of outputs for ROM depends on the square of maximum input binary number.

Let x, y, z are the inputs and D_0, D_1, D_2, D_3, D_4, D_5 are the outputs.

x	y	z	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

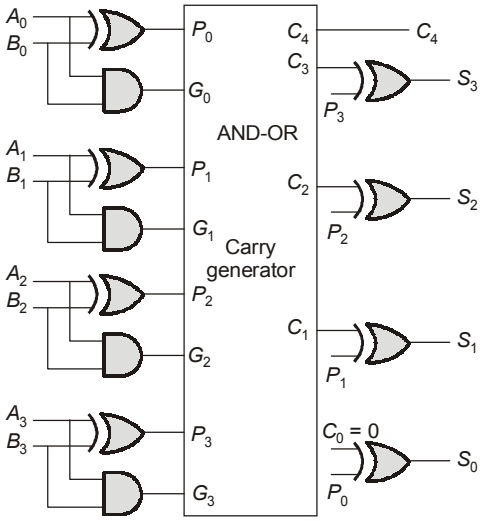
On observing the outputs $D_1 = 0$ and $D_0 = z$, for this ROM we can reduce two outputs to have minimum hardware in its design.

$\therefore$ The size of ROM is $2^3 \times 4 = 8 \times 4$



29. (a)

Consider the 4-bit carry look ahead adder given below,



Carry generator is a two level circuit, i.e., $t_{pd} = 2t_0$

total propagation delay of adder = 20 ns + $2t_0$ ns + 20 ns

= 60 ns

so, 40 ns + $2t_0$ ns = 60 ns

t_0 = 10

30. (a)

$$D_1 = Q_1 Q_0 \odot X$$
$$D_0 = \bar{Q}_1$$
$$Z = Q_0 + X$$

The state table of the given circuit can be developed as follows:

Present State		Input	FF Inputs		Next State		Output
Q_1	Q_0	X	D_1	D_0	Q_1^+	Q_0^+	Z
0	0	0	1	1	1	1	1
0	0	1	0	1	0	1	1
0	1	0	1	1	1	1	1
0	1	1	0	1	0	1	1
1	0	0	1	0	1	0	0
1	0	1	0	0	0	0	1
1	1	0	0	0	0	0	0
1	1	1	1	0	1	0	1

The state diagram given in option (a) satisfies this.

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