S.No. : 02 BS1_CS_A_080719

Digital Logic

CLASS TEST 2019-2020

COMPUTER SCIENCE & IT

Date of Test : 08/07/2019

ANSWER KEY ➤ Digital Logic

1.	(b)	7.	(c)	13.	(a)	19.	(b)	25.	(c)
2.	(d)	8.	(b)	14.	(c)	20.	(c)	26.	(b)
3.	(a)	9.	(b)	15.	(a)	21.	(d)	27.	(b)
4.	(a)	10.	(d)	16.	(d)	22.	(a)	28.	(a)
5.	(c)	11.	(d)	17.	(d)	23.	(a)	29.	(c)
6.	(b)	12.	(c)	18.	(b)	24.	(c)	30.	(b)

DETAILED EXPLANATIONS

1. (b)

Converting into decimal,

$$(2)_3 = 2 \times 3^{\circ} = 2$$
$$(3)_4 = 3 \times 4^{\circ} = 3$$
$$(14)_5 = 1 \times 5^1 + 4 \times 5^{\circ} = 9$$
$$(15)_6 = 1 \times 6^1 + 5 \times 6^{\circ} = 11$$

2. (d)

$$N = 5,$$
$$t_{pd} = 2 \text{ nsec}$$
$$T = 2\,N\,t_{pd}$$
$$\Rightarrow \quad T = 2 \times 5 \times 2 \times 10^{-9}$$
$$= 20 \text{ nsec}$$

3. (a)

$$Y = \bar{S}_0\bar{S}_1 I_0 + S_0\bar{S}_1 I_1 + \bar{S}_0 S_1 I_2 + S_0 S_1 I_3$$
$$= \bar{A}\bar{B}C + \bar{A}B \cdot 1 + A\bar{B} \cdot 0 + AB \cdot \bar{C}$$
$$= \bar{A}\bar{B}C + \bar{A}B \cdot (C + \bar{C}) + AB\bar{C}$$
$$= \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + AB\bar{C}$$
$$\approx 001, 011, 010, 110$$
$$f(A,B,C) = \Sigma m\,(1, 2, 3, 6)$$

4. (a)

$$M = \text{total number of states}$$
$$n = \text{total number of FF's}$$
$$M = 2^n \text{; Binary counter}$$
$$M \le 2^n \text{; Non-Binary counter}$$

5. (c)

Range of signed 1's complement number is $-2^{n-1} + 1$ to $2^{n-1} - 1$.

6. (b)

$$Y_1 = \bar{c}$$
$$F = Y_2 = \bar{d}Y_1 + dc$$
$$= \bar{d}\bar{c} + dc$$
$$= c \odot d$$

7. (c)

Output of the 4 : 1 MUX circuit in Figure **A** is

$$Y = I_0\bar{A}\bar{B} + I_1\bar{A}B + I_2 A\bar{B} + I_3 AB$$

Output of the circuit in Figure **B** is

$$Y = A \oplus B \oplus C = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

On comparison

$$I_0 = C$$
$$I_1 = \bar{C}$$
$$I_2 = \bar{C}$$
$$I_3 = C$$

8. (b)

Simplifying boolean expression:

$$\begin{aligned} F &= C(B + C)(A + B + C) \\ &= (CB + CC)(A + B + C) \\ &= (CB + C)(A + B + C) \\ &= C(1 + B)(A + B + C) \\ &= C(A + B + C) \\ &= AC + BC + C \\ &= C(1 + A + B) \\ &= C \end{aligned}$$

9. (b)

$$Y = I_0 \cdot \bar{S}_1\bar{S}_0 + I_1 \cdot \bar{S}_1 S_0 + I_2 \cdot S_1\bar{S}_0 + I_3 S_1 S_0$$
$$Y = A\bar{B} + (1)B = B + A\bar{B} = A + B$$

10. (d)

11. (d)

Counter output =

	S_2 / A_3	S_1 / A_2	E / A_1	S_0 / A_0		
1st clock	1	1	1	1	– 15	I_7
2nd	1	1	1	0	– 14	I_6
3rd	1	1	0	1	– 13	0
4th	1	1	0	0	– 12	0
5th	1	0	1	1	– 11	I_5
6th	1	0	1	0	– 10	I_4

For 1st and 2nd clock pulses, enable is 1

	S_2	S_1	S_0		
1st clock pulse –	1	1	1	→	1_7
2nd clock pulse –	1	1	0	→	1_6

For 3rd and 4th clock pulse, enable is 0,

So, Y is 0

12. (c)

The characteristics tabel with J, K, Q_n, Q_{n+1} and the excitation table for S and R is shown below –

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

The K-map for S and R is shown as –

For S,

$$S(J, K, Q_n) = \Sigma m(4, 6) + d(1, 5) = J\bar{Q}_n$$

J \ KQ_n	00	01	11	10
0		×		
1	1	×		1

$$S = J\bar{Q}_n$$

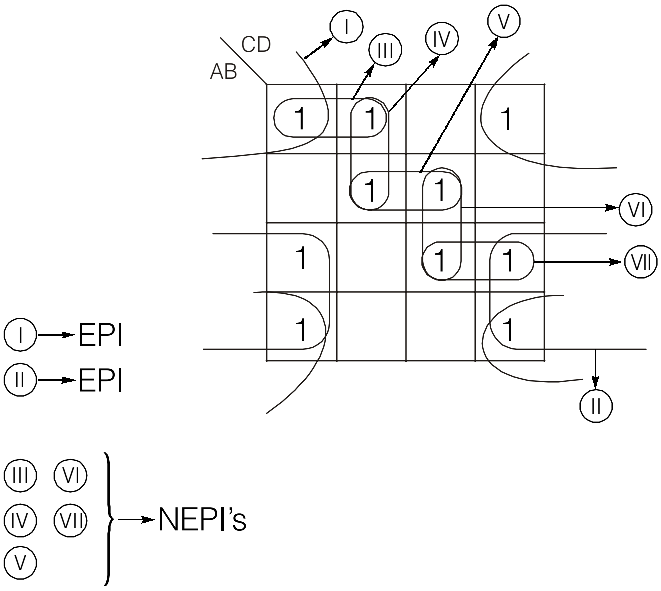
For R,

$$R(J, K, Q_n) = \Sigma m(3, 7) + d(0, 2) = KQ_n$$

J \ KQ_n	00	01	11	10
0	×		1	×
1			1	

$$R = KQ_n$$

13. (a)



EPI = Essential Prime Implicant [which cover a minterm not covered by any other prime implicants]
NEPI = Non Essential Prime Implicant. Number of EPI's = 2, number of NEPI's = 5.

14. (c)

Plotting the K-map for $Y = A\bar{B} + B\bar{C}$

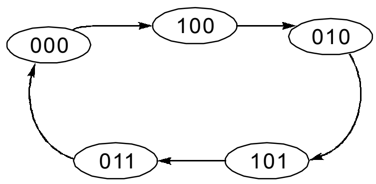
	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	3	1 (2)
A	1 (4)	1 (5)	7	1 (6)

So,

$$\Sigma m(2, 4, 5, 6) = \text{SOP}$$
$$\Sigma \pi(0, 1, 3, 7) = \text{POS}$$

15. (a)

Clock	Present state			FF2		FF1	FF0
	Q_2	Q_1	Q_0	$J_2 = \overline{Q}_0$,	$K_2 = 1$	$D_1 = Q_2$	$T_0 = Q_1$
	0	0	0	1	1	0	0
1	1	0	0	1	1	1	0
2	0	1	0	1	1	0	1
3	1	0	1	0	1	1	0
4	0	1	1	0	1	0	1
5	0	0	0				



The number of used states = 5
∴ modulus value = 5

16. (d)

$$\overline{Z} = (P + A)(Q + \overline{A})$$
$$\overline{Z} = PQ + AQ + \overline{A}P$$
If $$Z = \overline{A} + B$$
$$\overline{Z} = \overline{\overline{A} + B} = A\overline{B}$$
$$Q = \overline{B}, \quad P = O$$

17. (d)

Q_2	Q_1	Q_0	Cr
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1

So the output Q_2 can be directly connected to clear.
∴ Best architecture is a wire connection.

18. (b)

S_1 S_0 ← MUX inputs

Clock	$S.I = Y$	Q_3	Q_2	Q_1	Q_0
		0	0	1	1 ← Initial state
1	0	0	0	0	1
2	0	0	0	0	0
3	1	1	0	0	0
4	1	1	1	0	0
5	1	1	1	1	0
6	1	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1

After 8 clock pulse.

19. (b)

Let the base be x, then

$$\begin{aligned} 292_{10} &= 1204\,x \\ &= 1 \times x^3 + 2 \times x^2 + 0 \times x^1 + 4 \times x^0 \\ &= 292_{10} \\ &= x^3 + 2x^2 + 4 \\ &= 6 \text{ (By substitution)} \end{aligned}$$

20. (c)

A	B	J	K	Q_{n+1}
0	0	1	0	1
0	1	1	1	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0

$$Q_{n+1} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B\bar{Q}_n$$

$$Q_{n+1} = \bar{B} + \bar{A}B\bar{Q}_n$$

$$= \bar{B} + \bar{A}\bar{Q}_n$$

21. (d)

	Q_D	Q_T	FFD $D = \bar{Q}_T$	FFT $T = \bar{Q}_T \oplus Q_D$
Clock pulse	0	0	1	1
1	1	1	0	1
2	0	0	1	1
3	1	1	0	1
4	0	0		

So, output will either be 00 or 11 and never 10.

22. (a)

State table can be drawn from state diagram

Present state	Input	Next state
Q_n	X	Q_{n+1}
0	1	0
0	0	1
1	1	0
1	0	0

$Q_{n+1} = \overline{Q_n + X}$ (Q_{n+1} represent output of NOR gate)

23. (a)

In the circuit, we have

$$D_0 = \overline{Q_1 Q_2} = \bar{Q}_1 + \bar{Q}_2$$
$$D_1 = Q_0$$
$$D_2 = Q_1$$

The truth table for the circuit is obtained below:

	Present State			Inputs			Next State		
CLK number	Q_2	Q_1	Q_0	D_2	D_1	D_0	Q_2^+	Q_1^+	Q_0^+
initial	0	0	0	-	-	-	-	-	-
1	0	0	0	0	0	1	0	0	1
2	0	0	1	0	1	1	0	1	1
3	0	1	1	1	1	1	1	1	1
4	1	1	1	1	1	0	1	1	0

After 4 clock pulses, output is $Q_2\, Q_1\, Q_0 = 110$

24. (c)

For 1st 4×1 MUX,

$$I_0 = C$$
$$I_1 = \bar{C}$$
$$I_2 = \bar{C}$$
$$I_3 = C$$

So, $$f_1(A, B, C) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \Sigma_m(1, 2, 4, 7)$$

For 2nd 4×1 MUX,

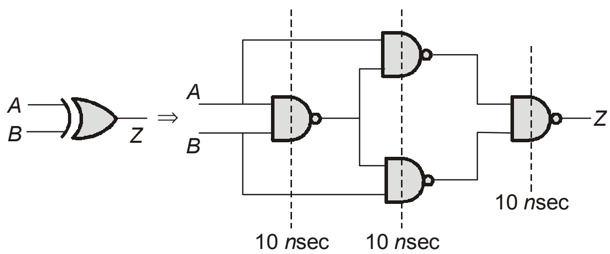
$$I_0 = C$$
$$I_1 = 1$$
$$I_2 = 0$$
$$I_3 = C$$

So, $$f_2(A, B, C) = \bar{A}\bar{B}C + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + AB\cdot C$$
$$= \Sigma_m(1, 2, 3, 7)$$

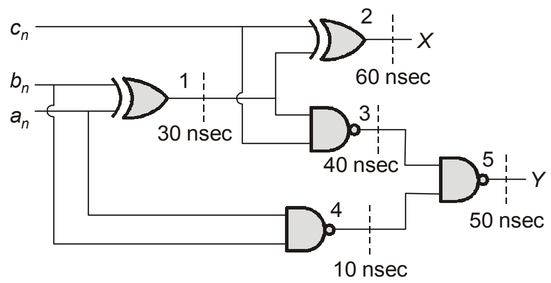
So, f_1 (A, B, C) represents the difference of full substractor while $f_2(A, B, C)$ represents the borrow of full substractor.

25. (c)

An Ex-OR gate can be represented as



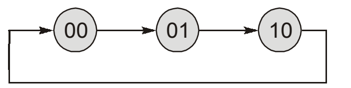
So, for EX-OR gate, it will take 30 nsec to get the output.



So, to get the output Y, it will take 50 nsec.

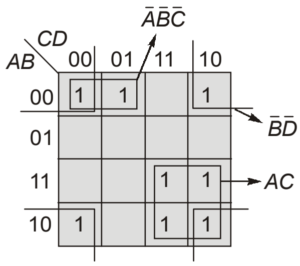
26. (b)

CLK	Q_1	Q_0	FFO $J_0 = \overline{Q}_1$	FFO $K_0 = 1$	FFI $J_1 = Q_0$	FFI $K_1 = \overline{Q}_0$
	0	0	1	1	0	1
1	0	1	1	1	1	0
2	1	0	0	1	0	1
3	0	0				



$N = 3$

27. (b)
The k-map has to rearranged as



$$F = \overline{A}\overline{B}\overline{C} + \overline{B}\overline{D} + AC$$

28. (a)
For the given 4 × 1 MUX, 'A' and 'B' are select lines and 'C' be the input

	I_0	I_1	I_2	I_3
$\overline{C}$	(0)	2	(4)	6
C	(1)	3	(5)	7
	1	0	1	0

So,
$$I_0 = 1 = a$$
$$I_1 = 0 = b$$
$$I_2 = 1 = c$$
$$I_3 = 0 = d$$

So, $a \oplus d = b \oplus c = 1$

So, output of NAND gate is 0 i.e. MUX 'E' connected to '0'.

The MUX is in disable state. MUX is having active high enable, but $E = 0$, so that MUX is in disable state.

Hence MUX output Z is equal to '0'.

29. (c)

Number of flip-flops for mod-16 ripple counter = 4

$$\text{Maximum clock frequency} = \frac{10^9}{4p}\text{Hz} = 5\text{ MHz}$$

$$p = \frac{10^9}{4 \times 5 \times 10^6} = \frac{1000}{20}$$

$$p = 50$$

30. (b)

$$X = (A \oplus B)(B \odot C)C$$

to get $X = 1$,

$$A \oplus B = 1$$

$$B \odot C = 1$$

$$C = 1$$

for $(ABC) = (101) \Rightarrow A \oplus B = 1,\ B \odot C = 0,\ C = 1 \Rightarrow X = 0$

for $(ABC) = (011) \Rightarrow A \oplus B = 1,\ B \odot C = 1,\ C = 1 \Rightarrow X = 1$

for $(ABC) = (111) \Rightarrow A \oplus B = 0,\ B \odot C = 1,\ C = 1 \Rightarrow X = 0$

for $(ABC) = (110) \Rightarrow A \oplus B = 0,\ B \odot C = 0,\ C = 0 \Rightarrow X = 0$

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