RIB RANK IMPROVEMENT BATCH
ELECTRICAL ENGINEERING

RIB-W | T1

Session 2019-20 | S.No. : 220619_LS1

## ANSWER KEY ➤ Digital Electronics

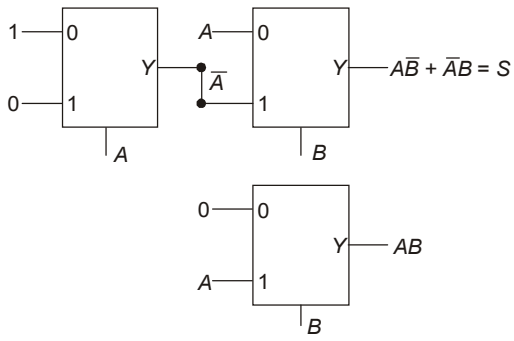
| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1. | (c) | 7. | (a) | 13. | (c) | 19. | (b) | 25. | (a) |
| 2. | (c) | 8. | (d) | 14. | (c) | 20. | (c) | 26. | (b) |
| 3. | (c) | 9. | (c) | 15. | (d) | 21. | (d) | 27. | (d) |
| 4. | (b) | 10. | (c) | 16. | (a) | 22. | (c) | 28. | (c) |
| 5. | (b) | 11. | (c) | 17. | (a) | 23. | (b) | 29. | (a) |
| 6. | (b) | 12. | (b) | 18. | (c) | 24. | (a) | 30. | (d) |

## DETAILED EXPLANATIONS

1. (c)

$$(AB + B\bar{C} + \bar{A}C)(A + C) = AB + AB\bar{C} + ABC + \bar{A}C$$
$$= AB + \bar{A}C$$

2. (c)



**3. (c)**

number of flip-flops required = 4

maximum delay = 4 × 10 nsec = 40 nsec

**4. (b)**

Total number of states possible with 11 flip-flops = $2^{11} = 2048$

Required states = 2014

Number of states to be eliminated

= 2048 – 2014 = 34

**5. (b)**

When MOD 5 and MOD 4 counters are cascaded, the combination becomes MOD 20 counter.

So, output frequency, $f_0 = \frac{f_i}{20} = \frac{20}{20} = 1$ MHz

**6. (b)**

In 2's complement data representation, range with n-bit is: $-(2^{n-1})$ to $+(2^{n-1} - 1)$.

So, 8-bit 2's complement can represent numbers between –128 to +127.

**7. (a)**

In the given digital circuit each multiplexer is working as a NOT gate thus it is a ring oscillator with five NOT gates. The frequency of oscillation will be $f = \frac{1}{2Nt_{pd}}$.

$N$ = number of NOT gates in cascade

$t_{pd}$ = propagation delay of each NOT gate.

$\therefore \quad f = \frac{1}{2 \times 5 \times 25ns} = 4 \times 10^6$ Hz = 4 MHz.

**8. (d)**

From the figure $J = \bar{Q}, K = 1$.

| Clock | $J$ | $K$ | $Q$ | $Q^+$ |
|---|---|---|---|---|
| – | 1 | 1 | 0 | – |
| 1 | 1 | 1 | 0 | 1 |
| 2 | 0 | 1 | 1 | 0 |
| 3 | 1 | 1 | 0 | 1 |
| 4 | 0 | 1 | 1 | 0 |
| 5 | 1 | 1 | 0 | 1 |

Hence, sequence of $Q$ is 010101.

**9. (c)**

Divide by 78 counter can be realized by using cascade of MOD-13 and MOD-6 counter.

**10. (c)**

$$Q^+ = \bar{X}\bar{Y} + X\bar{Y}Q + \bar{X}Y\bar{Q} = \bar{Y}\left[\bar{X} + XQ\right] + \bar{X}Y\bar{Q}$$

$$= \bar{Y}\bar{X} + \bar{Y}Q + \bar{X}Y\bar{Q} = \bar{Y}Q + \bar{X}\left[\bar{Y} + Y\bar{Q}\right] = \bar{Y}Q + \bar{X}\bar{Y} + \bar{X}\bar{Q}$$

$Q^+ = \bar{Y}Q + \bar{X}\bar{Q}$ [using Consensus Law]

**11. (c)**

$$\begin{array}{cccc} \textcircled{1} & \textcircled{1} & \textcircled{1} & \\ G & A & T & E \\ + & E & E & E \\ \hline T & 7 & E & A \end{array}$$

**13. (c)**

$$S_1 = A \oplus B$$
$$C_1 = AB$$
$$S = (A \oplus B) \oplus AB = (A \oplus B) \cdot \overline{AB} + (\overline{A \oplus B}) \cdot AB$$
$$= (A\bar{B} + \bar{A}B)(\bar{A} + \bar{B}) + (AB + \bar{A}\bar{B})(A,B) = A\bar{B} + \bar{A}B) + AB = A + B$$
$$C = (A \oplus B) \cdot AB = (A\bar{B} + \bar{A}B) \cdot AB = 0$$

**14. (c)**

| $Q_3$ | $Q_2$ | $Q_1$ | | |
|---|---|---|---|---|
| 0 | 0 | 0 | ← | Initial state |
| 0 | 0 | 1 | | 1st clock pulse |
| 0 | 1 | 1 | | 2nd clock pulse |
| 1 | 0 | 1 | | 3rd clock pulse |
| 0 | 0 | 0 | | 4th clock pulse |

⇒ Modulus of the counter is 4, After 8 clock pulses $Q_3\ Q_2\ Q_1$ will be 101

**15. (d)**

From the figure we can see that

- 1st change at 1 ns is accepted, so 6th bit i.e. *MSB* is 1
- 2nd change at $t = 2$ ns is not accepted, so 5th bit is 0.
- 3rd change at $t = 3$ ns is not accepted, so 4th bit is 0.
- 4th change at $t = 4$ ns is accepted, so 3rd bit is 1.
- 5th change at $t = 5$ ns is not accepted, so 2nd bit is 0.
- 6th change at $t = 6$ ns is accepted, so 1st bit is 1.

So, digital output is $(100101)_2$.

**16. (a)**

The following table represent the output of the multiplexer.

| Clock | Counter Output | | | MUX Input | | | Output |
|---|---|---|---|---|---|---|---|
| | $A_2$ | $A_1$ | $A_0$ | $S_1$ | $S_0$ | Enable | |
| – | 1 | 0 | 1 | 0 | 1 | 1 | $I_1$ |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2 | 0 | 1 | 1 | 1 | 0 | 1 | $I_2$ |
| 3 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

**17. (a)**

Since, % accuracy is 0.02 thus the maximum error will be

$$= \text{maximum output} \times \frac{(0.02)}{100} = 5 \times \frac{(0.02)}{100} = 1 \text{ mV}$$

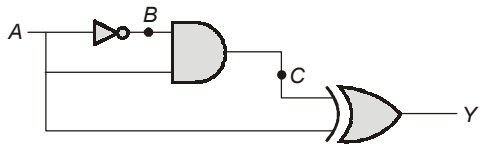
**18. (c)**

The input $D$ is $Q_0 \oplus Q_2 \oplus Q_3$.

| Clock | $D$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|---|
| – | – | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |
| 2 | 0 | 0 | 1 | 1 | 0 |
| 3 | 1 | 1 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 1 |
| 5 | 0 | 0 | 0 | 1 | 0 |
| 6 | 0 | 0 | 0 | 0 | 1 |

Hence, the pattern 0001 appears at 6$^{th}$ pulse.

**19. (b)**




| | $A$ | $B$ | $C$ | $Y$ |
|---|---|---|---|---|
| $t < 10$ ns | 1 | 1 | 0 | 0 |
| 10 ns $< t <$ 20 ns | 1 | 0 | 0 | 1 |
| 20 ns $< t <$ 30 ns | 1 | 0 | 1 | 1 |
| 30 ns $< t <$ 40 ns | 1 | 0 | 0 | 0 |
| 40 ns $< t$ | 1 | 0 | 0 | 1 |

$\Rightarrow$ option (b) is correct.

**20. (c)**

$$Y = \overline{ABC + \bar{A}\bar{B} + BC}$$

Dual of $Y$

$$Y_d = \overline{(A+B+C)\cdot(\bar{A}+\bar{B})\cdot(B+C)}$$

$$= \left[\overline{(A+B+C)} + \overline{(\bar{A}+\bar{B})}\right]\cdot(B+C)$$

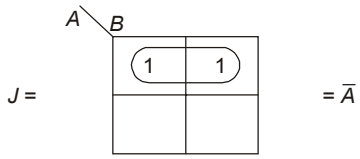
Compliment of $Y$

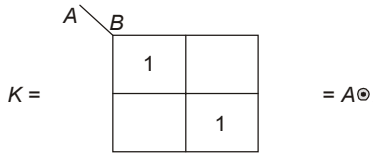
$$Y_c = \overline{\overline{(ABC + \bar{A}\bar{B})} + BC} = \overline{\overline{ABC + \bar{A}\bar{B}}}\cdot\overline{BC} = (ABC + \bar{A}\bar{B})\cdot\overline{BC}$$

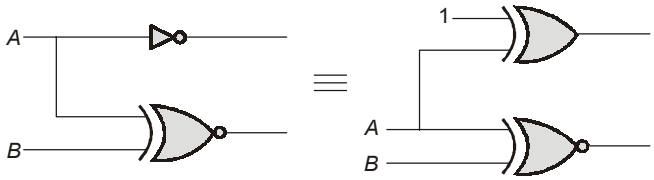
**21. (d)**

State Table

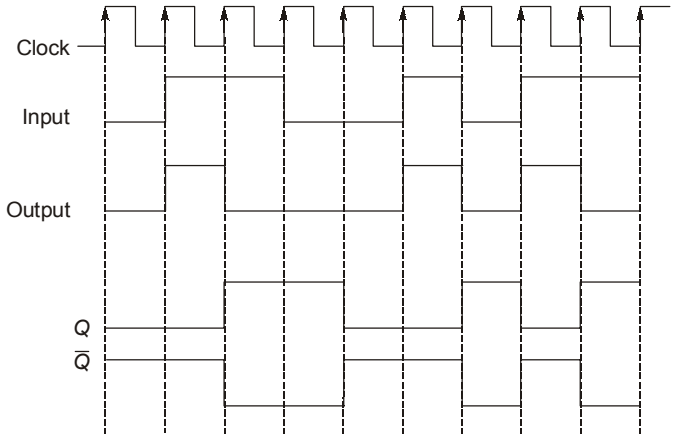
| $A$ | $B$ | $Q_{n+1}$ | $J$ | $K$ |
|---|---|---|---|---|
| 0 | 0 | $\bar{Q}_n$ | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | $Q_n$ | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 |




**22. (c)**




By checking all the options
option (c) correctly matches.

**23. (b)**

Initially $Q_0 = Q_1 = 0$

$\Rightarrow$ $Y_0 = 0$

$\Rightarrow$ $J$ - $K$ flip-flop is cleared

$Q_A = 0$ $\bar{Q}_A = 1$

As clock pulse is applied counter starts up counting

As counter reaches $Q_1 = 1$, $Q_0 = 1$ after 3 clock pulses $J$ - $K$ flip flop is preset.

$\Rightarrow$ $Q_A = 1$ $\bar{Q}_A = 0$

$\Rightarrow$ Counter starts down counting until $Y_0$ is low and this repeats.

So, Output $Q_1$ $Q_0$ in decimal form is

0, 1, 2, 3, 2, 1, 0, 1....

**24. (a)**

$$\overline{\text{Chip select}} = \overline{(A_2 \odot A_3).\overline{[(A_4 \odot A_5)+(A_6 \odot A_7)]}}$$

$$\text{Chip select} = (A_2 \odot A_3).\overline{[(A_4 \odot A_5)+(A_6 \odot A_7)]}$$

Chip select will be '1' when

$[(A_2 = A_3)$ and $(A_4 \neq A_5)$ and $(A_6 \neq A_7)]$

Since $A_1$, $A_0$ are not present in expression of chip select they can have any value.

So the address combination for chip select = 1 are

| | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | × | × |
| 2 | 1 | 0 | 1 | 0 | 0 | 0 | × | × |
| 3 | 1 | 0 | 0 | 1 | 0 | 0 | × | × |
| 4 | 0 | 1 | 0 | 1 | 0 | 0 | × | × |
| 5 | 0 | 1 | 1 | 0 | 1 | 1 | × | × |
| 6 | 1 | 0 | 1 | 0 | 1 | 1 | × | × |
| 7 | 1 | 0 | 0 | 1 | 1 | 1 | × | × |
| 8 | 0 | 1 | 0 | 0 | 1 | 1 | × | × |

We get 8 combinations only 1st combination match with option a

**25. (a)**

In the circuit, we have

$$D_0 = \overline{Q_1.Q_2} = \overline{Q}_1 + \overline{Q}_2$$

$$D_1 = Q_0$$

$$D_2 = Q_1$$

The truth table for the circuit is obtained below.

| CLK | Input | | | Output | | |
|---|---|---|---|---|---|---|
| | $D_2$ | $D_1$ | $D_0$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 2 | 1 | 1 | 1 | 0 | 1 | 1 |
| 3 | 1 | 1 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 1 | 1 | 0 |
| 5 | 0 | 0 | 0 | 1 | 0 | 0 |

The D-flip flop transfer the data from input to output, if CLK pulse is given. After 4 clock pulses, output is

$$Q_2\, Q_1\, Q_0 = 110$$

**26. (b)**

Since clock is applied to ÷ 12 counter. The AND gates have open collector output so RST will be '1' if both the AND gates produce '1'. Thus RST will be 1 when output of top counter is '0110' and output of bottom counter is '1001'. From the circuit we can determine that after every twelve pulses of clock, one pulse of CLK reach to the top counter. So,

| Clock | Output of bottom counter | Output of top counter | Z |
|---|---|---|---|
| 0 | 0000 | 0000 | 0 |
| . | . | . | . |
| . | . | . | . |
| 11 | 1011 | 0000 | 0 |
| 12 | 0000 | 0001 | 0 |
| . | . | . | . |
| . | . | . | . |
| 23 | 1011 | 0001 | 0 |
| 24 | 0000 | 0010 | 0 |
| . | . | . | . |
| . | . | . | . |
| 35 | 1011 | 0010 | 0 |
| 36 | 0000 | 0011 | 0 |
| . | . | . | . |
| . | . | . | . |
| 47 | 1011 | 1011 | 0 |
| 48 | 0000 | 0100 | 1 |
| . | . | . | . |
| . | . | . | . |
| 59 | 1011 | 0100 | 1 |
| 60 | 0000 | 0101 | 1 |
| . | . | . | . |
| . | . | . | . |
| 71 | 1011 | 0101 | 1 |
| 72 | 0000 | 0110 | 1 |
| . | . | . | . |
| . | . | . | . |
| 81 | 1001 | 0110 | 0 |
| 82 | 0000 | 0000 | 0 |

So $Z$ remain 1 for (12 + 12 + 9) clock cycles

So duty cycle $= \dfrac{12+12+8}{12+12+12+12+12+12+8} \times 100 = 39.5\%$

**27. (d)**

$$S_1 = \text{SUM} = A \oplus B \text{ and } S_0 = \text{CARRY} = A.B$$

$$Y = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$$

$$= (A \oplus B)'(AB)' C + (A \oplus B)'(AB) C + (A \oplus B)(AB)' C' + (A \oplus B)(AB) C'$$

$$Y = A \oplus B \oplus C$$

**28. (c)**

Given circuit is of 8 to 1 multiplexer. Multiplexer is used to select any one input out of all inputs at a time. Hence, output will be equal to $I_5$ for a particular combination of selection lines.

For $D = 1$;
$C = 0$;
$A = 1$

combination selects the $I_5$. Also, we have the given logic function as

$$F = AC + ABD + ACD + BCD$$

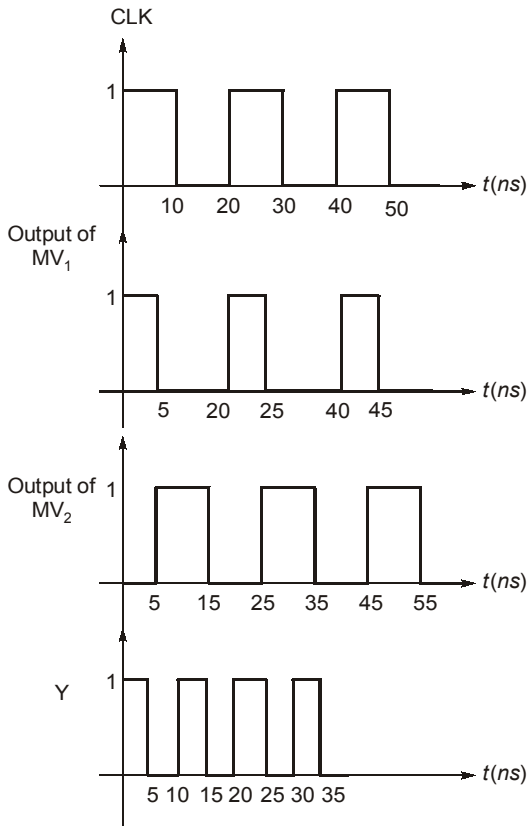
So, by substituting $D = 1$, $C = 0$, and $A = 1$,

We get

$$F = 0 + B + 0 + 0$$
$$F = B$$

Thus, input to $I_5$ must be equal to $B$.

29. (a)




Since $Y$ = (output of $MV_2$) $\oplus$ CLK

So the time period of $Y$ is 100 MHz

30. (d)

$A$ = 10 10 10 10
$B$ = 11 11 11 11
Ex-NOR : 10 10 10 10

Gray code of 10 10 10 10 is 11 11 11 11

Decimal equivalent of (11111111) = 255

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