CLASS TEST

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Digital Electronics

Duration : 1:00 hr. **Maximum Marks : 50**

Read the following instructions carefully

1. This question paper contains **30** objective questions. **Q.1-10** carry one mark each and **Q.11-30** carry two marks each.
2. Answer all the questions.
3. Questions must be answered on Objective Response Sheet (**ORS**) by darkening the appropriate bubble (marked **A**, **B**, **C**, **D**) using HB pencil against the question number. Each question has only one correct answer. In case you wish to change an answer, erase the old answer completely using a good soft eraser.
4. There will be **NEGATIVE** marking. For each wrong answer **1/3rd** of the full marks of the question will be deducted. More than one answer marked against a question will be deemed as an incorrect response and will be negatively marked.
5. Write your name & Roll No. at the specified locations on the right half of the **ORS**.
6. No charts or tables will be provided in the examination hall.
7. Choose the **Closest** numerical answer among the choices given.
8. If a candidate gives more than one answer, it will be treated as a **wrong answer** even if one of the given answers happens to be correct and there will be same penalty as above to that questions.
9. If a question is left blank, i.e., no answer is given by the candidate, there will be **no penalty** for that question.

DO NOT OPEN THIS TEST BOOKLET UNTIL YOU ARE ASKED TO DO SO

Q.No. 1 to Q.No. 10 carry 1 mark each

Q.1 If the value of $X + Y = 1$, then the value of $X \oplus Y$ is equal to

(a) X (b) $\bar{X} + \bar{Y}$
(c) 1 (d) 0

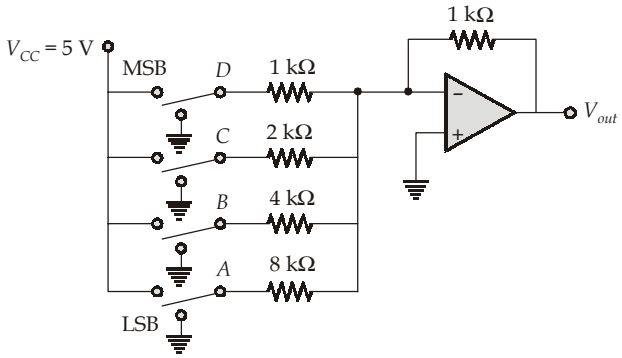
Q.2 The minimum number of 2 × 1 MUX required to implement a half-subtracter circuit when only basic inputs 0, 1, A and B are available is

(a) 2 (b) 4
(c) 5 (d) 6

Q.3 The total number of NAND gates required to implement a 4 × 1 multiplexer is (assuming a NAND gates of any number of inputs are available) _____.

(a) 2 (b) 4
(c) 7 (d) 9

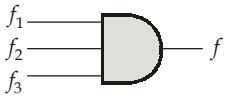
Q.4 Consider the figure shown below:



The weight of input (B) is

(a) – 2.5 V (b) – 1.25 V
(c) – 2 V (d) – 3 V

Q.5 Consider the logical function given below.
$f_1(A,B,C) = \Sigma m(2, 3, 4)$



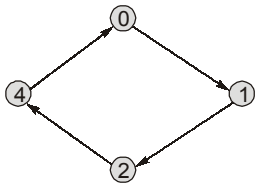
$f_2(A,B,C) = \Pi M(0, 1, 5, 6, 7)$
If 'f_{out}' is logic zero, then maximum number of possible minterm of function $f_3(A,B,C)$ is equal to

(a) 6 (b) 7
(c) 5 (d) 8

Q.6 A ripple counter is made with three positive edge triggered flip-flops. If the output of previous lower significant bit flip-flop is used as a triggering clock pulse of the next higher significant bit flip-flop, then the resultant counter is a

(a) MOD 3 up counter
(b) MOD 3 down counter
(c) MOD 8 bit up counter
(d) MOD 8 down counter

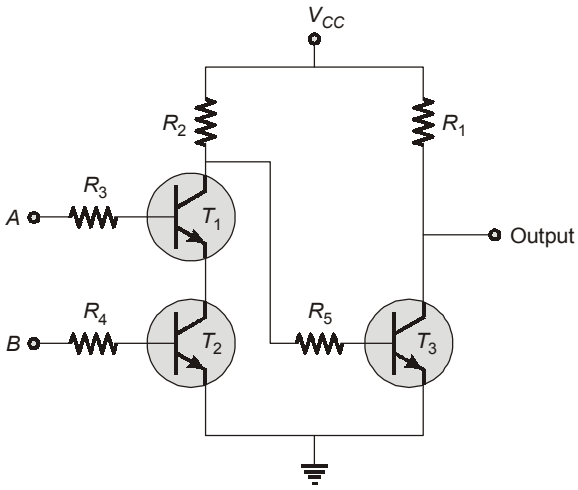
Q.7 The sequence diagram of a counter is shown in the figure below.



If the state values shown in the sequence diagram are the decimal equivalents of the corresponding states of the counter, then the minimum number of flip-flops required to design this counter is

(a) 3 (b) 4
(c) 2 (d) 5

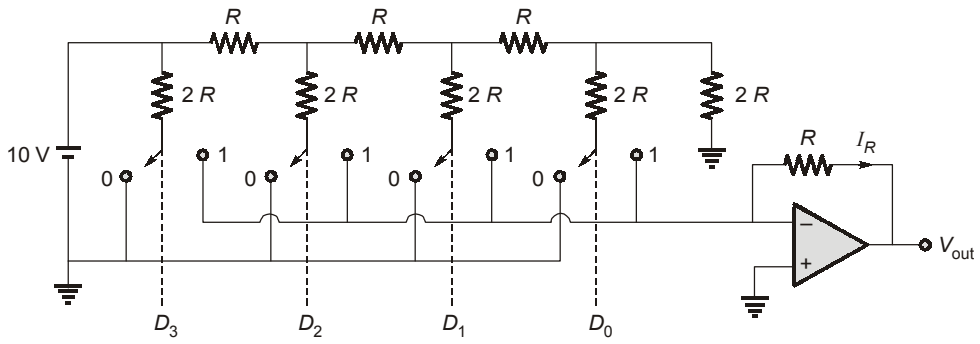
Q.8 Consider the circuit given in the figure below:



Assume that the voltage levels applied to the circuit are such that they ensure that the transistors will be either in saturation region or in cut-off region. Then the negative logic constructed by this circuit is

(a) AND (b) NAND
(c) OR (d) NOR

Q.9 Consider the circuit shown in the figure below:



If the value of R = 5 kΩ and the digital input signal $(D_3D_2D_1D_0)$ is $(1101)_2$, then the value of current I_R is

(a) 1.25 mA (b) 1.625 A
(c) 1.25 A (d) 1.625 mA

Q.10 Consider the following arithmetic operation

$$(24)_x + (17)_x = (40)_x$$

The least possible value of 'x' for which the above operation is valid is

(a) 5 (b) 9
(c) 11 (d) 16

Q.11 Let $X = X_2X_1X_0$ and $Y = Y_1Y_0$ be unsigned positive 3-digit and 2-digit numbers respectively. The output function 'f' = 1 only when $X > Y$ otherwise '0'. Then the value of output f is equal to

(a) $(X_2 + Y_1 + Y_0)(X_2 + \bar{X}_1 + \bar{Y}_0)(X_2 + X_1 + \bar{Y}_1)(X_2 + X_1 + X_0)(X_2 + X_0 + \bar{Y}_1)$

(b) $(X_2 + \bar{Y}_1 + \bar{Y}_0)(X_2 + X_1 + \bar{Y}_0)(X_2 + \bar{X}_1 + Y_1)(X_2 + X_1 + X_0)(X_2 + X_0 + \bar{Y}_1)$

(c) $(X_2 + \bar{Y}_1 + \bar{Y}_0)(X_2 + X_1 + \bar{Y}_0)(X_2 + X_1 + \bar{Y}_1)(X_2 + X_1 + X_0)(X_2 + X_0 + \bar{Y}_1)$

(d) $(X_2 + \bar{Y}_1 + \bar{Y}_0)(X_2 + \bar{X}_1 + \bar{Y}_0)(X_2 + X_1 + \bar{Y}_1)(X_2 + \bar{X}_1 + \bar{X}_0)(X_2 + X_0 + \bar{Y}_1)$

Q.12 The minimized expression for Boolean expression

$$f(A, B, C, D) = \Sigma m(0, 2, 4, 9, 11) + d(1, 5, 13)$$

can be expressed as

(a) $(A + \bar{C} + \bar{D})(\bar{B} + \bar{C})(A + \bar{D})$

(b) $(\bar{A} + \bar{D})(\bar{B} + \bar{C})(A + \bar{D})$

(c) $(A + \bar{D})(\bar{B} + \bar{C})(\bar{A} + D)$

(d) $(\bar{A} + \bar{C} + \bar{D})(\bar{B} + \bar{C})(\bar{A} + D)$

Q.13 The number of minterms after minimizing the following Boolean expression is _____.

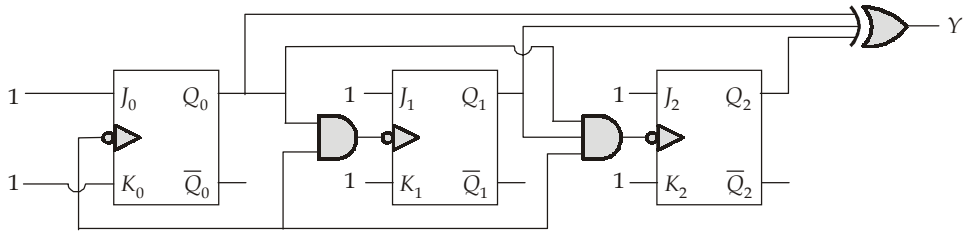
[D' + AB' + A'C + AC'D + A'C'D]'

(a) 1 (b) 2
(c) 3 (d) 4

Q.14 Consider a 3-bit number A and 2 bit number B are given to a multiplier. The output of multiplier is realized using AND gate and one bit full adders. If minimum number of AND gates required are X and one bit full adders required are Y, then $X + Y =$ _____.

(a) 9 (b) 7
(c) 8 (d) 6

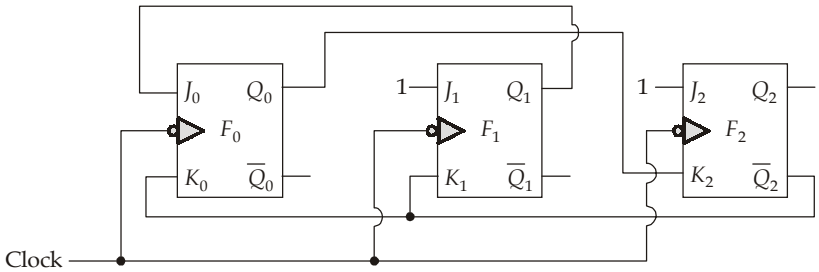
Q.15 Consider the circuit shown in the figure below:

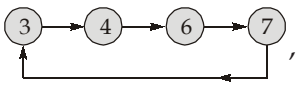


The value of output $Q_0Q_1Q_2$ and the value of output Y after the 5th clock pulse is (Assume the initially all the flip-flop are reseted.)

(a) Output = 001 and $Y = 1$
(b) Output = 101 and $Y = 0$
(c) Output = 100 and $Y = 1$
(d) Output = 010 and $Y = 1$

Q.16 Consider the counter circuit shown in the figure below:

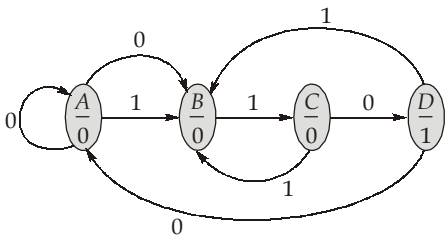


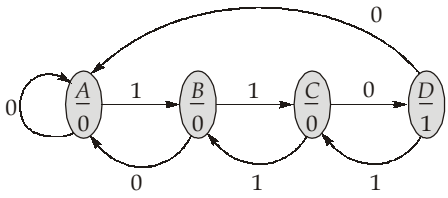
The counter is designed such that it counts the states 

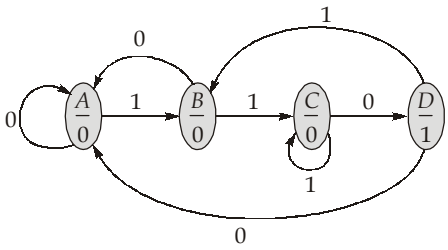
, then which of the following statements about this counter is true?

(a) The counter enters into a lockout state if the counter starts from $(5)_{10}$
(b) The counter enters into a lockout state if the counter starts from $(2)_{10}$
(c) The counter enters into a lockout state if the counter starts from $(3)_{10}$
(d) The counter do not enters into a lockout state.

Q.17 Out of the given state diagram of a Moore type sequence detector, which of the option represents a "110" sequence detector?

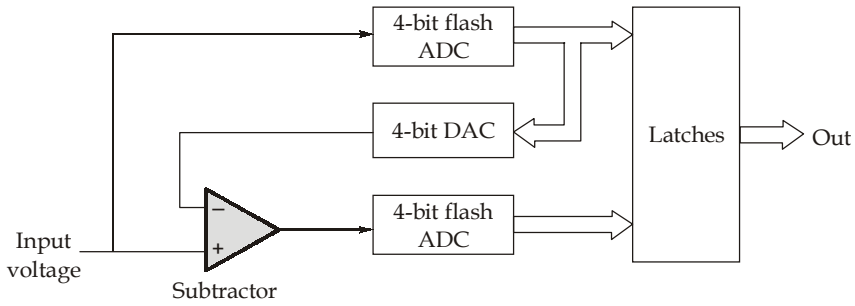
(a)


(b)


(c)


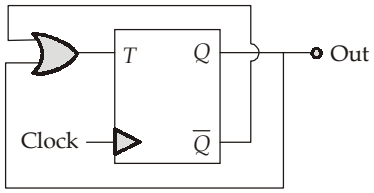
(d) none of the above

Q.18 Consider the circuit shown in the figure below:



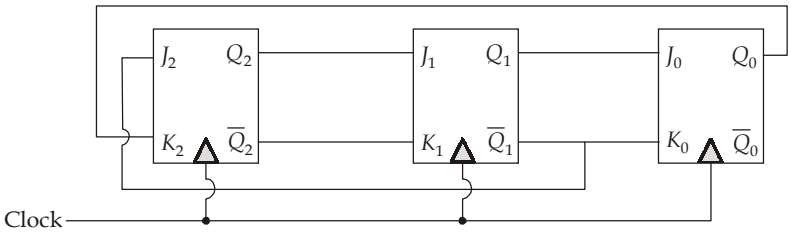
The circuit represents
(a) 4-bit subtracter circuit
(b) A 4-bit A to D convertor
(c) A 8-bit adder circuit
(d) A 8-bit A to D convertor

Q.19 Consider the circuit shown in the figure below:



If the input clock frequency is 10 kHz, then the output frequency is equal to
(a) 2.5 kHz (b) 3 kHz
(c) 10 kHz (d) 5 kHz

Q.20 Consider the circuit shown in the figure below.



Then the value of $(Q_2 Q_1 Q_0)$ after the first clock pulse is equal to _____.
(Assume all the outputs to be '0' initially)

(a) 010 (b) 110
(c) 111 (d) 100

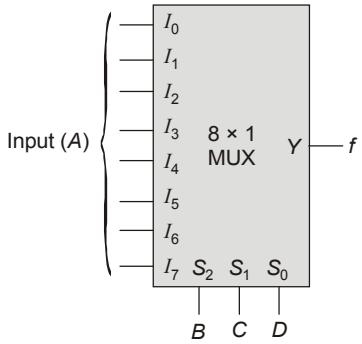
Q.21 A Mealy system produces an output 1 if the input has been '0' for atleast two consecutive clocks followed immediately by 1 for two or more consecutive clock. The minimum number of states required to design this system is

(a) 3
(b) 4
(c) 5
(d) 6

Q.22 Consider an n-variable boolean function $f(A, B, C, ...)$. If the boolean function is represented as $f(A, B, C, ...) = A + \overline{A}B + \overline{A}\overline{B}C + ...$, then the alternative representation of the above function can be given as

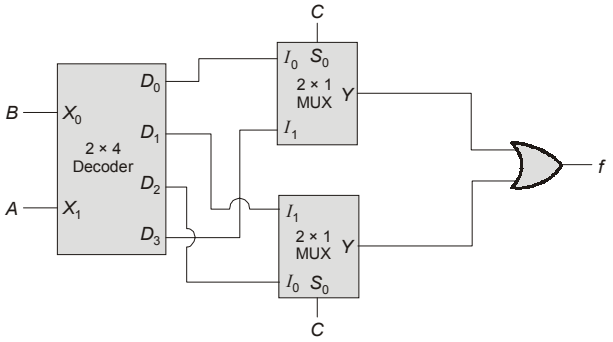
(a) $A + B + C + D.....$
(b) $\overline{A} + \overline{B} + \overline{C} + \overline{D} + ...$
(c) 1
(d) 0

Q.23 A 8 × 1 multiplexer is used to realize a four variable function, $f(A, B, C, D) = \Sigma m(0, 2, 4, 6, 7, 9, 14, 15)$. A is taken as MSB and it is used as the input to the multiplexer. The select line inputs are given supply from the variables B, C, D, where B is at the MSB and D is at the LSB of the select line, then the input to the MUX from I_0 to I_7 respectively are



(a) $\overline{A}, A, \overline{A}, 0, A, 0, 1, 1$
(b) $A, A, \overline{A}, 0, A, 0, 1, 1$
(c) $\overline{A}, \overline{A}, A, 0, A, 0, 1, 1$
(d) $\overline{A}, A, \overline{A}, 0, \overline{A}, 0, 1, 1$

Q.24 A logic function 'f' is implemented by the circuit shown in the figure below. The circuit consists of one 2 × 4 decoder, two 2 × 1 multiplexers and a two input OR gate connected in cascade. Then the function 'f' is equal to

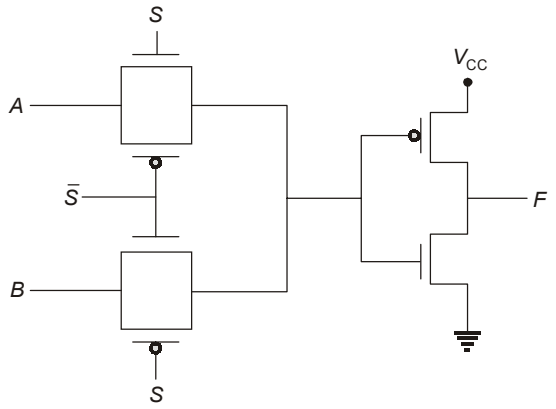


(a) $A \oplus B$ (b) $B \odot C$
(c) $A \oplus B \oplus C$ (d) $A \odot B$

Q.25 A ROM chip has to be created with a capacity of 16K × 8. If the available ROM chip is of the size 2K × 4, then the number of such chips required to construct a 16K × 8 ROM chip is

(a) 16 (b) 8
(c) 32 (d) 64

Q.26 The circuit shown in the figure below is constructed using MOS circuits and PASS transistors. For $S = 1$, the output F is equal to



(a) $\bar{A}B$ (b) $A\bar{B}$
(c) A (d) $\bar{A}$

Q.27 The K-map of a boolean function is shown in the figure below. The number of essential prime implicants of this function is _____.

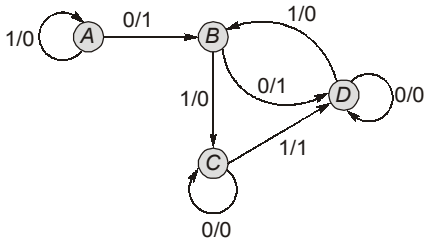
AB \ CD	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	0	1	1	1
10	0	1	0	0

(a) 2 (b) 4
(c) 7 (d) 6

Q.28 A 1-bit full adder takes 10 ns to generate output carry bit and 20 ns to generate the output sum bit. If four such full adders are cascaded to form a 4-bit parallel adder, then the maximum number of 4-bit additions per second that can be performed by the parallel adder is _____ × 10^6.

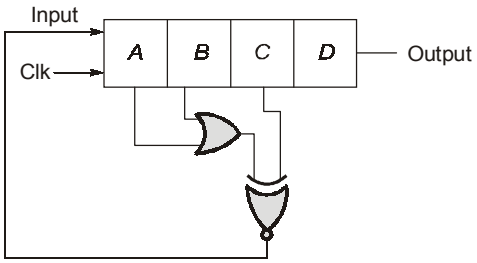
(a) 16 (b) 18
(c) 20 (d) 25

Q.29 The state diagram of a digital synchronous circuit is shown in the figure below. The machine has four states named as A, B, C and D. The input to this system is given by a bit stream of 0's and 1's. If the starting state of the circuit is A, then the number of times the output goes to 1, for an input bit stream of 010011, is



(a) 3 (b) 1
(c) 4 (d) 2

Q.30 A four bit serial in parallel out shift register is constructed as shown in the figure below. The register is a right shift register i.e. $A \rightarrow B$, $B \rightarrow C$, $C \rightarrow D$ and D is connected to the output. If the initial state ($ABCD$) of the shift register is (1000), then the minimum number of clock cycles after which the state ($ABCD$) of the shift register will be again equal to (1000) is _____ .



(a) 4 (b) 5
(c) 6 (d) 7

■■■■

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DIGITAL ELECTRONICS

Date of Test : 25/06/2022

ANSWER KEY ➤

1.	(b)	7.	(a)	13.	(a)	19.	(d)	25.	(a)
2.	(a)	8.	(c)	14.	(a)	20.	(d)	26.	(d)
3.	(c)	9.	(d)	15.	(b)	21.	(b)	27.	(b)
4.	(b)	10.	(c)	16.	(d)	22.	(a)	28.	(c)
5.	(c)	11.	(c)	17.	(c)	23.	(d)	29.	(d)
6.	(d)	12.	(c)	18.	(d)	24.	(b)	30.	(a)

DETAILED EXPLANATIONS

1. (b)

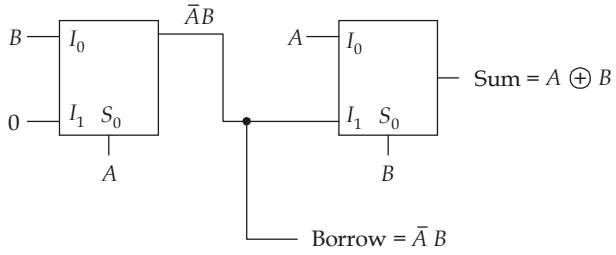
$$X \oplus Y = \overline{X \odot Y} = \overline{\bar{X}\bar{Y} + XY}$$

$$= \overline{(\bar{X}\bar{Y})}\,\overline{(XY)}$$

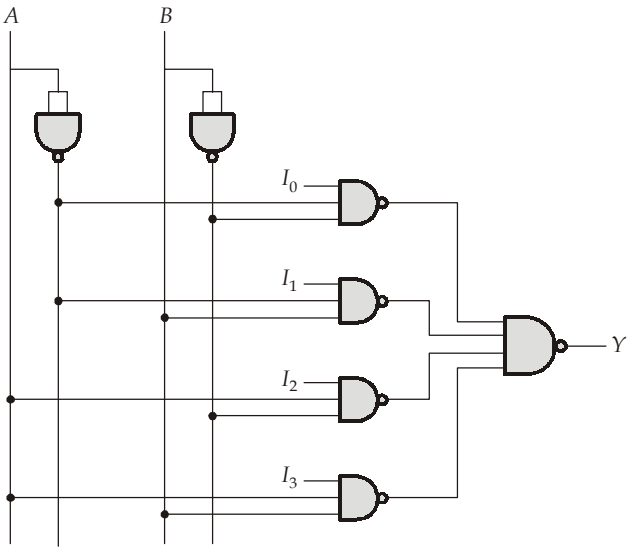
$$= (X + Y)(\bar{X} + \bar{Y})$$

$$= \bar{X} + \bar{Y} \qquad (\because\ X + Y = 1 \text{ which is given})$$

2. (a)



3. (c)



4. (b)

Let $B = 1$ and rest input bit equal to zero. The value of 1 is 5 V

$$\therefore \qquad V_0 = -\frac{5}{4\,\text{k}\Omega} \times 1\,\text{k}\Omega = -1.25\,\text{V}$$

5. (c)

$$f_1(A,B,C) = \Sigma m(2, 3, 4)$$

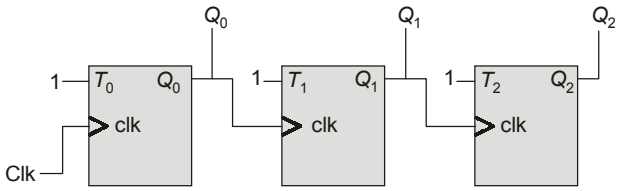
$$f_2(A,B,C) = \Sigma m(2, 3, 4)$$

for output f_{out} to be zero, f_3 should be equal to

$\therefore$ $f_3(A,B,C) = \Sigma m(0, 1, 5, 6, 7)$

Hence, the maximum number of possible minterms = 5.

6. (d)



Thus this will create a MOD 8 or 3 bit down counter.

7. (a)

To represent a state with decimal equivalent of 4, we require minimum "three" flip-flops.

$\because$ $(4)_{10} \rightarrow (100)_2$

8. (c)

$\because$ The logic will perform the function of positive AND gate.

Since,

A (Volt)	B (Volt)	T_1	T_2	T_3	Output
V^-	V^-	OFF	OFF	ON	V_{sat}
V^-	V^+	OFF	ON	ON	V_{sat}
V^+	V^-	ON	OFF	ON	V_{sat}
V^+	V^+	ON	ON	OFF	V_{CC}

The corresponding truth table for negative logic:

A	B	Output
1	1	1
1	0	1
0	1	1
0	0	0

Thus the circuit will behave as negative OR-logic.

9. (d)

$$I_R = I_3 + I_2 + I_0$$
$$= \left(\frac{E_{reff}}{2R} + \frac{E_{reff}}{4R} + \frac{E_{reff}}{16R}\right) = \left(\frac{10}{10} + \frac{10}{20} + \frac{10}{80}\right)$$
$$= \frac{130}{80} = \frac{13}{8} = 1.625 \text{ mA}$$

10. (c)

Writing the equation in expanded decimal form, we get,

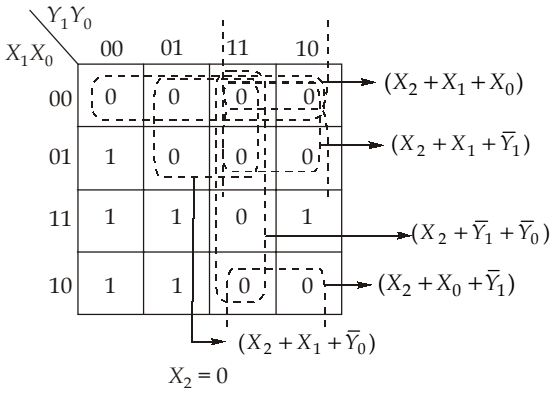
$$(2x + 4) + (x + 7) = 4x$$
$$3x + 11 = 4x$$
$$x = 11$$

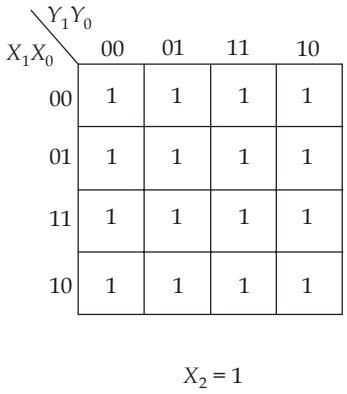
11. (c)

Now, $X > Y$ if

(a) $X_2 = 1$

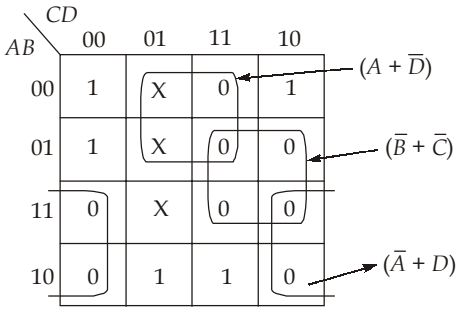
(b) $X_2 = 0$ and $X_1X_0 > Y_1Y_0$





12. (c)

The above expression can be represented in *K*-map as,



13. (a)

$[D' + AB' + A'C + AC'D + A'C'D]'$

$= [D' + AC'D + AB' + A'C + A'C'D]'$

$= [D' + AC' + AB' + A' [C + C'D]]'$

$= [D' + AC' + AB' + A' [C + D]]'$

$= [D' + AC' + AB' + A'C + A'D]'$

$(\because\ D' + A'D = D' + A')$

$= [D' + A' + AC' + AB' + A'C]'$

$(\because A' + A'C = A')$

$(\because A' + AC' + AB' = A'+A(C'+B') = A' + C' + B')$

$= [D' + A' + C' + B']'$

$= ABCD$

Hence, only 1 minterm is required.

14. (a)

Let

$$\begin{array}{lcccc} A = & & a_2 & a_1 & a_0 \\ B = & & & b_1 & b_0 \\ \hline A \times B = & & a_2b_0 & a_1b_0 & a_0b_0 \\ & b_1a_2 & b_1a_1 & b_1a_0 & \downarrow \\ \hline & b_1a_2 & (a_2b_0 + a_1b_1) & (a_1b_0 + b_1a_0) & a_0b_0 \\ & C_3 & C_2 & C_1 & C_0 \end{array}$$

Number of AND gates required $X = 6$

Number of one bit full adders required $Y = 3$

$$X + Y = 6 + 3 = 9$$

15. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

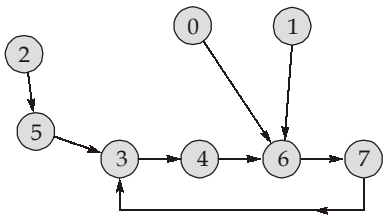
$\therefore$ $Y = Q_2 \oplus Q_1 \oplus Q_0$

$= 1 \oplus 0 \oplus 1 = 0$

16. (d)

Test for Lockout

Present State			Present Input						Next State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1	1	0	1	1	1	0
0	0	1	1	1	1	1	0	1	1	1	0
0	1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	1	1	0	0	0	0	1	1



Hence, the counter does not enter into lockout state.

19. (d)

$\because$ $Q + \bar{Q} = 1$ always, thus the flip-flop will toggle always.

$\therefore$ $f_{out} = \frac{f_{clk}}{2} = \frac{10}{2} \times 10^3 = 5\,\text{kHz}$

20. (d)

At first cycle, the inputs of flip-flop are

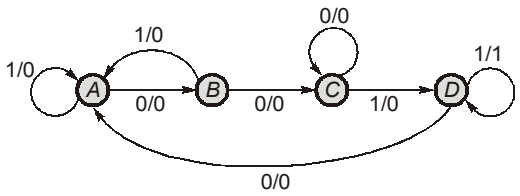
$J_2K_2 = 1\ 0$ (Set)
$J_1K_1 = 0\ 1$ (Reset)
$J_0K_0 = 0\ 1$ (Reset)

$\therefore$ $Q_2 = 1$
$Q_1 = 0$
$Q_0 = 0$

$\therefore$ Output $(Q_2Q_1Q_0) = (100)_2$

21. (b)

The state diagram can be drawn as



Hence, minimum number of states = 4.

22. (a)

$f(A, B, C, ...) = A + \bar{A}B + \bar{A}\bar{B}C + ...$

$= A + \bar{A}(B + \bar{B}C + \bar{B}\bar{C}D + ...)$

$= A + \bar{A}X$ (where $X = B + \bar{B}C + \bar{B}\bar{C}D + ...$)

$= A + X$ ($\because A + \bar{A}X = A + X$)

$= A + B + \bar{B}C + \bar{B}\bar{C}D + ...$

$= A + B + \bar{B}(C + \bar{C}D + ...)$

$= A + B + C + ...$

Hence, option (a) is correct.

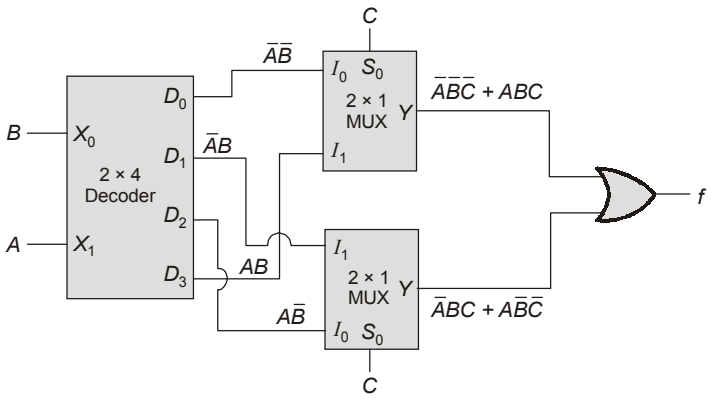
23. (d)

The input can be determined by constructing an input table as follows:

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	⓪	1	②	3	④	5	⑥	⑦
A	8	⑨	10	11	12	13	⑭	⑮
	$\bar{A}$	A	$\bar{A}$	0	$\bar{A}$	0	1	1

24. (b)

The above circuit can be redrawn as



Thus, $f = \underbrace{\bar{A}\bar{B}\bar{C} + ABC} + \underbrace{\bar{A}BC + A\bar{B}\bar{C}}$

$= \bar{B}\bar{C}(A + \bar{A}) + BC(\bar{A} + \bar{A})$

$= \bar{B}\bar{C} + BC$

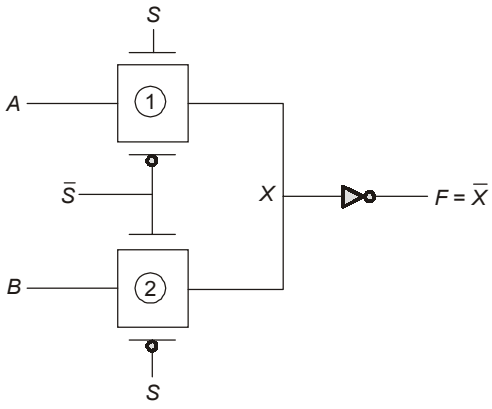
$= B \odot C$

25. (a)

To create a 16K × 8 ROM chip we require eight 2K × 4 chips in series and two such block of 8 chips to be connected in parallel to make the output line of 8 bits.

Hence, a total number of 16 chips are required.

26. (d)



Equivalent Circuit

From the equivalent circuit, it can be concluded that,

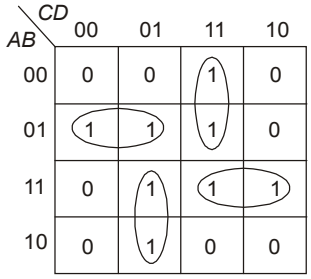
$\bar{F} = X = AS + B\bar{S}$

$\therefore \quad F = \overline{AS + B\bar{S}}$

For $S = 1$, $\quad F = \bar{A}$

27. (b)

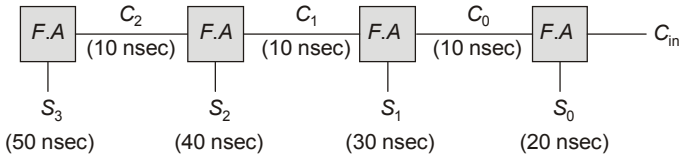
To find the essential prime implicants, we have to select those groups in which there is atleast one min-term which is part of only that group and cannot be grouped by any other way.



So, there are 4 prime implicants in the given *K*-map.

28. (c)

The 4-bit parallel adder can be analyzed as follows:



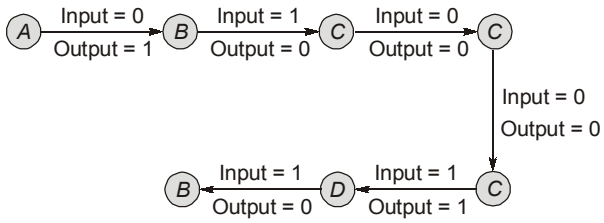
Thus, the last sum bit will be generated in 50 nsec.

Thus, the maximum rate of 4-bit additions possible is,

$$\frac{1}{50\times10^{-9}}/\text{sec} = \frac{10^9}{50}/\text{sec} = 20\times10^6/\text{sec}$$

29. (d)

For the given input, the output can be determined by following the sequence of states as given below.



From the above diagram it is clear that, the output goes to 1 for two times for the given input.

30. (a)

$$\text{Input} = (A+B)\odot C$$

Now,

Clk	Register	Input
Initially	1000	$(1+0)\odot0=0$
1	0100	$(0+1)\odot0=0$
2	0010	$(0+0)\odot1=0$
3	0001	$(0+0)\odot0=1$
4	1000	

■■■■