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Microprocessors

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CLASS TEST 2019-2020

ELECTRONICS ENGINEERING

Date of Test : 09/06/2019

ANSWER KEY ➤ Microprocessors

1.	(c)	7.	(b)	13.	(d)	19.	(d)	25.	(d)
2.	(a)	8.	(d)	14.	(c)	20.	(a)	26.	(c)
3.	(a)	9.	(b)	15.	(c)	21.	(a)	27.	(c)
4.	(c)	10.	(a)	16.	(a)	22.	(c)	28.	(c)
5.	(a)	11.	(c)	17.	(c)	23.	(a)	29.	(d)
6.	(b)	12.	(d)	18.	(c)	24.	(c)	30.	(a)

DETAILED EXPLANATIONS

1. (c)

SIM instruction can not reset TRAP flip-flop of flag register because TRAP is a non-makable interrupt.

2. (a)

The instruction CPI compares the immediate data with the contents of accumulator. Contents of accumulator remains same. All flags are affected but status of comparison can be read by only zero and carry flag.

3. (a)

By analysing the given table $IO/\overline{M}$ is high

$\Rightarrow$ IO operation

$\overline{RD}$ is logic low

$\Rightarrow$ IN operation

In I/O mapped I/O both address lines i.e., lower order and higher order. Contains same address.

$\Rightarrow$ IN 24 H is being executed.

4. (c)

$$\text{Total memory size} = 32\text{ MB}$$
$$= 2^5 \times 2^{20} \times 8 = 2^{28}\text{ bits}$$

Let number of address lines = n = number of data lines

so $2^n \times 2^n = 2^{28}$

$2^{2n} = 2^{28}$

$n = 14$

5. (a)

ANI instruction resets the carry flag. So, the control of program will not go back to LOOP.

6. (b)

Time required for execution = number of T states $\times$ time of 1 T states

$$= 12 \times \frac{1}{5 \times 10^{+6}} = 2.4 \times 10^{-6}$$
$$= 2.4\ \mu\text{sec}$$

7. (b)

TRAP $\equiv$ RST 4.5

Address of RST 4.5 = 4.5 × 8= $(0036)_{10}$

$= (0024)_H$

8. (d)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Starting Address	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	8800 H
⋮																	⋮
Ending Address	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	8FFF H

9. (b)

DMA controller routes the data directly from memory to I/O devices and vice-versa without passing through microprocessor.

10. (a)

INTR is level triggered.

11. (c)

1. MOV A, C
2. STC
3. CMC
4. DCR C

C | 00 | H

1. A | 00 | H
2. CY | 1 |
3. CY | 0 |
4. C | FF | H

	S	Z	X	AC	X	P	X	CY
Flags	1	0	0	0	0	1	0	0

$= 84\,H$

12. (d)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Starting Address	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	8800 H
⋮																	⋮
Ending Address	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	8FFF H

13. (d)

CY

1

A: | *x* | *x* | *x* | *x* | 0 | 0 | 0 | 0 |

After execution of RRC 4 time

A: | 0 | 0 | 0 | 0 | *x* | *x* | *x* | *x* |

Which is equivalent to dividing by $(10000)_2$ or 16.

14. (c)

Number of address lines = $\log_2$ (32 K) = $\log_2(2^5 \times 2^{10})$ = 15
Length of stack pointer = Length of program counter = 15
Since it is an 8 bit microcomputer
So, Numbers of data lines = 8.

15. (c)

IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$		
0	0	0	D_0	
0	0	1	D_1	MEM RD
0	1	0	D_2	MEM WR
0	1	1	D_3	
1	0	0	D_4	
1	0	1	D_5	I/O RD
1	1	0	D_6	I/O WR
1	1	0	D_7	

17. (c)

(1) SP → *4000* H
(2) SP – 2 → *3FFE* H
(3) SP – 2 → *3FFC* H
(4) PC → *3050* H
(5) SP + 2 → *3FFE* H PC → *3009* H
(6) SP → *3FFE* H PC → *300A* H

18. (c)

1	0	0	0	1	1	1	0
SOD	SDE	X	R7.5	MSE	M7.5	M6.5	M5.5

Serial data enable bit is zero.
⇒ Serial data is disabled.
MSE - Mask set enable bit is 1.
⇒ Masking of bit is enabled.
RST 7.5 and RST 6.5 are masked while RST 5.5 is enabled.

20. (a)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	1	0	1	0	0	0	1	50 H
0	1	0	1	0	0	1	1	53 H
0	1	0	1	0	1	0	0	54 H
0	1	0	1	0	1	1	1	57 H

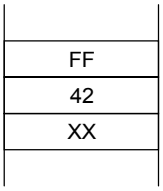
21. (a)

1. SP | 02 | 00 | H

2. BC | 10 | 28 | H

3. HL | 42 | FF | H

4. SP | 01 | FE | H



5. DE | 20 | FE | H

6. HL | 53 | 27 | H

7. HL | 20 | FE | H DE | 53 | 27 | H

8. HL | 74 | 25 | H

Content of HL register pair after execution of program is 7425 H.

22. (c)

1. A | 58 | H

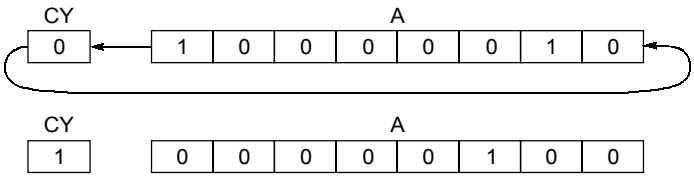
2. D | 82 | H

3. A | 00 | H Flags

S	Z	X	AC	X	P	X	CY
0	1	0	1	0	1	0	0

4. A | 82 | H

5.



23. (a)

Total number of RAM chip required = $\frac{128\,K}{2\,K} = 64$

$\Rightarrow$ 64 chip select signals are need to be generated with 1 : 2 decoder.

Number of decoder chips $= \frac{64}{2} = 32$

$= \frac{32}{2} = 16$

$= \frac{16}{2} = 8$

$= \frac{8}{2} = 4$

$= \frac{4}{2} = 2$

$= \frac{2}{2} = 1$

$= 32 + 16 + 8 + 4 + 2 + 1 = 63$

24. (c)

LXI B	BC	00 | 20 H
LOOP DCX	BC	00 | 1F H
MOV A, B	A	00
ORA C	A	1F

JNZ LOOP

The loop will execute 20 H times or 32 times.

The instruction ORA C is executed 32 times.

26. (c)

EI instruction is used to enable interrupt and used at the starting of main program.

DI instruction is used to disable only maskable interrupt.

SIM provide serial data only when serial data enable (SDE) bit is high.

Status Register contains flags.

27. (c)

Data set-up time is the minimum time for which the data must be valid before the write pulse ends.

29. (d)

Delay = Loop T-states $\times$ count $\times$ clock period

$= 32 \times 9470 \times \frac{1}{3.03 \times 10^6}$

$\approx$ 100 ms

30. (a)

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Maximum memory can be addressed is

$[(1FFF - 1000 + 1) + (2FFF - 2000 + 1) + (4FFF - 4000 + 1) + (8FFF - 8000 + 1)]$ H

$= 4000$ H Bytes

$= (16384)_{10}$ Bytes

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