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Microprocessors

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CLASS TEST 2019-2020

ELECTRICAL ENGINEERING

Date of Test : 09/06/2019

ANSWER KEY ➤ Microprocessors

1.	(d)	7.	(c)	13.	(a)	19.	(c)	25.	(c)
2.	(b)	8.	(c)	14.	(c)	20.	(c)	26.	(d)
3.	(d)	9.	(c)	15.	(a)	21.	(a)	27.	(a)
4.	(a)	10.	(b)	16.	(b)	22.	(d)	28.	(b)
5.	(b)	11.	(a)	17.	(b)	23.	(d)	29.	(c)
6.	(a)	12.	(c)	18.	(a)	24.	(a)	30.	(a)

DETAILED EXPLANATIONS

1. (d)

All instruction clear the accumulator.

```
XRA    A      ; A ⊕ A
ANI    00H    ; A AND 00
MVI    A      ; 00 → A
```

7. (c)

A_0 to A_4 are connected to NAND Gate and $A_5 - A_{15}$ lines are used to select any of 2048 addresses so to

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

So $(0\ 0\ 1\ F)_H$ to $(F\ F\ F\ F)_H$

11. (a)

MVI A, 01H → A = 01H
ORA A → A = 01H, CY = 0, AC = 0
Loop: RAR A → 00H, CY = 1
JNC Loop; statement is false come out from the loop
HLT
So, the loop will be executed 1 time.

12. (c)

The instruction Push B store the contents of BC in the stack. The POP PSW instruction copies the contents of BC in to PSW. The contents of register C will be copied into flag register.

D_0 = 1 = carry flag, D_6 = 0 = zero flag.

13. (a)

```
MVI    B, 89H    ; 89 → B
MOV    A, B      ; B → A
MOV    C, A      ; A → C
MVI    D, 37H    ; 37 → D
Out    Port 1    ; Display A
```

The contents of A is 89 H.

15. (a)

After POP instruction contents of H-L register are given by

H → 23 H
L → 10 H

and After executing SHLD 2050

2050 → 10 H
2051 → 23 H

17. (b)

After executing RAR contents of accumulator becomes $(07)_H$

After executing XCHG instruction contents of DE register pair becomes

D → 21H
E → 00H

STAX, D instruction loads the contents of accumulator into memory location pointed by register DE

So 2100 → $(07)_H$

22. (d)

The bit position of flag register is as follows.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	X	AC	X	P	X	CY

S = 1, P = 0

Result must have odd parity and $D_7 = 1$.

28. (b)

Instructions a and b mask the lower order address and not the higher order address.

ANI OFH; A AND OFH $\rightarrow$ A

ANA B; A AND B $\rightarrow$ A

29. (c)

LXI H, 9258H : 9258H $\rightarrow$ HL

MOV A, M : (9258H) $\rightarrow$ A

CMA : $\overline{A} \rightarrow A$

MOV M, A : A $\rightarrow$ M

This program complements the data of memory location 9258H. Best appropriate option is a.

■■■■