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Digital Electronics

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CLASS TEST 2019-2020

ELECTRICAL ENGINEERING

Date of Test : 04/06/2019

ANSWER KEY ➤ Digital Electronics

1.	(d)	7.	(c)	13.	(a)	19.	(a)	25.	(c)
2.	(b)	8.	(c)	14.	(d)	20.	(b)	26.	(c)
3.	(a)	9.	(c)	15.	(c)	21.	(c)	27.	(d)
4.	(c)	10.	(c)	16.	(b)	22.	(c)	28.	(d)
5.	(c)	11.	(c)	17.	(d)	23.	(a)	29.	(c)
6.	(b)	12.	(a)	18.	(c)	24.	(c)	30.	(b)

DETAILED EXPLANATIONS

1. (d)

Since P is stuck at '1', output Y will be zero if $X = 1$.

Here, $X = (A + B) + (\overline{B}C) = A + (B + \overline{B})(B + C)$

Thus, $X = A + B + C = 1$

2. (b)

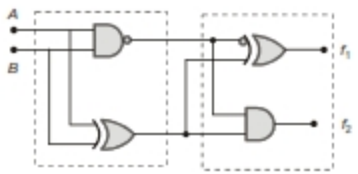
If the Present Count is → 1 0 0 1 1 0 0 1 1 1

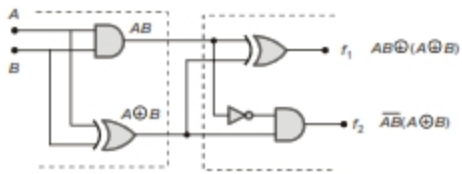
then Next Count will be → 1 0 0 1 1 0 1 0 0 0

We observe that '4' flip-flops are complemented to reach next count.

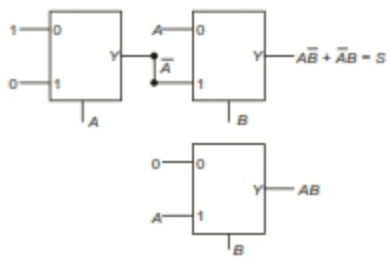
3. (a)

Applying alternate logic symbol for all the four gates and redrawing the circuit bubbled OR gate is NAND gate and $A \odot \overline{B} = A \oplus B$.





5. (c)



7. (c)

number of flip-flops required = 4

maximum delay = 4 × 10 nsec = 40 nsec

8. (c)

$(AB + B\overline{C} + \overline{A}C)(A + C) = AB + AB\overline{C} + ABC + \overline{A}C$

$= AB + \overline{A}C$

9. (c)

Range of signed 1's compliment number is $-2^{n-1} + 1$ to $2^{n-1} - 1$.

10. (c)

Numbers of 4 × 16 decoders required

$$\frac{256}{16} = 16$$

$$\frac{16}{16} = 1 = 16 + 1 = 17$$

11. (c)

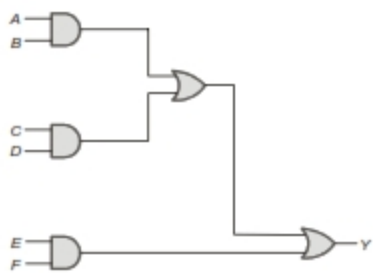
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\overline{D}$	0	2	4	(6)	8	(10)	(12)	14
D	(1)	3	5	(7)	(9)	(11)	13	15
	D	0	0	1	D	1	$\overline{D}$	0

So, the function F is Σm (1, 6, 7, 9, 10, 11, 12).

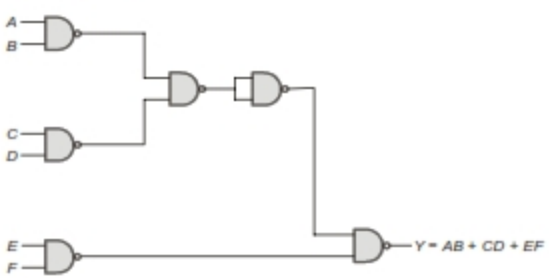
The number of minterms in F is 7 so number of maxterms will be 9.

12. (a)

AND - OR Realization of the function Y is



Equivalent NAND-NAND -realization



So, number of two input NAND gates required is '6'.

13. (a)

Let us consider active high input.

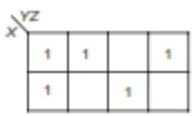
X \ YZ	00	01	11	10
0	0	1	1	0
1	0	1	0	1

$$F = \Sigma(1, 3, 5, 6)$$
$$= \bar{X}Z + \bar{Y}Z + XY\bar{Z}$$
$$= (Y + Z)\cdot(X + Z)\cdot(\bar{X} + \bar{Y} + \bar{Z})$$

14. (d)

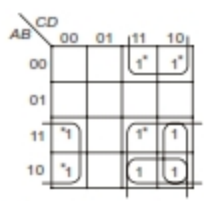
$$F = \overline{(XYZ) \oplus (XY) \oplus (YX) \oplus (XZ)}$$

X	Y	Z	XY	YZ	ZX	XYZ	F
0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	1
0	1	0	0	0	0	0	1
0	1	1	0	1	0	0	0
1	0	0	0	0	0	0	1
1	0	1	0	0	1	0	0
1	1	0	1	0	0	0	0
1	1	1	1	1	1	1	1

$F =$ 

$= \bar{X}\bar{Y} + \bar{Y}\bar{Z} + \bar{Z}\bar{X} + XYZ$

15. (c)



Number of essential prime implicants are 3.

16. (b)

Clock frequency f = 100 KHz

Time period of clock = $T_{CLK} = \frac{1}{f} = \frac{1}{100 \times 10^3}$

$T_{CLK} = 10^{-5}$ sec

∴ Number of bits = $n = 8$

⇒ Maximum conversion time of an 8-bit digital ramp ADC = $(2^n - 1)\, T_{CLK}$

$T_1 = (2^n - 1) \times T_{CLK} = (2^8 - 1) \times 10^{-5} = 2550\ \mu$ sec

Maximum conversion time of successive approximation ADC = $n \,.\, T_{CLK}$

$T_2 = nT$

$T_2 = 8 \times 10^{-5}$ sec $= 80\ \mu$ sec

$$\frac{T_1}{T_2} = \frac{2550}{80} = 31.875 \simeq 31.88$$

17. (d)

Total count $\Rightarrow M = (16383)_{10}$

as we know that,

Number of required flip-flops $(n) \geq \log_2(M+1)$

$$n \geq \log_2(16383+1)$$

$$n \geq \log_2(16384)$$

$$\left\{\log_2 16384 = \frac{\log_{10} 16384}{\log_{10} 2}\right\}$$

$$n \geq 14$$

So, 14 flip-flops are required.

18. (c)

	Q_A	Q_B	Q_C	$Q_A \oplus Q_C$
	1	1	0	1
1	1	0	1	0
2	0	1	0	0
3	1	0	0	1
4	0	0	1	1
5	0	1	1	1

After 5 clock pulse $Q_A\, Q_B\, Q_C$ will be 011.

19. (a)

Analog voltage = resolution × binary equivalent

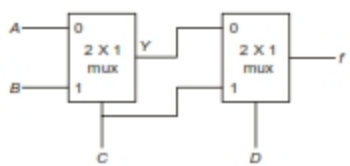
$$= \frac{15}{2^6} \times \left[2^5 \times 0 + 2^4 \times 1 + 2^3 \times 1 + 2^2 \times 1 + 2^1 \times 0 + 2^0 \times 1\right] = 6.79\ \text{V}$$

21. (c)

Race around condition never occurs in dynamic or edge triggering.

Static shift registers are made up of flip-flops while dynamic shift registers are made up of CMOS.

22. (c)

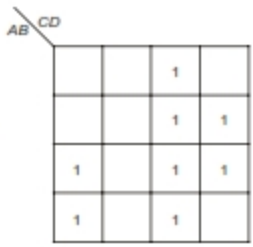


$$Y = A\bar{C} + BC$$

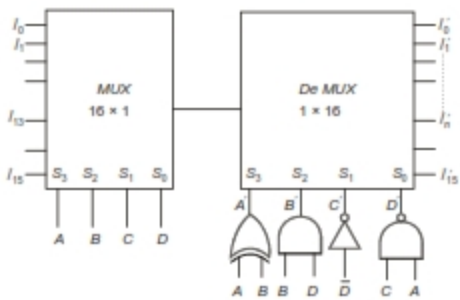
$$f = Y\bar{D} + CD$$

$$f = (A\bar{C} + BC)\bar{D} + CD = A\bar{C}\bar{D} + BC\bar{D} + CD$$

$f(A,B,C,D) = \Sigma m(3, 6, 7, 8, 11, 12, 14, 15)$



23. (a)



$I_{13} \rightarrow A\ B\ C\ D$

$1\ 1\ 0\ 1$

$A' = A \oplus B = 1 \oplus 1 = 0$

$B' = B \cdot D = 1 \cdot 1 = 1$

$C' = \overline{\overline{D}} = D = 1$

$D' = \overline{CA} = \overline{0.1} = 1$

$I_n \rightarrow A'\ B'\ C'\ D'$

$0\ 1\ 1\ 1$

$(A'\ B'\ C'\ D') = 7$

$\Rightarrow \quad n = 7$

24. (c)

Let a number N is given to the system

output after 1's compliment $= 15 - N$

output after 2's compliment $= 16 - 15 + N = N + 1$

3 such systems are connected in cascade.

so final output = Input $+ (3)_{10} = 1010 + 0011 = 1101$

25. (c)

Q_3	Q_2	Q_1
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0
0	0	0

Total number of possible states $= 2^3 = 8$

used states $= 6$

unused states $= 8 - 6 = 2$

26. (c)

$S_1 = A \oplus B$

$C_1 = AB$

$S = (A \oplus B) \oplus AB = (A \oplus B) \cdot \overline{AB} + (\overline{A \oplus B}) \cdot AB$

$= (A\bar{B} + \bar{A}B)(\bar{A} + \bar{B}) + (AB + \bar{A}\bar{B})(A,B) = A\bar{B} + \bar{A}B) + AB = A + B$

$C = (A \oplus B) \cdot AB = (A\bar{B} + \bar{A}B) \cdot AB = 0$

27. (d)

Number of function using n variables is 2^{2^n}.

Since, here $n = 3$, so number of function is 256.

28. (d)

Let us assume initial outputs of both the flip flops to be 0.

Clock	D_1	D_2	Q_1	Q_2	$\overline{Q_1}$	$\overline{Q_2}$	Y
0	1	0	0	0	1	1	0
1	1	1	1	0	0	1	0
2	0	1	1	1	0	0	1
3	0	0	0	1	1	0	0
4	1	0	0	0	1	1	0
5	1	1	1	0	0	1	0
6	0	1	1	1	0	0	1

Thus, the output sequence is Y(0 0 1 0 0 0 1...)

Thus the period of output is four clock cycles. For one clock cycle output is high and for three cycles it is low. Thus,

$$\text{Duty cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100 = \frac{1}{4} \times 100 = 25\%$$

29. (c)

Here

$$J_0 = 1,$$
$$K_0 = Q_2,$$
$$J_1 = \overline{Q}_2 \odot Q_0,$$
$$K_1 = 1,$$
$$J_2 = Q_1,$$
$$K_2 = 1$$

Clock	Present state $Q_2\ Q_1\ Q_0$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$	Next state $Q_2\ Q_1\ Q_0$
0	0 0 0	0 1	0 1	1 0	0 0 1
1	0 0 1	0 1	1 1	1 0	0 1 1
2	0 1 1	1 1	1 1	1 0	1 0 1
3	1 0 1	0 1	0 1	1 1	0 0 0
4	0 0 0	0 1	0 1	1 0	0 0 1

Thus output will have four states (000, 001, 011, 101) and after 115 clock pulses output will be at 101.

30. (b)

$$(10)^3_{16} = (1000)_{16} = (4096)_{10}$$
$$(64)^2_{10} = (X)^2_{10}$$
$$\Rightarrow \quad X = 64$$

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