S.No. : 02 CH1_EE_C+D_210519

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CLASS TEST 2019-2020

ELECTRICAL ENGINEERING

Digital Electronics

Date of Test : 21/05/2019

Answer Key

1.	(b)	7.	(a)	13.	(b)	19.	(d)	25.	(a)
2.	(a)	8.	(b)	14.	(a)	20.	(a)	26.	(c)
3.	(a)	9.	(b)	15.	(b,d)	21.	(a)	27.	(b)
4.	(a)	10.	(a)	16.	(a)	22.	(a)	28.	(a)
5.	(c)	11.	(b)	17.	(c)	23.	(a)	29.	(a)
6.	(d)	12.	(a)	18.	(a)	24.	(b)	30.	(*)

DETAILED EXPLANATIONS

1. (b)

$$0.514 \times 8 = 4.112$$
$$0.112 \times 8 = 0.896$$
$$0.896 \times 8 = 7.168$$
$$0.168 \times 8 = 1.344$$
$$0.344 \times 8 = 2.752$$
$$\therefore \quad (0.514)_{10} = (0.40712)_8$$

2. (a)

Since both PRESET & CLEAR are active low inputs, it will not affect to output status for a given condition. For J = 0, K = 0 input condition output of a JK FF holds. The previous value $Q^+ = Q$

3. (a)

For successive approximation type ADC, conversion time remains the same for any analogue input.

$$\therefore \quad t_{conv} = nT$$
T = Clock period
n = Number of bit

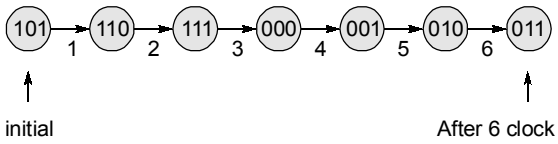
$$T = \frac{1}{1 \times 10^6} = 1\,\mu s$$
$$\therefore \quad t_{con} = 12 \times 1 = 12\,\mu s$$

5. (c)

$$\frac{64}{2} = 32, \quad \frac{32}{2} = 16, \quad \frac{16}{2} = 8$$
$$\frac{8}{2} = 4, \quad \frac{4}{2} = 2, \quad \frac{2}{2} = 1$$
$$\therefore \quad \text{Total} = 32 + 16 + 8 + 4 + 2 + 1 = 63$$

6. (d)

MOD-8 ripple up counter counts from 000 to 111

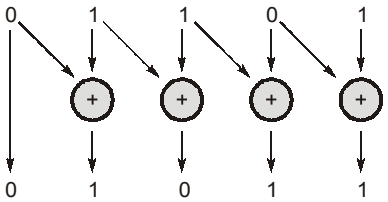


7. (a)

$$\text{Number of chips required} = \frac{\text{Required size of RAM}}{\text{Available size of RAM}} = \frac{64K \times 16}{16K \times 8} = 4 \times 2 = 8$$

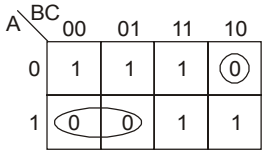
9. (b)

Binary to gray code conversion



10. (a)

k-map simplification



POS expression is $F = (\bar{A} + B) \cdot (A + \bar{B} + C)$

11. (b)

Octal number is obtained by 7's complement of 5264

$$7777 - 5264 = (2513)_8$$

$$\text{Binary equivalent of } (2513)_8 = (010\ 101001\ 011)_2$$

Hexadecimal equivalent of $(010\ 101001\ 011)_2 = (54B)_{16}$

12. (a)

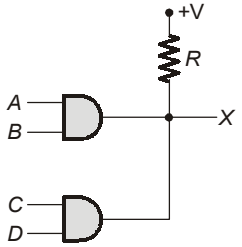
Paralleling of two NAND gate at the input leads to a wire AND

$\therefore$ The logic expression at point x.

$$x = \overline{AB} \cdot \overline{CD}$$

Hence,

$$y = \bar{X} = \overline{\overline{AB} \cdot \overline{CD}} = AB + CD$$



13. (b)

Let n number of flip flop cascaded each having propagation delay of t_{pd}.

Frequency of operation

$$\frac{1}{nt_{pd}} \geq 10\ \text{MHz}$$

$\therefore$

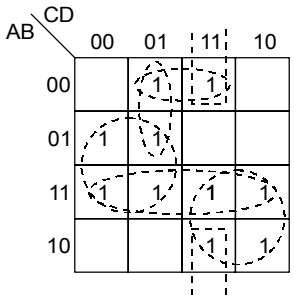
$$n \leq \frac{1}{t_{pd} \times 10\ \text{MHz}} \leq \frac{1}{12 \times 10^{-9} \times 10^{7}} \leq \frac{100}{12}$$

$$n = 8$$

For $n = 8$ MOD number of counter $2^8 = 256$

14. (a)

Drawing k-map

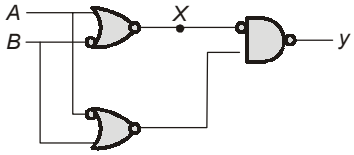


From above k-map it is clear the minterms 4, 10 are grouped only once. Hence the essential prime implicants are $B\bar{C}, AC$.

16. (a)

From figure,

$$X = \overline{A + \bar{B}} = \bar{A}B$$



Similarly,

$$y = \overline{\bar{X} \cdot \bar{A} + B} = X + (\bar{A} + B) = \bar{A}B + A \cdot \bar{B}$$

$$= A \oplus B$$

$\therefore$ X represent BORROW & y represents DIFFERENCE output.

17. (c)

$$\text{Step size} = \frac{\text{Full scale output}}{\text{Number of steps}} = \frac{5V}{2^8 - 1} = 19.607\ \text{mV}$$

For a digital input (10000010) = (130_{10}) analogue output $130 \times 19.607 = 2.549$ V

$$\text{Error} = \pm\frac{0.5 \times 5}{100} = 0.025$$

Expected range of output 2.524 – 2.574 V

18. (a)

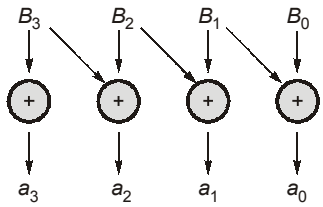
Number of input = 4

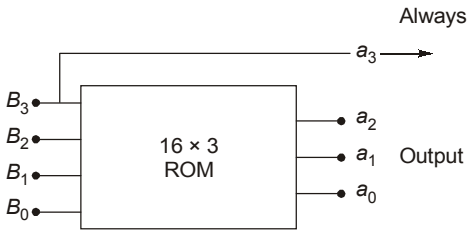
$\therefore$ $a_3 = B_3$

$\therefore$ $a_2 = B_2 \oplus B_3$

$a_1 = B_2 \oplus B_1$

$a_0 = B_1 \oplus B_0$





Size of ROM requires $2^4 \times 3 = 16 \times 3$

19. (d)

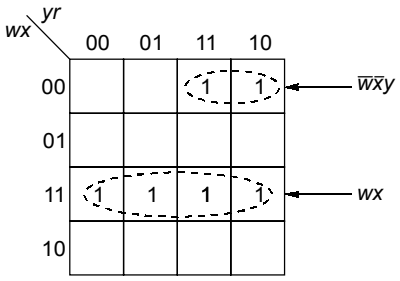
Initial state to be 1000.

CLK	A	B	C	D	X
X	1	0	0	0	0
1	0	1	0	0	1
2	1	0	1	0	1
3	1	1	0	1	0
4	0	1	1	0	0
5	0	0	1	1	0
6	0	0	0	1	1
7	1	0	0	0	0

Hence after 7 clock pulses SIPO shift register comes back to initial state.

20. (a)

k-map simplification



21. (a)

MOD number of BCD counter = 10

MOD number of n bit Johnson counter = $2n$

MOD number of n bit ring counter = n

$\therefore$ Hence MOD number of given counter arrangement = $10 \times 6 \times 2 = 120$

$$f_0 = \frac{f_{clk}}{120}$$

$$f_{ck} = f_0 \times 120 = 24 \text{ kHz}$$

22. (a)

Output y will be high only it

J_2 = X = 1 and C has a low-to-HIGH transition

X will be high only if

A = 1 and B has a LOW-to-HIGH transition.

From above two conditions, it is clear that output y will go high for the following sequence

A - B - C

Analysis:

A = 1 and B goes high, A rising edge of B will trigger flip-flop

$\therefore$ $X = 1$ [$J_1 = 1$; $K_1 = 0$]

Now, C goes high. A rising edge of C will trigger flip-flop 2

$\therefore$ $Y = 1$ [J_2 = X = 1; $K_2 = 0$]

23. (a)

X-Y = X + 2s complement of Y.

2's complement of Y = 1's complement + 1

= 0111100 + 1 = 0111101

X-Y = 1010100

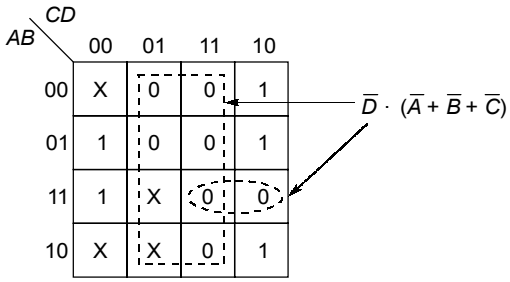
0111101

= **1**0010001

Discard carry, X - Y = 0010001

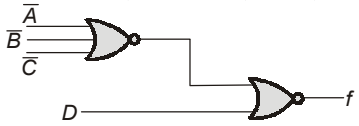
24. (b)

Drawing k-map



POS form is suitable for NOR gate implementation

$$f = \bar{D}(\bar{A}+\bar{B}+\bar{C}) = \overline{\overline{D}(\bar{A}+\bar{B}+\bar{C})} = \overline{D+\overline{\bar{A}+\bar{B}+\bar{C}}}$$



NOT required 1 NOR gate.

$\therefore$ Total 5 NOR gates required.

25. (a)

From figure

$$y = \bar{Q}A + Q\bar{B}$$

Q - Present state

$\therefore$ $$Q^+ = D = y = \bar{Q}A + Q\bar{B}$$

Q^+ = Next state

For $A = 1$, $B = 1$

$$Q^+ = \bar{Q},1 + Q,0 = \bar{Q}$$

For $A = 1$, $B = 0$

$$Q^+ = \bar{Q},1 + Q,1 = 1$$

26. (c)

Select line ABC →	I_0 000	I_1 001	I_2 010	I_3 011	I_4 100	I_5 101	I_6 110	I_7 111
$\bar{D}$	0	(2)	4	6	(8)	10	12	(14)
D	(1)	3	5	(7)	(9)	(11)	13	(15)
	D	$\bar{D}$	0	D	1	D	0	1

27. (b)

Analysis of the circuit, $J = \bar{Q} \oplus x, \quad k = \bar{J}$

x	Q	J	K	Q+
0	0	1	0	1
0	1	0	1	0
1	0	0	1	0
1	1	1	0	1

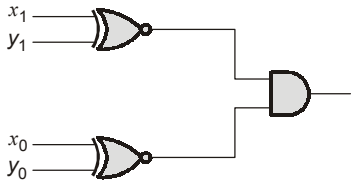
$\therefore$ $$Q(t+1) = x \odot Q(t)$$

28. (a)

Two numbers will be equal if $y_1 = x_1$ and $y_0 = x_0$

Ex-NOR logic gate outputs 1(HIGH) for the same input.

∴ Above condition will be implement as



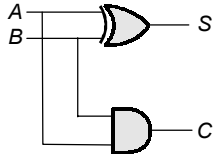
29. (a)

8 bit binary parallel adder can be implemented by 7FA + 1HA

FA = Full adder

HA = Half adder

Half adder



HA requires 1 Ex-OR & 1 AND gate.

1 HA costs 2 + 1 = 3 units

Full adder requires 2HA & 1 OR gate

∴ We total require, 15HA & 7OR gate

∴ Total cost = 15 × cost of HA + 7 × cost of OR gate

= 15 × 3 + 7 × 1

= 52 units

30. (*)

Question data insufficient.

■■■■