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DIGITAL ELECTRONICS

Date of Test : 13/03/2022

ANSWER KEY ➤

1.	(b)	7.	(a)	13.	(a)	19.	(d)	25.	(a)
2.	(a)	8.	(c)	14.	(a)	20.	(d)	26.	(d)
3.	(c)	9.	(d)	15.	(b)	21.	(b)	27.	(b)
4.	(b)	10.	(c)	16.	(d)	22.	(a)	28.	(c)
5.	(c)	11.	(c)	17.	(c)	23.	(d)	29.	(d)
6.	(d)	12.	(c)	18.	(d)	24.	(b)	30.	(a)

DETAILED EXPLANATIONS

1. (b)

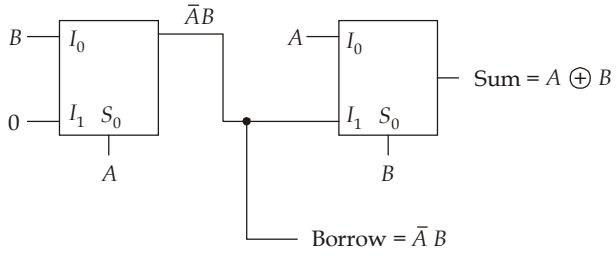
$$X \oplus Y = \overline{X \odot Y} = \overline{\bar{X}\bar{Y} + XY}$$

$$= \overline{(\bar{X}\bar{Y})}\,\overline{(XY)}$$

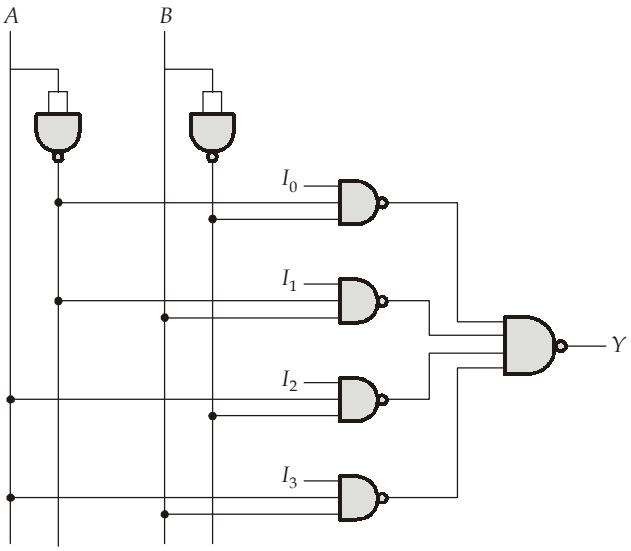
$$= (X + Y)(\bar{X} + \bar{Y})$$

$$= \bar{X} + \bar{Y} \qquad (\because\ X + Y = 1 \text{ which is given})$$

2. (a)



3. (c)



4. (b)

Let $B = 1$ and rest input bit equal to zero. The value of 1 is 5 V

$$\therefore \qquad V_0 = -\frac{5}{4\,\text{k}\Omega} \times 1\,\text{k}\Omega = -1.25\ \text{V}$$

5. (c)

$$f_1(A,B,C) = \Sigma m(2, 3, 4)$$

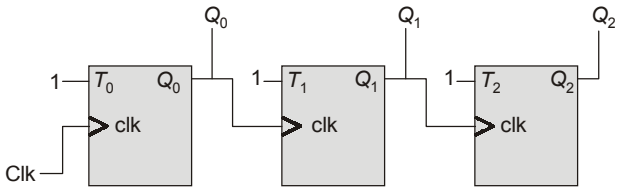
$$f_2(A,B,C) = \Sigma m(2, 3, 4)$$

for output f_{out} to be zero, f_3 should be equal to

$\therefore$ $f_3(A,B,C) = \Sigma m(0, 1, 5, 6, 7)$

Hence, the maximum number of possible minterms = 5.

6. (d)



Thus this will create a MOD 8 or 3 bit down counter.

7. (a)

To represent a state with decimal equivalent of 4, we require minimum "three" flip-flops.

$\because$ $(4)_{10} \rightarrow (100)_2$

8. (c)

$\because$ The logic will perform the function of positive AND gate.

Since,

A (Volt)	B (Volt)	T_1	T_2	T_3	Output
V^-	V^-	OFF	OFF	ON	V_{sat}
V^-	V^+	OFF	ON	ON	V_{sat}
V^+	V^-	ON	OFF	ON	V_{sat}
V^+	V^+	ON	ON	OFF	V_{CC}

The corresponding truth table for negative logic:

A	B	Output
1	1	1
1	0	1
0	1	1
0	0	0

Thus the circuit will behave as negative OR-logic.

9. (d)

$$I_R = I_3 + I_2 + I_0$$
$$= \left(\frac{E_{reff}}{2R} + \frac{E_{reff}}{4R} + \frac{E_{reff}}{16R}\right) = \left(\frac{10}{10} + \frac{10}{20} + \frac{10}{80}\right)$$
$$= \frac{130}{80} = \frac{13}{8} = 1.625 \text{ mA}$$

10. (c)

Writing the equation in expanded decimal form, we get,

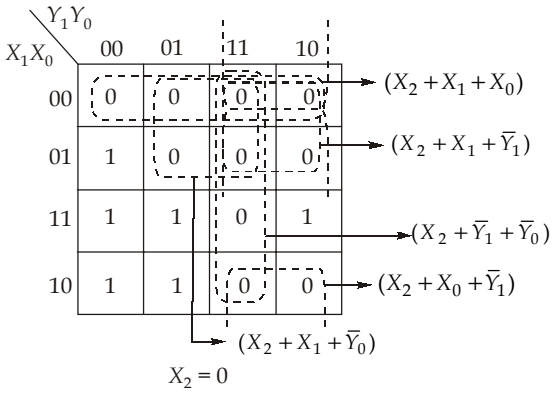
$$(2x + 4) + (x + 7) = 4x$$
$$3x + 11 = 4x$$
$$x = 11$$

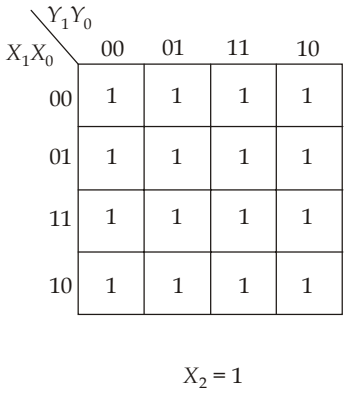
11. (c)

Now, $X > Y$ if

(a) $X_2 = 1$

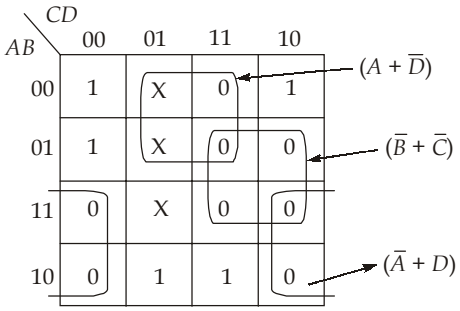
(b) $X_2 = 0$ and $X_1X_0 > Y_1Y_0$





12. (c)

The above expression can be represented in *K*-map as,



13. (a)

$[D' + AB' + A'C + AC'D + A'C'D]'$

$= [D' + AC'D + AB' + A'C + A'C'D]'$

$= [D' + AC' + AB' + A' [C + C'D]]'$

$= [D' + AC' + AB' + A' [C + D]]'$

$= [D' + AC' + AB' + A'C + A'D]'$

$(\because\ D' + A'D = D' + A')$

$= [D' + A' + AC' + AB' + A'C]'$

$(\because\ A' + A'C = A')$

$(\because\ A' + AC' + AB' = A'+A(C'+B') = A' + C' + B')$

$= [D' + A' + C' + B']'$

$= ABCD$

Hence, only 1 minterm is required.

14. (a)

Let

$$\begin{array}{lcccc} A = & & a_2 & a_1 & a_0 \\ B = & & & b_1 & b_0 \\ \hline A \times B = & & a_2b_0 & a_1b_0 & a_0b_0 \\ & b_1a_2 & b_1a_1 & b_1a_0 & \downarrow \\ \hline & b_1a_2 & (a_2b_0 + a_1b_1) & (a_1b_0 + b_1a_0) & a_0b_0 \\ & C_3 & C_2 & C_1 & C_0 \end{array}$$

Number of AND gates required $X = 6$

Number of one bit full adders required $Y = 3$

$$X + Y = 6 + 3 = 9$$

15. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

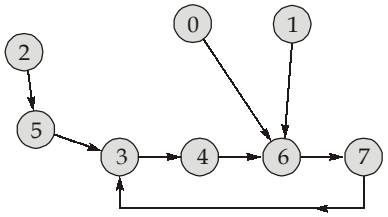
$\therefore$ $Y = Q_2 \oplus Q_1 \oplus Q_0$

$= 1 \oplus 0 \oplus 1 = 0$

16. (d)

Test for Lockout

Present State			Present Input						Next State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1	1	0	1	1	1	0
0	0	1	1	1	1	1	0	1	1	1	0
0	1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	1	1	0	0	0	0	1	1



Hence, the counter does not enter into lockout state.

19. (d)

$\because$ $Q + \bar{Q} = 1$ always, thus the flip-flop will toggle always.

$\therefore$ $f_{out} = \frac{f_{clk}}{2} = \frac{10}{2} \times 10^3 = 5\,\text{kHz}$

20. (d)

At first cycle, the inputs of flip-flop are

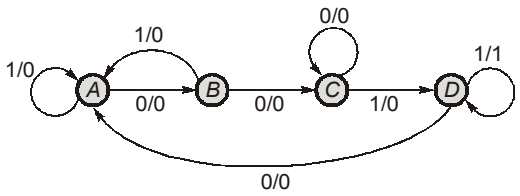
$J_2K_2 = 1\ 0$ (Set)
$J_1K_1 = 0\ 1$ (Reset)
$J_0K_0 = 0\ 1$ (Reset)

$\therefore$ $Q_2 = 1$
$Q_1 = 0$
$Q_0 = 0$

$\therefore$ Output $(Q_2Q_1Q_0) = (100)_2$

21. (b)

The state diagram can be drawn as



Hence, minimum number of states = 4.

22. (a)

$f(A, B, C, ...) = A + \bar{A}B + \bar{A}\bar{B}C + ...$

$= A + \bar{A}(B + \bar{B}C + \bar{B}\bar{C}D + ...)$

$= A + \bar{A}X$ (where $X = B + \bar{B}C + \bar{B}\bar{C}D + ...$)

$= A + X$ ($\because A + \bar{A}X = A + X$)

$= A + B + \bar{B}C + \bar{B}\bar{C}D + ...$

$= A + B + \bar{B}(C + \bar{C}D + ...)$

$= A + B + C + ...$

Hence, option (a) is correct.

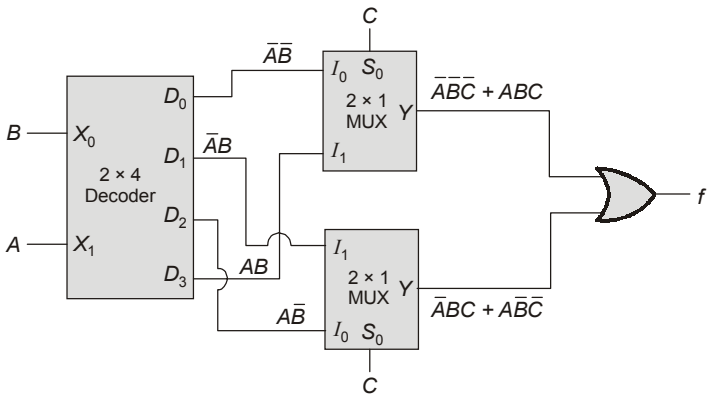
23. (d)

The input can be determined by constructing an input table as follows:

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	⓪	1	②	3	④	5	⑥	⑦
A	8	⑨	10	11	12	13	⑭	⑮
	$\bar{A}$	A	$\bar{A}$	0	$\bar{A}$	0	1	1

24. (b)

The above circuit can be redrawn as



Thus, $f = \underbrace{\bar{A}\bar{B}\bar{C} + ABC} + \underbrace{\bar{A}BC + A\bar{B}\bar{C}}$

$= \bar{B}\bar{C}(A + \bar{A}) + BC(\bar{A} + \bar{A})$

$= \bar{B}\bar{C} + BC$

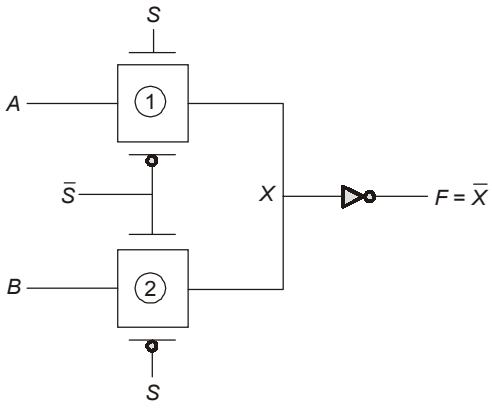
$= B \odot C$

25. (a)

To create a 16K × 8 ROM chip we require eight 2K × 4 chips in series and two such block of 8 chips to be connected in parallel to make the output line of 8 bits.

Hence, a total number of 16 chips are required.

26. (d)



Equivalent Circuit

From the equivalent circuit, it can be concluded that,

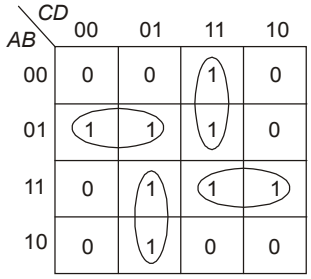
$\bar{F} = X = AS + B\bar{S}$

$\therefore \quad F = \overline{AS + B\bar{S}}$

For $S = 1$, $\quad F = \bar{A}$

27. (b)

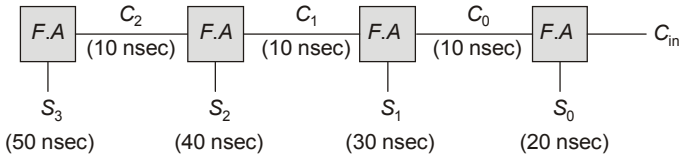
To find the essential prime implicants, we have to select those groups in which there is atleast one min-term which is part of only that group and cannot be grouped by any other way.



So, there are 4 prime implicants in the given *K*-map.

28. (c)

The 4-bit parallel adder can be analyzed as follows:



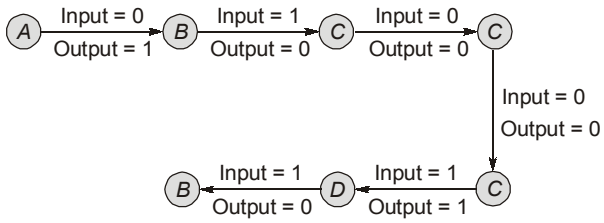
Thus, the last sum bit will be generated in 50 nsec.

Thus, the maximum rate of 4-bit additions possible is,

$$\frac{1}{50\times10^{-9}}/\text{sec} = \frac{10^9}{50}/\text{sec} = 20\times10^6/\text{sec}$$

29. (d)

For the given input, the output can be determined by following the sequence of states as given below.



From the above diagram it is clear that, the output goes to 1 for two times for the given input.

30. (a)

$$\text{Input} = (A+B)\odot C$$

Now,

Clk	Register	Input
Initially	1000	$(1+0)\odot0=0$
1	0100	$(0+1)\odot0=0$
2	0010	$(0+0)\odot1=0$
3	0001	$(0+0)\odot0=1$
4	1000	

■■■■